TechNexion

March 6th 2011

SOM

TDM-3730 System on Module

TechNexion

TDM-3730

TDM-3730 System on Module

Hardware Manual

Rev A

1 Contents

2 Revision

Revision	Date	Description	Created by
0.90	21/06/2011	Preliminary version	TechNexion
A	05/07/2011	First public version	TechNexion
A-01	11/08/2011	Change in Wifi signals description	TechNexion
A-02	06/03/2012	Add Chapter about multiplexing in Software	TechNexion

3 Care and Maintenance

3.1 General

Your device is a product of superior design and craftsmanship and should be treated with care. The following suggestions will help you.

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

These suggestions apply equally to your device, battery, charger, or any enhancement. If any device is not working properly, take it to the nearest authorized service facility for service.

3.2 Regulatory Information

Disposal of Waste Equipment by Users in Private Household in the European Union

This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service or the shop where you purchased the product.

We hereby declare that the product is in compliance with the essential requirements and other relevant provisions of European Directive 1999/5/EC (radio equipment and telecommunications terminal equipment Directive).

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The Compliance of RoHS New Requirement

According to the new requirements in directive 2002/95/EC, DecaBDE is added with specification starting by July 1, 2008 as follows:

Cadmium (Cd)	: Under 100ppm
Lead (Pb)	: Under 1000ppm
Mercury (Hg)	: Under 1000ppm
Hexavalent Chromium (Cr6)	: Under 1000ppm
PBB	: Under 1000ppm
PBDE (include DecaBDE)	: Under 1000ppm

Please confirm and send back, thanks.

RoHS Compliance Statement

We aware the change in this directive and our product can meet this new specification as above.

Company Stamp

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Federal Communications Commission (FCC) Unintentional emitter per FCC Part 15

This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio or television reception. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio and television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

■ Reorient or relocate the receiving antenna

■ Increase the separation between the equipment and receiver

■ Connect the equipment to an outlet on a different circuit from that to which the receiver is connected

■ Consult the dealer or an experienced radio/TV technician for help.

WARNING! To reduce the possibility of heat-related injuries or of overheating the computer, do not place the computer directly on your lap or obstruct the computer air vents. Use the computer only on a hard, flat surface. Do not allow another hard surface, such as an adjoining optional printer, or a soft surface, such as pillows or rugs or clothing, to block airflow. Also, do not allow the AC adapter to contact the skin or a soft surface, such as pillows or rugs or clothing, during operation. The computer and the AC adapter comply with the user-accessible surface temperature limits defined by the International Standard for Safety of Information Technology Equipment (IEC 60950).

4 Description

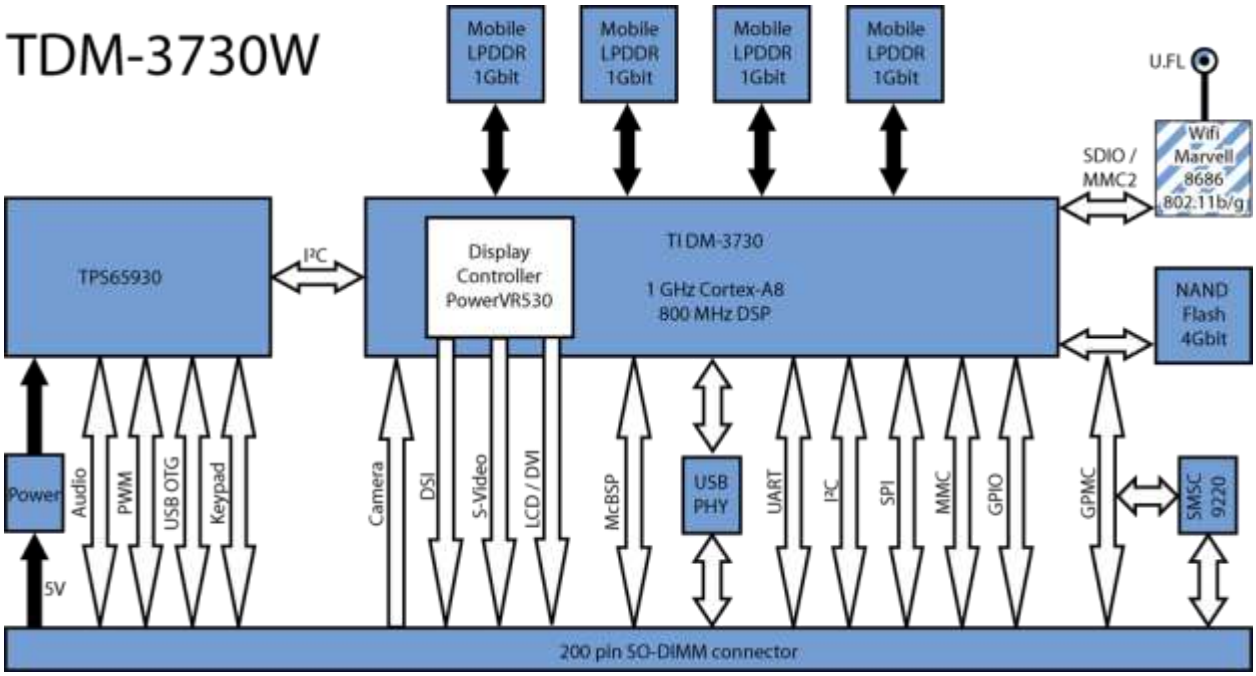
The TDM-3730 Is a highly integrated System on Module (SOM) containing the TI ARM Cortex A8 DaVinci DM3730 processor, PMIC, Wireless LAN, USB PHY, LAN Controller, Memory and NAND Flash.
The high-performance, digital media processors are based on the enhanced device architecture and are integrated on advanced 45-nm process technology. This architecture is designed to provide best in class ARM and Graphics performance while delivering low power consumption. This balance of performance and power allow the device to support the following example applications:

- Portable Data Terminals
- Navigation
- Auto Infotainment
- Gaming
- Medical Imaging
- Home Automation
- Human Interface
- Industrial Control
- Test and Measurement
- Single board Computers

The device can support numerous HLOS and RTOS solutions including Linux, Android and Windows Embedded CE by TechNexion and/ or third parties.

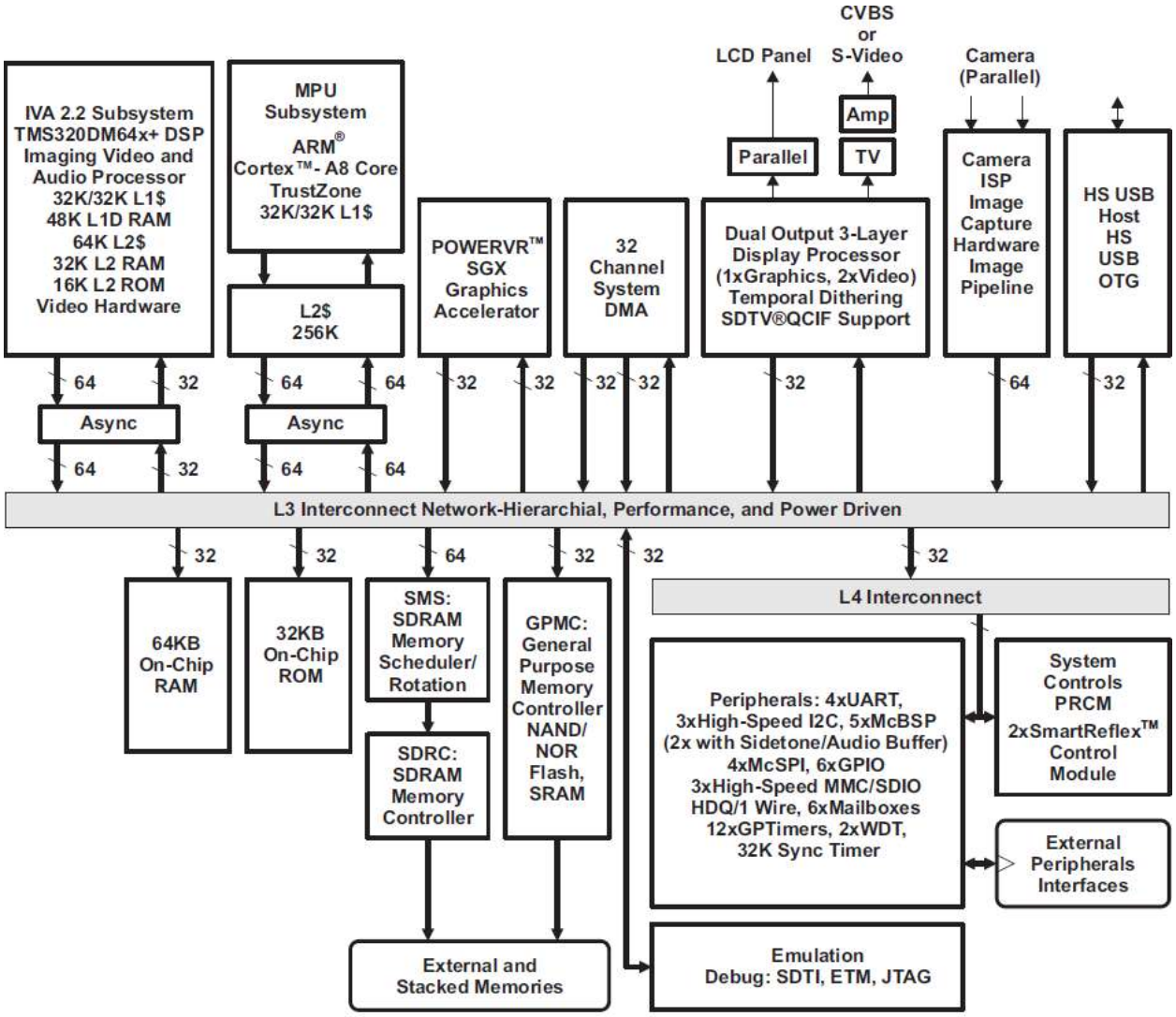
One can always check our website (www.technexion.com) for additional product detail information, mechanical design files, software programming guides, source code software and custom baseboard creation guideline.

4.1 Block Diagram TDM-3730 System on Module



4.2 Functional Block Diagram CPU

The functional block diagram of the DM3730 Digital Media Processor is shown below.



DM3730 Functional Block Diagram

5 System Components

5.1 CPU: DM-3730

5.1.1 DM-3730 Digital Media Processor Features

Texas Instruments (TI) DM3730 Digital Media Processor

- Compatible with OMAP™ 3 Architecture
- ARM® Microprocessor (MPU) Subsystem
  - Up to 1-GHz ARM® Cortex™-A8 Core Also supports 300, 600, and 800-MHz operation
  - NEON™ SIMD Coprocessor
- High Performance Image, Video, Audio (IVA2.2TM) Accelerator Subsystem
  - Up to 800-MHz TMS320C64x+TM DSP Core Also supports 260, 520, and 660-MHz operation
  - Enhanced Direct Memory Access (EDMA) Controller (128 Independent Channels)
  - Video Hardware Accelerators
- POWERVR SGX™ Graphics Accelerator
  - Tile Based Architecture Delivering up to 20 MPoly/sec
  - Universal Scalable Shader Engine: Multi-threaded Engine Incorporating Pixel and Vertex Shader Functionality
  - Industry Standard API Support: OpenGLES 1.1 and 2.0, OpenVG1.0
  - Fine Grained Task Switching, Load Balancing, and Power Management
  - Programmable High Quality Image Anti-Aliasing
- Advanced Very-Long-Instruction-Word (VLIW) TMS320C64x+TM DSP Core
  - Eight Highly Independent Functional Units
  - Six ALUs (32-/40-Bit); Each Supports Single 32- bit, Dual 16-bit, or Quad 8-bit, Arithmetic per Clock Cycle
  - Two Multipliers Support Four 16 x 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-Bit Results) per Clock Cycle
  - Load-Store Architecture With Non-Aligned Support
  - 64 32-Bit General-Purpose Registers
  - Instruction Packing Reduces Code Size
  - All Instructions Conditional
  - Additional C64x+TM Enhancements
    - Protected Mode Operation
    - Expectations Support for Error Detection and Program Redirection
    - Hardware Support for Modulo Loop Operation
- C64x+TM L1/L2 Memory Architecture
  - 32K-Byte L1P Program RAM/Cache (Direct Mapped)
  - 80K-Byte L1D Data RAM/Cache (2-Way Set- Associative)
  - 64K-Byte L2 Unified Mapped RAM/Cache (4- Way Set-Associative)
  - 32K-Byte L2 Shared SRAM and 16K-Byte L2 ROM

- C64x+TM Instruction Set Features
  - Byte-Addressable (8-/16-/32-/64-Bit Data)
  - 8-Bit Overflow Protection
  - Bit-Field Extract, Set, Clear
  - Normalization, Saturation, Bit-Counting
  - Compact 16-Bit Instructions
  - Additional Instructions to Support Complex Multiplies
- 1.8-V I/O and 3.0-V (MMC1 only), 0.9-V to 1.2-V Adaptive Processor CoreVoltage

  0.9-V to 1.1-V Adaptive Core Logic Voltage

  Note: These are default Operating Performance Point (OPP) voltages and could be optimized to lower values using SmartReflex AVS.

- Serial Communication
  - Multichannel Buffered Serial Ports (McBSPs)
    - 512 Byte Transmit/Receive Buffer (McBSP3)
    - 5K-Byte Transmit/Receive Buffer (McBSP2)
    - SIDETONE Core Support (McBSP2 and 3 Only) For Filter, Gain, and Mix Operations
    - Direct Interface to I2S and PCM Device and T Buses
    - 128 Channel Transmit/Receive Mode
  - Master/Slave Multichannel Serial Port Interface (McSPI) Ports
  - High-Speed/Full-Speed/Low-Speed USB OTG Subsystem (12-/8-Pin ULPI Interface)
  - High-Speed/Full-Speed/Low-Speed Multiport USB Host Subsystem
    - 12-/8-Pin ULPI Interface or 6-/4-/3-Pin Serial Interface
  - One HDQ/1-Wire Interface
  - UARTs (One with Infrared Data Association [IrDA] and Consumer Infrared [CIR] Modes)
  - Master/Slave High-Speed Inter-Integrated Circuit (I2C) Controllers
- Camera Image Signal Processing (ISP)
  - CCD and CMOS Imager Interface
  - Memory Data Input
  - BT.601/BT.656 Digital YCbCr 4:2:2 (8-/10-Bit) Interface
  - Glueless Interface to Common Video Decoders
  - Resize Engine
    - Resize Images From 1/4x to 4x
    - Separate Horizontal/Vertical Control
- System Direct Memory Access (SDMA) Controller (32 Logical Channels With Configurable Priority)
- Comprehensive Power, Reset, and Clock Management
  - SmartReflexTM Technology

    - Dynamic Voltage and Frequency Scaling (DVFS)
- ARM® Cortex™-A8 Core
    - ARMv7 Architecture
        - TrustZone®
        - Thumb®-2
        - MMU Enhancements
    - In-Order, Dual-Issue, Superscalar Microprocessor Core
    - NEON Multimedia Architecture
    - Over 2x Performance of ARMv6 SIMD
    - Supports Both Integer and Floating Point SIMD
    - Jazelle® RCT Execution Environment Architecture
    - Dynamic Branch Prediction with Branch Target Address Cache, Global History Buffer, and 8-Entry Return Stack
    - Embedded Trace Macrocell (ETM) Support for Non-Invasive Debug
- ARM Cortex-A8 Memory Architecture:
    - 32K-Byte Instruction Cache (4-Way Set-Associative)
    - 32K-Byte Data Cache (4-Way Set-Associative)
    - 256K-Byte L2 Cache
- 32K-Byte ROM
- 64K-Byte Shared SRAM
- Endianess:
    - ARM Instructions - Little Endian
    - ARM Data – Configurable
    - DSP Instructions/Data - Little Endian
- Removable Media Interfaces:
    - Multimedia Card (MMC)/ Secure Digital (SD) With Secure Data I/O (SDIO)
- Test Interfaces
    - IEEE-1149.1 (JTAG) Boundary-Scan Compatible
    - Embedded Trace Macro Interface (ETM)
    - Serial Data Transport Interface (SDTI
- Up to 125 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions)
- 45-nm CMOS Technology
- CPU Package:
    - 423-pin s-PBGA package (CUS Suffix), .65mm Ball Pitch

5.2 PMIC: TPS-65930

5.2.1 TPS-65930 – Introduction

The TPS65930 devices are power-management ICs for OMAP™ and other mobile applications. The devices include power-management, a universal serial bus (USB) high-speed (HS) transceiver, light -emitting diode (LED) drivers, an analog-to-digital converter (ADC), a real-time clock (RTC), and embedded power control (EPC). In addition, the TPS65930 includes a full audio codec with two digital-to-analog converters (DACs) and two ADCs to implement dual voice channels, and a stereo downlink channel that can play all standard audio sample rates through a multiple format inter-integrated sound (I2S™)/time division multiplexing (TDM) interface.

These optimized devices support the power and peripheral requirements of the OMAP application processors. The power portion of the devices contains three buck converters, two controllable by a dedicated SmartReflex™ class-3 interface, multiple low dropout (LDO) regulators, an EPC to manage the power sequencing requirements of OMAP, and an RTC and backup module. The RTC can be powered by a backup battery when the main supply is not present, and the devices include a coin-cell charger to recharge the backup battery as needed.

The USB module provides a HS 2.0 OTG transceiver suitable for direct connection to the OMAP UTMI+ low pin interface (ULPI), with an integrated charge pump and full support for the carkit CEA-936A specification. An ADC is provided for monitoring signals, such as supply voltage, entering the device, and two additional external ADC inputs are provided for system use.

The devices provide driver circuitry to power two LED circuits that can illuminate a panel or provide user indicators. The drivers also provide pulse width modulation (PWM) circuits to control the illumination levels of the LEDs. A keypad interface implements a built-in scanning algorithm to decode hardware-based key presses and reduce software use, with multiple additional general-purpose input/output devices (GPIOs) that can be used as interrupts when configured as inputs.

5.2.2 TPS-65930: Features

The TPS65930 devices offer the following features:

- Audio:
  - Differential input main microphones
  - Mono auxiliary input
  - External predrivers for class D (stereo)
  - Automatic level control (ALC)
  - Digital and analog mixing
  - 16-bit linear audio stereo DAC (96, 48, 44.1, and 32 kHz and derivatives)
  - 16-bit linear audio stereo ADC (48, 44.1, and 32 kHz and derivatives)
- USB:
  - USB 2.0 on-the-go (OTG)-compliant HS transceivers
  - 12-bit universal transceiver macro interface ULPI
  - USB power supply (5-V charge pump for VBUS)
- Additional Features:
  - Keypad Interface (up to 6 × 6)
- Backup battery charger

5.3 Memory

The TDM-3730 has a dual channel 32 bit External Memory Interfaces (EMI) controller.

Each 32 bit wide channel is connected 16 bit wide to two Hynix H5MS1G62AFR MOBILE DDR SDRAM Chips SDRAM_nCS0 and SDRAM_nCS1 signals are used to select them.

The standard configuration is organized as 1Gbit (4Bank x 16M x 16bits). Therefore given 4 chips are used a total of 4Gbit or 512MB of memory is available.

Features:

- Mobile DDR SDRAM
  - Double data rate architecture: two data transfer per clock cycle
- Mobile DDR SDRAM INTERFACE
  - x16 bus width
  - Multiplexed Address (Row address and Column address)
- SUPPLY VOLTAGE
  - 1.8V device: VDD and VDDQ = 1.7V to 1.95V
- MEMORY CELL ARRAY
  - 1Gbit (x16 device) = 4Bank x 16Mb x 16 I/O
- DATA STROBE
  - x16 device: LDQS and UDQS
  - Bidirectional, data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
  - Data and data mask referenced to both edges of DQS
- LOW POWER FEATURES
  - PASR (Partial Array Self Refresh)
  - AUTO TCSR (Temperature Compensated Self Refresh)
  - DS (Drive Strength)
- INPUT CLOCK
  - Differential clock inputs (CK, CK)
- Data MASK
  - LDM and UDM: Input mask signals for write data
  - DM masks write data-in at the both rising and falling edges of the data strobe
- MODE and EXTENDED MODE REGISTER SET and STATUS REGISTER READ
  - Keep to the JEDEC Standard regulation (Low Power DDR SDRAM)
- CAS LATENCY
  - Programmable CAS latency 2 or 3 supported
- BURST LENGTH
  - Programmable burst length 2 / 4 / 8 with both sequential and interleave mode
- AUTO PRECHARGE
  - Option for each burst access
- AUTO REFRESH AND SELF REFRESH MODE
- CLOCK STOP MODE
  - Keep to the JEDEC Standard regulation
- INITIALIZING THE MOBILE DDR SDRAM
  - Occurring at device power up or interruption of device power

5.4 NAND Flash

NAND on the TDM-3730 is populated as Micron MT29F4G16ABBDAH4D and connected 16 bit wide to the DM3730 GPMC bus.

The default TDM-3730 supports the chip which provides 512MB of addressable space.

The GPMC_nCS0 signal is used for it's selection.

Features:

- Open NAND Flash Interface (ONFI) 1.0-compliant
- Single-level cell (SLC) technology
- Organization
  - Page size x8: 2112 bytes (2048 + 64 bytes)
  - Page size x16: 1056 words (1024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Plane size: 2 planes x 2048 blocks per plane
  - Device size: 4Gb: 4096 blocks; 8Gb: 8192 blocks
- Asynchronous I/O performance
  - tRC/tWC: 20ns (3.3V), 25ns (1.8V)
- Array performance
  - Read page: 25µs
  - Program page: 200µs (TYP: 1.8V, 3.3V)
  - Erase block: 700µs (TYP)
- Command set: ONFI NAND Flash Protocol
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Ready/Busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: Write protect entire device
- First block (block address 00h) is valid when shipped from factory with ECC. For minimum required ECC, see Error Management.
- Block 0 requires 1-bit ECC if PROGRAM/ERASE cycles are less than 1000
- RESET (FFh) required as first command after poweron
- Alternate method of device initialization (Nand_Init) after power up (contact factory)
- Internal data move operations supported within the plane from which data is read
- Quality and reliability
  - Data retention: 10 years
  - Endurance: 100,000 PROGRAM/ERASE cycles

5.5 Network: SMSC LAN9220

The LAN9220 is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9220 is fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant, and supports HP Auto-MDIX. The variable voltage I/O signals of the LAN9220 accommodate lower voltage I/O signaling without the need for voltage level shifters.

Qualified Magnetics – Magnetics listed under this heading have been tested in order to verify proper operation with the specific device listed with it.

Suggested magnetic – Magnetics listed under this heading have ***not*** been tested in order to verify proper operation with the specific device listed with it. This category of magnetic has been evaluated by the contents of the vendor supplied datasheet and legacy performance only.

Vendor	Part Number	Package	Temp
Qualified Magnetics			
UDE	RT7-115A1K1A	Integrated RJ45	0° - +70° C
Pulse	H1102	16-pin SOIC	0° - +70° C
Halo	TG110-RP55N5	16-pin SOIC	0° - +70° C
Halo	HFJ11-RP26E- L12RL	Integrated RJ45	0° - +70° C
Delta	RJSE1R5310A	Integrated RJ45	0° - +70° C
Pulse	HX1188	16-pin SOIC	-40° - +85° C
Halo	TG110-RPE5N5	16-pin SOIC	-40° - +85° C
Halo	HFJ11-RPE26E-L12RL	Integrated RJ45	-40° - +85° C
TDK	TLA-6T717W	Integrated RJ45	-40° - +85° C
Delta	LFE8505T	16-pin SOIC	-40° - +85° C
Suggested Magnetics			
Pulse	J0011D01B	Integrated RJ45	0° - +70° C
Midcom	000-7219-35	Cardbus	0° - +70° C
Bothhand	TS6121C	16-pin SOIC	0° - +70° C
Bothhand	LU1S041X-43	Integrated RJ45	0° - +70° C
Midcom	000-7090-37R	16-pin SOIC	-40° - +85° C
Midcom	MIC66211-5171T- LF3	Integrated RJ45	-40° - +85° C
Elec & Eltek	820-M0323R	16-pin SOIC	-40° - +85° C

5.6 USB PHY

The SMSC USB3320 is a Hi-Speed USB 2.0 transceiver that provides a configurable physical layer (PHY) solution and is an excellent macth for a wide variety of products. USB3320 uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB Transceiver to the link. ULPI uses a method of in-band signalling and status byte transfers between the link and transceiver to facilitate a USB session with only 12 pins.

5.7 WiFi Module

The Marvell® 88W8686 is a low-power highly-integrated IEEE 802.11g/b MAC/Baseband/RF WLAN system-on-chip (SoC), designed to support IEEE 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps, as well as 802.11b data rates of 1, 2, 5.5, and 11 Mbps.

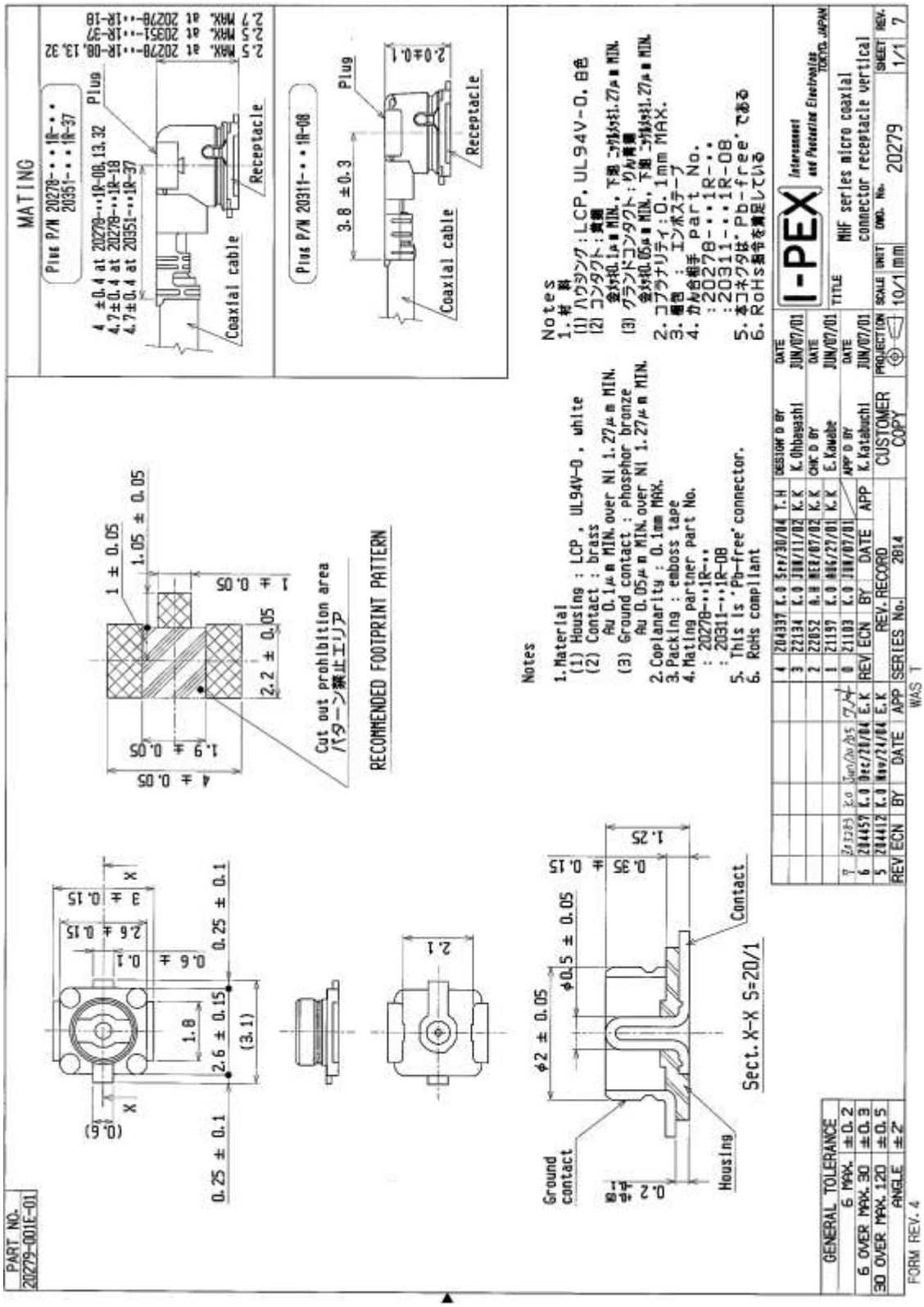
General features:

- Ultra low-power dissipation
- Single-chip integration of 802.11g/b wireless RF and baseband, MAC, CPU, memory, and host interfaces
- Integrates all RF to baseband transmit and receive operations, with support for external PAs
- Fully integrated frequency synthesizers with optimized phase noise performance for OFDM applications
- Integrated direct conversion WLAN RF radio
- Supports 19.2, 20, 24, 26, 38.4, and 40 MHz oscillator clock sources
- Software backward compatible with 88W8385 and 88W8015 devices

5.7.1 WiFi Signals Description

SIGNAL NAME	DESCRIPTION
MMC2_CLK	Clock
MMC2_CMD	Command
MMC2_d0	4 bit data
MMC2_d1	4 bit data
MMC2_d2	4 bit data
MMC2_d3	4 bit data
GPIO54	Reserved
GPIO 157	Wifi enable – power on

5.7.2 I-PEX Connector



6 How to use the Multiplex Mode

The function of the pins on the module can be changed by adjusting the multiplex mode (mux).

6.1 Multiplexing in u-boot (Linux)

Multiplexing can be done in u-boot in the tdm3730.h file

(Use the file in this directory: board/technexion/tdm3730/tdm3730.h)

Example of what it might look like:

```
MUX_VAL(CP(ETK_D2),     (IEN|PTD|EN|M4))
```

The last part "M4" is the multiplex mode and you can change that according the table in the Chapter 7.

The line of code is build up as follows:

- The name of the variable is the function in Mode 0; ETK_D2
- The current Multiplex mode is M4, which means that currently this pin is GPIO_16

Pin #	Ball #	Pin Name	mode	V	type	description
84	AC7	MCSPI3 CS0	1	1.8	IO	SPI Enable 0, polarity configured by software
		etk_d2	0		O	ETK data 2
		GPIO_16	4		IO	General-purpose IO 16
		Mm1_txdat	5		IO	USB data. Used as VP in 4-pin VP_VM mode
		Hw_dbg4	7		O	Debug signal 4

Table 1: Example of pin 84 on the TDM-3730 module and the different functions for each multiplex mode (see Chapter 7)

After this you will need to recompile:

```
Uboot#          make distclean
Uboot#          make tdm3730_config
Uboot#          make tdm3730
```

This will create the u-boot.bin

6.2 Multiplexing in Windows Embedded Compact 7

Change the following file:

C:\WINCE700\platform\TN_TDM_3730\SRC\INC\bsp_padcfg.h

Change code :

```
#define GPIO_PADS_37XX  \

        PAD_ENTRY(ETK_D4,   INPUT_DISABLED | MUXMODE(4))     /* GPIO 18 */ \
```

Then recompile

7 TDM-3730 Module Pin Description

Pin #	Ball #	Pin Name	mode	V	type	description
1	X	VBUS_5V		5	I	Power
2	X	DC_5V		5	I	5V
3	X	GND		GND	GND	Power
4	X	DC_5V		5	I	5V
5	X	PreDriv.RIGHT			O	Predriver output right P for external class-D amplifier
6	X	DC_5V		5	I	5V
7	X	PreDriv.LEFT			O	Predriver output left P for external class-D amplifier
8	X	DC_5V		5	I	5V
9	X	MIC_BIAS_G		GND	GND	Dedicated ground for microphones
10	X	DC_5V		5	I	5V
11	X	MIC_MAIN_P		2.5/ 2.75	I	Main microphone left input (P)
12	X	DC_5V		5	I	5V
13	X	PWR_ON		4.2	I	Input; detect a control command to start or stop the system
14	AA10	SYS_nRESPWRON	0	1.8	I	Power On Reset
15	X	HOST nOC		1.8	IO	HOST nOC
16	X	RESETB				USB PHY
17	X	SYSEN		1.8	OD	System enable output
18	X	LEDA		4.2	D	User definable LED Indicator
19	X	GND		GND	GND	Power
20	X	MMC1 CD		1.8	IO	Card Detection1
21	X	HSUSB ID		4.2	IO	USB ID
22	X	LCD PWM		1.8	IO	LCD Backlight on/off
23	X	MIC MAIN M		2.5/ 2.75	I	Main microphone left input (M)
24	X	AUXR		2.5/ 2.75	I	Auxiliary audio input right
25	X	MIC BIAS		2.5/ 2.75	Pwr	Analog microphone bias 1
26	X	CHRG STATE		1.5	IO	Battery type
27	X	VIO 1V8		1.8	O	Power
28	X	DVI_nDISABLE		1.8	IO	DVI/ Backlight control
29	X	VIO 1V8		1.8	O	Power
30	X	LCD ENBKL		1.8	IO	LCD Backlight Control
31	X	VIO 1V8		1.8	O	Power
32	X	HSUSB DN		4.2		USB data N/USB carkit transmit data
33	X	VIO 1V8		1.8	O	Power

Pin #	Ball #	Pin Name	mode	V	type	description
34	X	HSUSB DP		4.2	IO	USB data P/USB carkit receive data
35	X	IDM0			IOA	USB PHY 3320C
36	X	ADCIN2		2.5/ 2.75	I	General –purpose ADC Input
37	X	IDP0			IOA	USB PHY 3320C
38	X	CAM IO		4.2		VBAT.RIGHT - VAUX2.OUT
39	X	VMMC1		4.2	O	Power
40	R4	MCSPI1 SIMO	0	1.8	IO	Slave data in, master data out
		MMC2_dat5	1		IO	MMC/SD Card Data bit 5
		GPIO_172	4		IO	General-purpose IO 172
		Safe_mode	7			
41	T5	MCSPI1 CLK	0	1.8	IO	SPI Clock
		MMC2_dat4	1		IO	MMC/SD Card Data bit 4
		GPIO_171	4		IO	General-purpose IO 171
		Safe_mode	7			
42	X	KPD.C4		1.8	D	Keypad column 4
43	T4	MCSPI1 SOMI	0	1.8	IO	Slave data out, master data in
		Mmc2_dat6	1		IO	MMC/SD Card Data bit 6
		GPIO_173	4		IO	General-purpose IO 173
		Safe_mode	7			
44	X	KPD.C3		1.8	D	Keypad column 3
45	T6	mcspi1_cs0	0	1.8	IO	SPI Enable 0, polarity configured by software
		Mmc2_dat7	1		IO	MMC/SD Card Data bit 7
		GPIO_174	4		IO	General-purpose IO 174
		Safe_mode	7			
46	X	KPD.C2		1.8	D	Keypad column 2
47	V4	mcbsp3_fsx	0	1.8	IO	Combined frame synchronization
		Uart2_rx	1		I	UART2 Receive data
		GPIO_143	4		IO	General-purpose IO 143
		Safe_mode	7			
48	X	KPD.C1		1.8	D	Keypad column 1
49	V5	Mcbsp3_dr	0	1.8	I	Received serial data
		Uart2_rts	1		O	UART2 request to send
		GPIO_141	4		IO	General-purpose IO 141
		Safe mode	7			
50	X	KPD.C0		1.8	D	Keypad column 0
51	W4	MCBSP3 CLKX	0	1.8	IO	Combined serial clock
		UArt 2_TX	1		O	UART2_transmit data
		GPIO_142	4		IO	General-purpose IO 142
		Safe mode	7			
52	X	KPD.R4		1.8	I	Keypad row 4

Pin #	Ball #	Pin Name	mode	V	type	description
53	V6	MCBSP3_DX	0	1.8	IO	Transmitted serial data
		UART2_CTS	1		I	UART2_CTS
		GPIO_140	4		IO	General-purpose IO 140
		Safe mode	7			
54	X	KPD.R3		1.8	I	Keypad row 3
55	T21	MCBSP2_CLKX	0	1.8	IO	Combined serial Clock
		GPIO_117	4		IO	General-purpose IO 117
		Safe_mode	7			
56	X	KPD.R2		1.8	I	Keypad row 2
57	AB16	Sys_boot 5	0	1.8	I	Boot configuration mode bit 5
		Mmc2_dir_dat3	1		O	Direction control for DAT4, DAT5, DAT6, and DAT7 signals case an external transceiver used
		Dss_data22	3		O	LCD Pixel Data bit 22
		GPIO_7	4		IO	General-purpose IO 7
		Safe_mode	7			
58	X	KPD.R1		1.8	I	Keypad row 1
59	R20	Mcbsp2_dx	0	1.8	IO	Transmitted serial data
		GPIO_119	4		IO	General-purpose IO 119
		Safe mode	7			
60	X	KPD.R0		1.8	I	Keypad row 0
61	V19	Mcbsp2_dr	0	1.8	IO	Received serial data
		GPIO_118	4		IO	General-purpose IO 118
		Safe mode	7			
62	X	KPD.R5		1.8	I	Keypad row 5
63	V20	Mcbsp2_fsx	0	1.8	IO	Combined frame synchronization
		GPIO_116	4		IO	General-purpose IO 116
		Safe mode	7			
64	AA1	LCD PON	4	1.8	IO	General-purpose IO 139
		Mmc2_dat7	0		IO	MMC/ SD Card Data bit 7
		Mmc2_clkin	1		I	MMC/ SD Input Clock
		Mmc3_dat3	3		IO	MMC/ SD Card Data bit 3
		Mm3_rxdm	6		IO	Transmit enable
		Safe mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
65	AA2	LCD_INI	4	1.8	IO	General-purpose IO 137
		Mmc2_dat5	0		IO	MMC/SD card data bit 5
		Mmc2_dir_dat1	1		O	Direction control for DAT1 and DAT3 signals case an external transceiver used
		Cam_global_reset	2		IO	Global reset is used strobe synchronization
		Mmc3_dat1	3		IO	MMC/SD Card Data bit 1
		Mm3_rxdp	6		IO	Vplus receive data (not used in 3- or 4-pin configurations)
		Safe mode	7			
66	Y2	LCD_envdd	4	1.8	IO	General-purpose IO 138
		Mmc2_dat6	0		IO	MMC/SD Card Data bit 6
		Mmc2_dir_cmd	1		O	Direction control for CMD signal case an external transceiver is used
		Cam_shutter	2		O	Mechanical shutter control signal
		Mmc3_dat2	3		IO	MMC/SD Card Data bit 2
		Safe mode	7			
67	AB2	TS nPEN IRQ	4	1.8	IO	General-purpose IO 136
		Mmc2_dat4	0		IO	MMC/SD Card Data bit 4
		Mmc2_dir_dat0	1		O	Direction control for DAT2 signal case an external transceiver used
		Mmc3_dat0	3		IO	MMC/SD Card Data bit 0 / SPI Serial Input
		Safe mode	7			
68	AC1	GPIO_12	4	1.8	IO	General-purpose IO 12
		etk_clk	0		O	ETK trace clock
		mcbsp5_ clkx	1		IO	Combined serial clock
		mmc3_clk	2		O	MMC/SD Output Clock
		mm1_rxdp	5		IO	Vplus receive data (not used in 3- or 4-pin configurations)
		hw_dbg0	7		O	Debug signal 0
69	AD2	GPIO_19	4	1.8	IO	General-purpose IO 19
		etk_d5	0		O	ETK data 5
		mcbsp5_fsx	1		IO	Combined frame synchronization
		mmc3_dat1	2		IO	MMC/SD Card Data bit 1
		hw_dbg7	7		O	Debug signal 7
70	X	GND		GND	GND	Ground
71	Y7	Sys_clkout1	0	1.8	O	Configurable output clock1
		GPIO_10	4		IO	General-purpose IO 10
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
72	AD3	GPIO_13	4	1.8	IO	General-purpose IO 13
		etk_ctl	0		O	ETK trace ctl
		mmc3_cmd	2		IO	MMC/SD command signal
		hw_dbg1	7		O	Debug signal 1
73	AC12	I2C3_sda	0	1.8	IOD	I2C Serial Bidirectional Data. Output is open drain.
		GPIO_185	4		IO	General-purpose IO 185
		Safe mode	7			
74	AC5	GPIO_18	4	1.8	IO	General-purpose IO 18
		Etk_d4	0		O	ETK data 4
		Mcbsp5_dr	1		I	Received serial data
		Mmc3_dat0	2		IO	MMC/SD Card Data bit 0 / SPI Serial Input
		Hw_dbg6	7		O	Debug signal 6
75	AC13	I2C3 SCL	0	1.8	OD	I2C Master Serial clock. Output is open drain
		GPIO_184	4		IO	General-purpose IO 184
		safemode	7			
76	AC14	I2C2 SDA	0	1.8	IOD	I2C Serial Bidirectional Data. Output is open drain.
		GPIO_183	4		IO	General-purpose IO 183
		Safe_mode	7			
77	AD6	MCSPI3 SIMO	1	1.8	IO	Slave data in, master data out IO
		Etk_d0	0		O	ATK data 0
		Mmc3_dat4	2		IO	MMC/SD Card Data bit 4
		GPIO_14	4		IO	General-purpose IO 14
		Mm1_rxcv	5		IO	Differential receiver signal input (not used in 3-pin mode)
		Hw_dbg2	7		O	Debug signal 2
78	AC15	I2C2 SCL	0	1.8	OD	I2C Master Serial clock. Output is open drain
		GPIO_168	4		IO	General-purpose IO 168
		Safe_mode	7			
79	X	GND		GND	GND	Ground
80	AC6	MCSPI3 SOMI	1	1.8	IO	Slave data out, master data in
		Etk_d1	0		O	ETK data 1
		GPIO_15	4		IO	General-purpose IO 15
		Mm1_txse0	5		IO	Single-ended zero. Used as VM in 4-pin VP_VM mode.
		Hw_dbg3	7		O	Debug signal 3

Pin #	Ball #	Pin Name	mode	V	type	description
81	AD9	MCSPI3_CS1	1	1.8	O	SPI Enable 1, polarity configured by software
		etk_d7	0		O	ETK data 7
		mmc3_dat7	2		IO	MMC/SD Card Data bit 7
		GPIO_21	4		IO	General-purpose IO 21
		mm1_txen_n	5		IO	Transmit enable
		hw_dbg9	7		O	Debug signal 9
82	AD8	MCSPI3 CLK	1	1.8	IO	SPI Clock
		Etk_d3	0		O	ETK data 3
		Mmc3_dat3	2		IO	MMC/SD Card Data bit 3
		GPIO_17	4		IO	General-purpose IO 17
		Hw_dbg5	7		O	Debug signal 5
83	AB24	TV SVIDEO Y	0	1.8	AO	TV analog output Composite: cvideo1_out
84	AC7	MCSPI3 CS0	1	1.8	IO	SPI Enable 0, polarity configured by software
		etk_d2	0		O	ETK data 2
		GPIO_16	4		IO	General-purpose IO 16
		Mm1_txdat	5		IO	USB data. Used as VP in 4-pin VP_VM mode
		Hw_dbg4	7		O	Debug signal 4
85	AA23	TV SVIDEO C	0	1.8	AO	TV analog output S-VIDEO: cvideo2_out
86	AC2	UART1 CTS	0	1.8	I	UART1 Clear To Send
		GPIO_150	4		IO	General-purpose IO 150
		Safe_mode	7			
87	W6	UART1 RTS	0	1.8	O	UART1 Request To Send
		GPIO_149	4		IO	General-purpose IO 149
		Safe_mode	7			
88	AD5	Mmc1_WP	4	1.8	IO	General-purpose IO 23
		Etk_d9	0		O	ETK data 9
		Mmc3_dat5	2		IO	MMC/SD Card Data bit 5
		Mm1_rxdm	5		IO	Vminus receive data (not used in 3- or 4-pin configurations)
		Hw_dbg11	7		O	Debug signal 11
89	W7	UART1 TX	0	1.8	O	UART1 Transmit data
		GPIO_148	4		IO	General-purpose IO 148
		Safe_mode	7			
90	AC8	GPIO_20	4	1.8	IO	General-purpose IO 20
		Etk_d6	0		O	ETK data 6
		Mcbsp5_dx	1		O	Transmitted serial data O AF13
		Mmc3_dat2	2		IO	MMC/SD Card Data bit 2
		Hw_dbg8	7		O	Debug signal 8
91	X	KPD.C5		1.8	D	Keypad column 5

Pin #	Ball #	Pin Name	mode	V	type	description
92	V7	UART1 RX	0	1.8	I	UART1 Receive data
		Mcbsp1_clkr	2		IO	Receive Clock
		Mcspi4_clk	3		IO	SPI Clock
		GPIO_151	4		IO	General-purpose IO 151
		Safe mode	7			
93	N23	MMC1 DAT3	0	1.8/ 3.3	IO	MMC/SD Card Data bit 3
		GPIO125 (2)	4		IO	General-purpose IO 125
		Safe mode	7			
94	M20	MMC1 DAT2	0	1.8/ 3.3	IO	MMC/SD Card Data bit 2
		GPIO_124 (2)	4		IO	General-purpose IO 124
		Safe mode	7			
95	M23	MMC1 CLK0	0	1.8/ 3.3	O	MMC/SD Output Clock
		GPIO_120 (2)	4		IO	General-purpose IO 120
		Safe mode	7			
96	M21	MMC1 DAT1	0	1.8/ 3.3	IO	MMC/SD Card Data bit 1
		GPIO_123 (2)	4		IO	General-purpose IO 123
		Safe mode	7			
97	M22	MMC1 DAT0	0	1.8/ 3.3	IO	MMC/SD Card Data bit 0/ SPI Serial Input
		GPIO_122 (2)	4		IO	General-purpose IO 122
		Safe_mode	7			
98	K22	DSS D21	0	1.8	O	LCD Pixel Data bit 21
		Mcspi3_cs0	2		IO	SPI Enable 0, polarity configured by software
		Dss_data3	3		IO	LCD Pixel Data bit 3
		GPIO_91	4		IO	General-purpose IO 91
		Safe_mode	7			
99	L23	MMC1 CMD	0	1.8/ 3.3	IO	MMC/SD command signal
		GPIO_121 (2)	4		IO	General-purpose IO 121
		Safe_mode	7			
100	J21	DSS ACBIAS	0	1.8	O	AC bias control (STN) or pixel data enable (TFT) output
		GPIO_69	4		IO	General-purpose IO 69
		Safe_mode	7			
101	J22	DSS D16	0	1.8	IO	LCD Pixel Data bit 16
		GPIO_86	4		IO	General-purpose IO 86
		Safe_mode	7			
102	AC22	DSS D10	0	1.8	IO	LCD Pixel Data bit 10
		GPIO_80	4		IO	General-purpose IO 80
		Safe_mode	7			
103	H23	Dss_data19	0	1.8	IO	LCD Pixel Data bit 19
		mcspi3_simo	2		IO	Slave data in, master data out
		dss_data1	3		IO	LCD Pixel Data bit 1
		GPIO_89	4		IO	General-purpose IO 89
		safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
104	AC23	Dss_data11	0	1.8	IO	LCD Pixel Data bit 11
		GPIO_81	4		IO	General-purpose IO 81
		Safe mode	7			
105	G24	Dss_data18	0	1.8	IO	LCD Pixel Data bit 18
		mcspi3_clk	2		IO	SPI Clock
		dss_data0	3		IO	LCD Pixel Data bit 0
		GPIO_88	4		IO	General-purpose IO 88
		safe_mode	7			
106	AD21	Dss_data4	0	1.8	IO	LCD Pixel data bit 4
		Uart3_rx_irrx	2		I	UART3 Receive data, IR and Remote RX
		GPIO_74	4		IO	General-purpose IO 74
		Safe mode	7			
107	G23	Dss_data17	0	1.8	IO	LCD Pixel data bit 17
		GPIO_87	4		IO	General-purpose IO 87
		Safe mode	7			
108	AB22	Dss_data12	0	1.8	IO	LCD Pixel data bit 12
		GPIO_82	4		IO	General-purpose IO 82
		Safe mode	7			
109	G22	Dss_pclk	0	1.8	O	LCD Pixel Clock
		GPIO_66	4		IO	General-purpose IO 66
		Hw_dbg12	5		O	Debug signal 12
		Safe mode	7			
110	AC21	Dss_data5	0	1.8	IO	LCD Pixel data bit 5
		Uart3_tx_irtx	2		O	UART3 Transmit data, IR TX
		GPIO_75	4		IO	General-purpose IO 75
		Safe mode	7			
111	F23	Dss_data9	0	1.8	IO	LCD Pixel data bit 8
		Uart3_tx_irtx	2		O	UART3 Transmit data, IR TX
		GPIO_79	4		IO	General-purpose IO 79
		Hw_dbg17	5		O	Debug signal 17
		Safe mode	7			
112	AC19	Dss_data0	0	1.8	IO	LCD Pixel Data bit 0
		Uart1_cts	2		I	UART1 Clear To Send
		GPIO_70	4		IO	General-purpose IO 70
		Safe mode	7			
113	F22	Dss_vsync	0	1.8	O	LCD Vertical Synchronization
		GPIO_68	4		IO	General-purpose IO 68
		Safe mode	7			
114	AD20	Dss_data2	0	1.8	IO	LCD Pixel Data bit 2
		GPIO_72	4		IO	General-purpose IO 72
		Safe mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
115	E24	Dss_data8	0	1.8	IO	LCD Pixel Data bit 8
		Uart3_rx_irrx	2		I	UART3 Transmit data, IR TX
		GPIO_78	4		IO	General-purpose IO 78
		Hw_dbg16	5		O	Debug signal 16
		Safe Mode	7			
116	AC20	Dss_data3	0	1.8	IO	LCD Pixel Data bit 3
		GPIO_73	4		IO	General-purpose IO 73
		Safe mode	7			
117	E23	Dss_data7	0	1.8	IO	LCD Pixel Data bit 7
		Uart1_rx	2		I	UART1 Receive data
		GPIO_77	4		IO	General-purpose IO 77
		Hw_dbg15	5		O	Debug signal 15
		Safe_mode	7			
118	AB19	Dss-d1	0	1.8	IO	LCD Pixel Data bit 11
		Uart1_rts	2		O	UART1 Request To Send
		GPIO_71	4		IO	General-purpose IO 71
		Safe_mode	7			
119	D24	Dss_data6	0	1.8	IO	LCD Pixel Data bit 6
		Uart1_rx	2		I	UART1 Receive data
		GPIO76	4		IO	General-purpose IO 76
		Hw_dbg14	5		O	Debug signal 14
		Safe mode	7			
120	Y22	Dss_data13	0	1.8	IO	LCD Pixel Data bit 13
		GPIO_83	4		IO	General-purpose IO 83
		Safe mode	7			
121	D23	Dss_data20	0	1.8	O	LCD Pixel Data bit 20
		Mcspi3_somi	2		IO	Slave data out, master data in
		Dss_data3	3		IO	LCD Pixel Data bit 3
		GPIO_91	4		IO	General-purpose IO 91
		Safe mode	7			
122	W22	Dss_data14	0	1.8	IO	LCD Pixel Data bit 14
		GPIO_84	4		IO	General-purpose IO 84
		Safe_mode	7			
123	E22	Dss_hsync	0	1.8	O	LCD Horizontal Synchronization
		GPIO_67	4		IO	General-purpose IO 67
		Hw_dbg13	5		O	Debug signal 13
		Safe_mode	7			
124	W21	Dss_data23	0	1.8	O	LCD Pixel Data bit 23
		Dss_data5	3		IO	LCD Pixel Data bit 5
		GPIO_93	4		IO	General-purpose IO 93
		Safe_mode	7			
125	X	GND		GND	GND	Ground

Pin #	Ball #	Pin Name	mode	V	type	description
126	V21	Dss_data22	0	1.8	O	LCD Pixel Data bit 22
		Mcspi3_cs1	2		O	SPI Enable 1, polarity configured by software
		Dss_data4	3		IO	LCD Pixel Data bit 4
		GPIO_92	4		IO	General-purpose IO 92
		Safe_mode	7			
127	C23	UART3 TX	0	1.8	O	UART3 Transmit data, IR TX
		GPIO_166	4		IO	General-purpose IO 166
		Safe_mode	7			
128	V22	Dss_data15	0	1.8	IO	LCD Pixel Data bit 15
		GPIO_85	4		IO	General-purpose IO 85
		Safe_mode	7			
129	B24	UART3_RX_IRRX	0	1.8	I	UART3 Receive data, IR and Remote RX
		GPIO_165	4		IO	General-purpose IO 165
		Safe_mode	7			
130	X	GND		GND	GND	Ground
131	B23	UART3_RTS_SD	0	1.8	O	UART3 Request To Send, IR enable
		GPIO_164	4		IO	General-purpose IO 164
		Safe mode	7			
132	AB18	Cam_d0	0	1.8	I	Camera digital image data bit 0
		GPIO_99 (1)	4		I	General-purpose IO 99
		Safe mode	7			
133	A24	HDQ_SIO	0	1.8	IOD	Bidirectional HDQ 1-Wire control and data Interface. Output is open drain.
		Sys_altclk	1		I	Alternate clock source selectable for GPTIMERs (maximum 54 MHz), USB (48 MHz), or NTSC/PAL (54 MHz)
		i2c2_sccbe	2		OD	Serial Camera Control Bus Enable
		i2c3_sccbe	3		OD	Serial Camera Control Bus Enable
		GPIO_170	4		IO	General-purpose IO 170
		Safe_mode	7			
134	AC18	Cam_d1	0	1.8	I	Camera digital image data bit 1
		GPIO-100 (1)	4		I	General-purpose IO 100
		Safe mode	7			
135	A23	UART3 CTS	0	1.8	IO	UART3 Clear To Send (input), Remote TX (output)
		GPIO_163	4		IO	General-purpose IO 163
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
136	L24	Cam_d6	0	1.8	I	Camera digital image data bit 6
		GPIO_105 (1)	4		I	General-purpose IO 105
		Safe_mode	7			
137	G21	Cam_d11	0	1.8	I	Camera digital image data bit 11
		GPIO_110	4		IO	General-purpose IO 110
		Hw_dbg9	5		O	Debug signal 9
		Safe_mode	7			
138	K24	Cam_d7	0	1.8	I	Camera digital image data bit 7
		GPIO_106 (1)	4		I	General-purpose IO 106
		Safe_mode	7			
139	J20	Cam_strobe	0	1.8	O	Flash strobe control signal
		GPIO_126	4		IO	General-purpose IO 126
		Hw_dbg11	5		O	Debug signal 11
		Safe_mode	7			
140	K23	CAM D9	0	1.8	I	Camera digital image data bit 9
		GPIO_108 (1)	4		I	General-purpose IO 108
		Safe_mode	7			
141	F21	CAM D10	0	1.8	I	Camera digital image data bit 10
		GPIO_109	4		IO	General-purpose IO 109
		Hw_dbg8	5		O	Debug signal 8
		Safe_mode	7			
142	J23	Cam_d8	0	1.8	I	Camera digital image data bit 8
		GPIO_107 (1)	4		I	General-purpose IO 107
		Safe_mode	7			
143	C22	Cam xclkb	0	1.8	O	Camera clock output b
		GPIO_111	4		IO	General-purpose IO 111
		Safe_mode	7			
144	H24	Cam_fld	0	1.8	IO	Camera fiel identification
		Cam_global_reset	2		IO	Global reset is used strobe synchronization
		GPIO_98	4		IO	General-purpose IO 98
		Hw_dbg3	5		O	Debug signal 3
		Safe_mode	7			
145	A22	Cam_hs	0	1.8	IO	Camera horizontal synchronization
		GPIO_94	4		IO	General-purpose IO 94
		Hw_dbg0	5		O	Debug signal 0
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
146	J19	Cam_pclk	0	1.8	I	Camera pixel clock
		GPIO_97	4		IO	General-purpose IO 97
		Hw_dbg2	5		O	Debug signal 2
		Safe_mode	7			
147	B22	Cam_xclka	0	1.8	O	Camera clock output a
		GPIO_96	4		IO	General-purpose IO 96
		Safe_mode	7			
148	G19	Cam_d2	0	1.8	I	Camera digital image data bit 2
		GPIO_102	4		IO	General-purpose IO 102
		Hw_dbg5	5		O	Debug signal 5
		Safe_mode	7			
149	F18	Cam_wen	0	1.8	I	Camera write enable
		Cam_shutter	2		O	Mechanical shutter control signal
		GPIO_167	4		IO	General-purpose IO 167
		Hw_dbg10	5		O	Debug signal 10
		Safe_mode	7			
150	G20	Cam_d4	0	1.8	I	Camera digital image data bit 4
		GPIO_103	4		IO	General-purpose IO 103
		Hw_dbg6	5		O	Debug signal 6
		Safe_mode	7			
151	B21	Cam_d5	0	1.8	I	Camera digital image data bit 5
		GPIO_104	4		IO	General-purpose IO 104
		Hw_dbg7	5		O	Debug signal 7
		Safe_mode	7			
152	F19	Cam_d3	0	1.8	I	Camera digital image data bit 3
		GPIO_102	4		IO	General-purpose IO 102
		Hw_dbg5	5		O	Debug signal 5
		Safe_mode	7			
153	E18	Cam_vs	0	1.8	IO	Camera vertical synchronization
		GPIO_95	4		IO	General-purpose IO 95
		Hw_dbg1	5		O	Debug signal 1
		Safe_mode	7			
154	R2	GPMC_d8 (3)	0	1.8	IO	GPMC data bit 8
		GPIO_44	4		IO	General-purpose IO 44
		Safe_mode	7			
155	T2	GPMC_d9 (3)	0	1.8	IO	GPMC data bit 8
		GPIO_45	4		IO	General-purpose IO 45
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
156	V2	GPMC_d15 (3)	0	1.8	IO	GPMC data bit 15
		GPIO_51	4		IO	General-purpose IO 51
		Safe_mode	7			
157	U1	GPMC_d10 (3)	0	1.8	IO	GPMC data bit 10
		GPIO_46	4		IO	General-purpose IO 46
		Safe_mode	7			
158	U2	GPMC_d13 (3)	0	1.8	IO	GPMC data bit 13
		GPIO_49	4		IO	General-purpose IO 49
		Safe_mode	7			
159	T3	GPMC_d12 (3)	0	1.8	IO	GPMC data bit 12
		GPIO_48	4		IO	General-purpose IO 48
		Safe_mode	7			
160	M3	GPMC_d4 (3)	0	1.8	IO	GPMC data bit 4
161	P2	GPMC_d6	0	1.8	IO	GPMC data bit 6
162	V1	GPMC_d14 (3)	0	1.8	IO	GPMC data bit 14
		GPIO_50	4		IO	General-purpose IO 50
		Safe_mode	7			
163	P1	GPMC_d5 (3)	0	1.8	IO	GPMC data bit 5
164	R1	GPMC_d7 (3)	0	1.8	IO	GPMC data bit 7
165	W2	GPMC_clk	0	1.8	O	GPMC clock
		GPIO_59	4		IO	General-purpose IO 59
		Safe_mode	7			
166	R3	GPMC_d11 (3)	0	1.8	IO	GPMC data bit 11
		GPIO_47	4		IO	General-purpose IO 47
		Safe_mode	7			
167	X	GND		GND	GND	Ground
168	X	GND		GND	GND	Ground
169	M2	GPMC_d2 (3)	0	1.8	IO	GPMC data bit 2
170	N2	GPMC_d3 (3)	0	1.8	IO	GPMC data bit 3
171	M1	GPMC_d1 (3)	0	1.8	IO	GPMC data bit 1
172	F2	GPMC_noe	0	1.8	O	Output enable
173	G3	GPMC_nwe	0	1.8	O	Write enable
174	L2	GPMC_d0 (3)	0	1.8	IO	GPMC data bit 0
175	J2	GPMC_a6 (4)	0	1.8	O	GPMC output address bit 6
		GPIO_39	4		IO	General-purpose IO 39
		Safe_mode	7			
176	K3	GPMC_a2 (4)	0	1.8	O	GPMC output address bit 2
		GPIO_35	4		IO	General-purpose IO 35
		Safe_mode	7			
177	X	GND		GND	GND	Ground

Pin #	Ball #	Pin Name	mode	V	type	description
178	G2	GPMC_a10 (4)	0	1.8	O	GPMC output address bit 10
		Sys_ndmareq3	1		I	External A request 3 (system expansion). Level (active low) or edge (falling) selectable.
		GPIO_43	4		IO	General-purpose IO 43
		Safe mode	7			
179	J1	GPMC_a7 (4)	0	1.8	O	GPMC output address bit 7
		GPIO_40	4		IO	General-purpose IO 40
		Safe_mode	7			
180	X	GND		GND	GND	Ground
181	K5	GPMC_nbe0_cle	0	1.8	O	Lower Byte Enable. Also used for Command Latch Enable
		GPIO_60	4		IO	General-purpose IO 60
		Safe_mode	7			
182	F1	GPMC_nadv_ale	0	1.8	O	Address Valid or Address Latch Enable
183	J3	GPMC_a5 (4)	0	1.8	O	GPMC output address bit 5
		GPIO_38	4		IO	General-purpose IO 38
		Safe_mode	7			
184	G4	GPMC_ncs7	0	1.8	O	GPMC chip select bit 7
		GPMC_io_dir	1		O	GPMC IO direction control for use with external transceivers
		Mcbsp4_fsx	2		IO	Combined frame synchronization
		Gpt_8_pwm_evt	3		IO	PWM or event for GP timer 8
		GPIO_58	4		IO	General-purpose IO 58
		Safe_mode	7			
185	K2	GPMC_a3 (4)	0	1.8	O	GPMC output address bit 3
		GPIO_36	4		IO	General-purpose IO 36
		Safe_mode	7			
186	J4	GPMC_a4 (4)	0	1.8	O	GPMC output address bit 4
		GPIO_37	4		IO	General-purpose IO 37
		Safe_mode	7			
187	K4	GPMC_a1 (4)	0	1.8	O	GPMC output address bit 1
		GPIO_34	4		IO	General-purpose IO 34
		Safe_mode	7			
188	H2	GPMC_a9	0	1.8	O	GPMC output address bit 9
		Sys_ndmareq2	1		I	External A request 2 (system expansion). Level (active low) or edge (falling) selectable.
		GPIO_42	4		IO	General-purpose IO 42
		Safe_mode	7			
189	H1	GPMC_a8	0	1.8	O	GPMC output address bit 8
		GPIO_41	4		IO	General-purpose IO 41
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
190	C2	GPMC_wait3	0	1.8	I	External indication of wait
		Sys_ndmareq1	1		I	External A request 1 (system expansion). Level (active low) or edge (falling) selectable.
		Uart4_rx	2		I	UART4 Receive data
		GPIO_65	4		O	General-purpose IO 65
		Safe_mode	7			
191	X	Ether_txn			AO	LAN9220: transmit negative output
192	F4	GPMC_ncs4	0	1.8	O	GPMC Chip Select bit 4
		Sys_ndmareq1	1		I	External A request 1 (system expansion). Level (active low) or edge (falling) selectable.
		Mcbsp4_clkx	2		IO	Combined serial clock
		Gpt_9_pwm_evt	3		IO	PWM or event for GP timer 9
		GPIO_55	4		IO	General-purpose IO 55
		Safe_mode	7			
193	X	Ether_txp			AO	LAN9220: transmit positive output
194	F3	GPMC_nxs6	0	1.8	O	GPMC chip select bit 6
		Sys_ndmareq3	1		I	External A request 3 (system expansion). Level (active low) or edge (falling) selectable.
		Mcbsp4_dx	2		IO	Transmitted serial data
		Gpt_11_pwm_evt	3		IO	PWM or event for GP timer 11
		GPIO_57	4		IO	General-purpose IO 57
		Safe_mode	7			
195	X	Ether_rxn			AI	LAN9220: receive negative input
196	X	LANLED_spd			VO	LAN9220: LED1 speed indicator
197	X	Ether_rxp			AI	LAN9220: receive postive input
198	X	LANLED_link			VOD	LAN9220: LED2 link and activity indicator
199	X	GND		GND	GND	Ground
200	X	GND		GND	GND	Ground

7.1.1 Definitions

X=Pin on other chip than DM-3730

(1) This GPIO is only an input (and not an output).

(2) The usage of this GPIO is strongly restricted. For more information, see the General-Purpose Interface chapter of the AM/DM37x Multimedia Device Technical Reference Manual (literature number SPRUGN4).

(3) The usage of local bus signals are resticted

(4) The local bus address signals can be used as GPIO only if the ethernet PHY is not assembled

1. **MODE:** Multiplexing mode number.
    - Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the pin corresponds to the name of the pin. There is always a function mapped on the primary mode. Notice that primary mode is not necessarily the default mode.
      Note: The default mode is the mode at the release of the reset; also see the RESET REL. MODE column.
    - Modes 1 to 7 are possible modes for alternate functions. On each pin, some modes are effectively used for alternate functions, while some modes are not used and do not correspond to a functional configuration.
2. **TYPE:** Signal direction
    - I = Input
    - O = Output
    - I/O = Input/output
    - D = Open drain
    - DS = Differential
    - A = Analog
    - PWR = Power
    - GND = Ground

      Note: In the safe mode, the buffer is configured in high-impedance.

8 Signal Description

8.1 External Memory Interfaces – GPMC Signals Description

The General Purpose Memory Controller (GPMC) is used to interface external memory devices: such as NOR Flash, NAND Flash, Pseudo SRAM, SRAM or Field programmable Gate Array (FPGA)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
GPMC ALE	Address Valid or Address Latch Enable	O	182
GPMC CLE	Lower Byte Enable. Also used for Command Latch Enable	O	181
GPMC D0	GPMC data bit 0	IO	174
GPMC D1	GPMC data bit 1	IO	171
GPMC D2	GPMC data bit 2	IO	169
GPMC D3	GPMC data bit 3	IO	170
GPMC D4	GPMC data bit 4	IO	160
GPMC D5	GPMC data bit 5	IO	163
GPMC D6	GPMC data bit 6	IO	161
GPMC D7	GPMC data bit 7	IO	164
GPMC D8	GPMC data bit 8	IO	154
GPMC D9	GPMC data bit 9	IO	155
GPMC D10	GPMC data bit 10	IO	157
GPMC D11	GPMC data bit 11	IO	166
GPMC D12	GPMC data bit 12	IO	159
GPMC D13	GPMC data bit 13	IO	158
GPMC D14	GPMC data bit 14	IO	162
GPMC D15	GPMC data bit 15	IO	156
GPMC nOE	Output Enable	O	172
GPMC nWE	Write Enable	O	173
GPMC A1	GPMC output address bit 1	O	187
GPMC A2	GPMC output address bit 2	O	176
GPMC A3	GPMC output address bit 3	O	185
GPMC A4	GPMC output address bit 4	O	186
GPMC A5	GPMC output address bit 5	O	183
GPMC A6	GPMC output address bit 6	O	175
GPMC A7	GPMC output address bit 7	O	179
GPMC A8	GPMC output address bit 8	O	189
GPMC A9	GPMC output address bit 9	O	188
GPMC A10	GPMC output address bit 10	O	178
GPMC CLK	GPMC Clock	O	165
GPMC nCS4	GPMC Chip Select bit 4	O	192
GPMC nCS6	GPMC Chip Select bit 6	O	194
GPMC nCS7	GPMC Chip Select bit 7	O	184
GPMC WAIT3	External indication of wait	I	190

Note 1: GPMC nCS0 is connected to NAND IC on TDM-3730.
Note 2: GPMC nCS5 is connected to SMSC LAN9220 IC on TDM-3730.

8.2 Video Interfaces –CAM Signals description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Cam_hs	Camera Horizontal Synchronization	IO	145
Cam_vs	Camera Vertical Synchronization	IO	153
Cam_xclka	Camera Clock Output a	O	147
Cam_xclkb	Camera Clock Output b	O	143
Cam_d0	Camera digital image data bit 0	I	132
Cam_d1	Camera digital image data bit 1	I	134
Cam_d2	Camera digital image data bit 2	I	148
Cam_d3	Camera digital image data bit 3	I	152
Cam_d4	Camera digital image data bit 4	I	150
Cam_d5	Camera digital image data bit 5	I	151
Cam_d6	Camera digital image data bit 6	I	136
Cam_d7	Camera digital image data bit 7	I	138
Cam_d8	Camera digital image data bit 8	I	142
Cam_d9	Camera digital image data bit 9	I	140
Cam_d10	Camera digital image data bit 10	I	141
Cam_d11	Camera digital image data bit 11	I	137
Cam_fld	Camera field identification	IO	144
Cam_pclk	Camera pixel clock	I	146
Cam_wen	Camera Write Enable	I	149
Cam_strobe	Flash strobe control signal	O	139
Cam_IO	VBAT.RIGHT - VAUX2.OUT		38

The camera ISP can support the following features:

- **Image sensor:**
  - Interface with various image sensors:
    - R, G, B primary colors
    - Ye, Cy, Mg, G complementary colors
  - Support for electronic rolling shutter (ERS) and global-release reset shutters
- **CSI1/CCP2B serial interface:** The CSI1/CCP2B receiver is compatible with the SMIA CCP2 specification and the MIPI CSI1 specification.
- **Two MIPI CSI2 serial interfaces:** The camera ISP implements two MIPI CSI2 serial interface receivers (CSI2A and CSI2C). The CSI2 receivers enables data transfer at up to 2Gbps. It is based on the MIPI CSI2 Specification 1.0.
- **Parallel interface:** The camera parallel interface (CPI) supports two modes:
  - **SYNC mode:** In this mode, the image-sensor module provides horizontal and vertical synchronization signals to the parallel interface, along with the pixel clock. This mode works with 8-, 10-, 11-, and 12-bit data (if using CCDC inside the Video processing hardware above 10 bit data must be internally converted to 10 bit by the Bridge lane shifter). SYNC mode supports progressive and interlaced image-sensor modules.
  - **ITU mode:** In this mode, the image-sensor module provides an ITU-R BT 656-compatible data stream. The horizontal and vertical synchronization signals are not provided to the interface. Instead, the data stream embeds start-of-active

video (SAV) and end-of-active video (EAV) synchronization code. This mode works in 8- and 10-bit configurations

- **Video processing hardware:** The Video processing hardware removes the need for expensive camera modules to perform processing functions. It consists of parts: front end and back end:
  - **Video processing front end (VPFE)**
  - **Video processing back end (VPBE)**
- **Statistic collection modules (SCM):** The host CPU uses statistics to adjust various parameters for processing image data.
- **Central-resource shared buffer logic (SBL):** Buffers and schedules memory accesses requested by camera ISP modules
- **Circular buffer:** Prevents storage of full image frames in memory when data must be post-processed and/or preprocessed by software
- **Memory management unit (MMU):** Manages virtual-to-physical address translation for external addresses and solves the memory-fragmentation issue. Enables the camera driver to dynamically allocate and de-allocate memory; the MMU handles memory fragmentation.
- **Clock generator:** Generates two independent clocks that can be used by two external image sensors
- **Timing control:**
  - Generation clocks passed to the clock generator
  - Generation of signals for strobe flash, mechanical shutter, and global reset. Support for red-eye removal.
- **Open core protocol (OCP) compliant:**
  - One 64-bit master interface connected to L3
  - One 32-bit slave interface connected to L4
- Parallel Camera Interface (CPI)
  - **Video and Graphics Digitizer 1.8-V Mode: i**nput maximum frequency 148.5 MHz supported by the ISP module in 8-bit mode with 8 to 16 data bits conversion bridge enabled
  - **12-Bit SYNC Normal Progressive Mode:** input maximum frequency 75 MHz supported by the ISP module.
  - **8-Bit SYNC Packed Progressive Mode:** input maximum frequency 130 MHz supported by the ISP module.
  - **12-Bit SYNC Normal Interlaced Mode:** input maximum frequency 75 MHz supported by the ISP module
  - **8-Bit SYNC Packed Interlaced Mode:** input maximum frequency 130 MHz supported by the ISP module.
  - **ITU Mode:** input maximum frequency 75 MHz supported by the ISP module

8.3 Video Interfaces – DSS Signals Description

The Display Subsystem can support

- Color and monochrome displays up to 2048 x 2048 x 24-bpp resolution
- 256 x 24-bit entries palette in red, green, blue (RGB)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Dss_pclk	LCD Pixel Clock	O	109
Dss_hsync	LCD Horizontal Synchronization	O	123
Dss_vsync	LCD Vertical Synchronization	O	113
Dss_acbias	AC bias control (STN) or pixel data enable (TFT) output	O	100
Dss_data0	LCD Pixel Data bit 0	O	112
Dss_data1	LCD Pixel Data bit 1	O	118
Dss_data2	LCD Pixel Data bit 2	O	114
Dss_data3	LCD Pixel Data bit 3	O	116
Dss_data4	LCD Pixel data bit 4	O	106
Dss_data5	LCD Pixel Data bit 5	O	110
Dss_data6	LCD Pixel Data bit 6	O	119
Dss_data7	LCD Pixel Data bit 7	O	117
Dss_data8	LCD Pixel Data bit 8	O	115
Dss_data9	LCD Pixel Data bit 9	O	111
Dss_data10	LCD Pixel Data bit 10	O	102
Dss_data11	LCD Pixel Data bit 11	O	104
Dss_data12	LCD Pixel Data bit 12	O	108
Dss_data13	LCD Pixel Data bit 13	O	120
Dss_data14	LCD Pixel Data bit 14	O	122
Dss_data15	LCD Pixel Data bit 15	O	128
Dss_data16	LCD Pixel Data bit 16	O	101
Dss_data17	LCD Pixel Data bit 17	O	107
Dss_data18	LCD Pixel Data bit 18	O	105
Dss_data19	LCD Pixel Data bit 19	O	103
Dss_data20	LCD Pixel Data bit 20	O	121
Dss_data21	LCD Pixel Data bit 21	O	98
Dss_data22	LCD Pixel Data bit 22	O	126
Dss_data23	LCD Pixel Data bit 23	O	124
LCD_PON	LCD Enable	IO	64
LCD_ENVDD	LCD Voltage On	IO	66
LCD ENBKL	LCD Backlight Control	IO	30
LCD PWM	LCD Backlight on/off	IO	22

The TDM-3730 can easily be connected to a 18 or 24 bit TTL panel by following the following table.

DSS_D	24 bit	18 bit
Dss_data0	B0	
Dss_data1	B1	
Dss_data2	B2	B0
Dss_data3	B3	B1
Dss_data4	B4	B2
Dss_data5	B5	B3
Dss_data6	B6	B4
Dss_data7	B7	B5
Dss_data8	B0	
Dss_data9	G1	
Dss_data10	G2	G0
Dss_data11	G3	G1
Dss_data12	G4	G2
Dss_data13	G5	G3
Dss_data14	G6	G4
Dss_data15	G7	G5
Dss_data16	R0	
Dss_data17	R1	
Dss_data18	R2	R0
Dss_data19	R3	R1
Dss_data20	R4	R2
Dss_data21	R5	R3
Dss_data22	R6	R4
Dss_data23	R7	R5

8.4 Video Interfaces – TV Signals Description

The video encoder converts RGB video signals to conform to the NTSC/PAL standard analog video. The video encoder includes an integrated synchronization signal generator and two single channel video digital-to-analog converters (DACs) with video amplifiers, data manager, luma stage, chroma stage, modulator, and a control interface.

The output data to the TV set are the analog composite data from the video DAC stage. The following video standards are supported:

- NTSC-J, M
- PAL-B, D, G, H, I
- PAL-M

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Cvideo1_out	TV analog output Composite: cvideo1_out	AO	83
Cvideo2_out	TV analog output S-VIDEO: cvideo2_out	AO	85

8.5 Serial Communication Interfaces – I²C Signals Description

The device contains multimaster high-speed (HS) inter-integrated circuit (I2C) ™ controllers), each of which provides an interface between a local host (LH), such as the microprocessor unit (MPU) subsystem, and any I2C-bus-compatible device that connects through the I2C serial bus. External components attached to the I2C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I2C interface.
Each HS I2C controller can be configured to act like a slave or master I2C-compatible device.

INTER-INTEGRATED CIRCUIT INTERFACE (I2C2)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
I2C2_SCL	I2C Master Serial clock. Output is open drain	OD	78
I2C2_SDA	I2C Serial Bidirectional Data. Output is open drain.	IOD	76

Note: These signals have a 4.7kΩ pull up resistor to 1.8 V

INTER-INTEGRATED CIRCUIT INTERFACE (I2C3)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
I2C3_SCL	I2C Master Serial clock. Output is open drain	OD	75
I2C3_SDA	I2C Serial Bidirectional Data. Output is open drain.	IOD	73

Note: These signals have a 4.7kΩ pull up resistor to 1.8 V

8.6 Serial Communication Interfaces – McBSP LP Signals Description

The multichannel buffered serial port (McBSP) provides a full-duplex direct serial interface between the device and other devices in a system such as other application chips (digital base band), audio and voice codec, etc. Because of its high level of versatility, it can accommodate to a wide range of peripherals and clocked frame oriented protocols.

MULTICHANNEL BUFFERED SERIALPORT (McBSP LP 2)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Mcbsp2_dr	Received serial data	I	61
Mcbsp2_dx	Transmitted serial data	O	59
Mcbsp2_clkx	Combined serial clock	IO	55
Mcbsp2_fsx	Combined frame synchronization	IO	63

MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 3)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Mcbsp3_dr	Received serial data	I	49
Mcbsp3_dx	Transmitted serial data	O	53
Mcbsp3_clkx	Combined serial clock	IO	51
Mcbsp3_fsx	Combined frame synchronization	IO	47

8.7 Serial Communication Interfaces – McSPI Signals Description

The multichannel serial port interface (McSPI) is a master/slave synchronous serial bus. The McSPI modules differ as follows: SPI1 supports up to four peripherals, SPI3 supports up to two peripherals

The McSPI instances include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths ranging from 4 bits to 32 bits
- Up to four master channels or single channel in slave mode
- Master multichannel mode:
    - Full duplex/half duplex
    - Transmit-only/receive-only/transmit-and-receive modes
    - Flexible I/O port controls per channel
    - Two direct memory access (DMA) requests (read/write) per channel
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Support start-bit write command
- Support start-bit pause and break sequence
- 64 bytes built-in FIFO available for a single channel
- Force CS mode for continuous transfers

MULTICHANNEL SERIAL PORT INTERFACE (McSPI1)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Mcspi1_clk	SPI Clock	IO	41
Mcspi1_simo	Slave data in, master data out	IO	40
Mcspi1_somi	Slave data out, master data in	IO	43
Mcspi1_cs0	SPI Enable 0, polarity configured by software	IO	45

MULTICHANNEL SERIAL PORT INTERFACE (McSPI3)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Mcspi3_clk	SPI Clock	IO	82
Mcspi3_simo	Slave data in, master data out	IO	77
Mcspi3_somi	Slave data out, master data in	IO	80
Mcspi3_cs0	SPI Enable 0, polarity configured by software	IO	84
Mcspi3_cs1	SPI Enable 1, polarity configured by software	O	81

8.8 Serial Communication Interfaces – UARTs Signals Description

The module contains two universal asynchronous receiver/transmitter (UART) devices controlled by the microprocessor unit (MPU):

- UART1 is pinned out for use as UART devices only.
- UART3, which adds infrared communication support, is pinned out for use as a UART, infrared data association (IrDA), or consumer infrared (CIR) device, and can be programmed to any available operating mode.

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART1)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Uart1_cts	UART1 Clear To Send	I	86
Uart1_rts	UART1 Request To Send	O	87
Uart1_rx	UART1 Receive data	I	92
Uart1_tx	UART1 Transmit data	O	89

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART2)

Multiplex option instead of McBSP3 Signals

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Uart2_cts	UART2 Clear To Send	I	53
Uart2_rts	UART2 Request To Send	O	49
Uart2_rx	UART2 Receive data	I	47
Uart2_tx	UART2 Transmit data	O	51

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART3) / IrDA

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Uart3_cts_rctx	UART3 Clear To Send (input), Remote TX (output)	IO	135
Uart3_rts_sd	UART3 Request To Send, IR enable	O	131
Uart3_rx_irrx	UART3 Receive data, IR and Remote RX	I	129
Uart3_tx_irtx	UART3 Transmit data, IR TX	O	127

8.9 Serial Communication Interfaces – USB Signals Description

The USB Host is connected to the SMSC USB3320

The USB3320 is a highly integrated full featured Hi-Speed USB 2.0 transceiver based on MCSC's proven ULPI interface. The USB3320 provides an extremely flexible solution in a convenient 5 x 5 mm QFN package. It supports a wide variety of different reference clock frequencies with one single part, as well as accepting clocking from crystal/resonators and the ULPI 60 MHz Clock-In mode. As with previous generations of SMSC's USB transceivers, the USB3320 integrates a USB switch and both ESD and VBUS over-voltage protection devices.

Note1: USB 1.1 devices can be connected to the USB 2.0 host port only through a USB 2.0 hub.

Note2: Single USB 1.1 devices can be connected directly to the USB OTG port. This port should however during boot up always be kept in OTG mode.

Note3: It's not advisable to connect a hub to the USB OTG port.

Note4: ESD decoupling circuits are advised on all USB devices and ports.

USB Host

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
IDM0	D – pin of the USB cable	IO A	35
IDP0	D + pin of the USB cable	IOA	37
RESETB	When low, the part is suspended with all ULPI outputs tri-stated. When high, the USB3320 will operate as a normal ULPI device		16

The USB OTG is connected to the TPS65930 USB Transceiver

The TPS65930 device includes a USB OTG transceiver that supports USB 480 Mbps HS, 12 Mbps full-speed (FS), and USB 1.5 Mbps low-speed (LS) through a 4-pin ULPI.

The device has a USB OTG transceiver that allows system implementation that complies with the following specifications:

- Universal Serial Bus 2.0 Specification
- On-The-Go Supplement to the USB 2.0 Specification
- UTMI+ Low Pin Interface Specification

USB OTG

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
HSUSB_DN	USB data N/USB carkit transmit data	IO	32
HSUSB_DP	USB data P/USB carkit receive data	IO	34
HSUSB_ID	USB ID	IO	21
VBUS_5V0	Power	PWR	1

Note: It is advised to use USB OTG only for USB OTG

8.10 Removable Media Interfaces – MMC/ SDIO Signals

The multimedia card high-speed/SD/SD I/O (MMC/SD/SDIO) host controller provides an interface between a local host (LH) such as a microprocessor unit (MPU) or digital signal processor (DSP) and either MMC, SD memory cards, or SDIO cards and handles MMC/SD/SDIO transactions with minimal LH intervention.
The application interface manages transaction semantics. The MMC/SD/SDIO host controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRC), start/end bit, and checking for syntactical correctness.
The application interface can send every MMC/SD/SDIO command and either poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to warn of end of operation.
The application interface can read card responses or flag registers. It can also mask individual interrupt sources. All these operations can be performed by reading and writing control registers. The MMC/SD/SDIO host controller also supports two DMA channels.

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
MMC1 CD	Card Detection1	IO	20
MMC1 CLK0	MMC/SD Output Clock	O	95
MMC1 CMD	MMC/SD command signal	IO	99
MMC1 DAT0	MMC/SD Card Data bit 0 / SPI Serial Input	IO	97
MMC1 DAT1	MMC/SD Card Data bit 1	IO	96
MMC1 DAT2	MMC/SD Card Data bit 2	IO	94
MMC1 DAT3	MMC/SD Card Data bit 3	IO	93
MMC1 WP	MMC Write Protect	IO	88
VMMC1	Power 1V8/ 3V3	O	39

8.11 General Purpose IOs Signals Description

By using Multiplexing a maximum of **125 pins** on the module can be turned into GPIOs. By default the following GPIOs are already acting as GPIO as first function and do not need any software configuration.

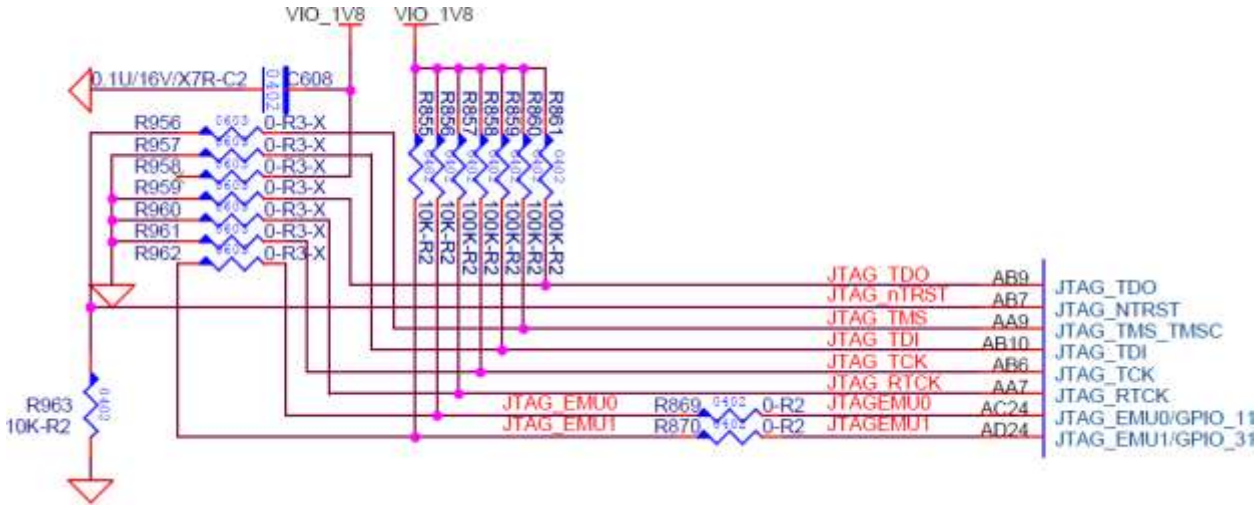
SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
GPIO 12	General-purpose IO 12	IO	68
GPIO 13	General-purpose IO 13	IO	72
GPIO 18	General-purpose IO 18	IO	74
GPIO 19	General-purpose IO 19	IO	69
GPIO 20	General-purpose IO 20	IO	90
GPIO_137	General-purpose IO 137	IO	65

GPIOs Signals Description

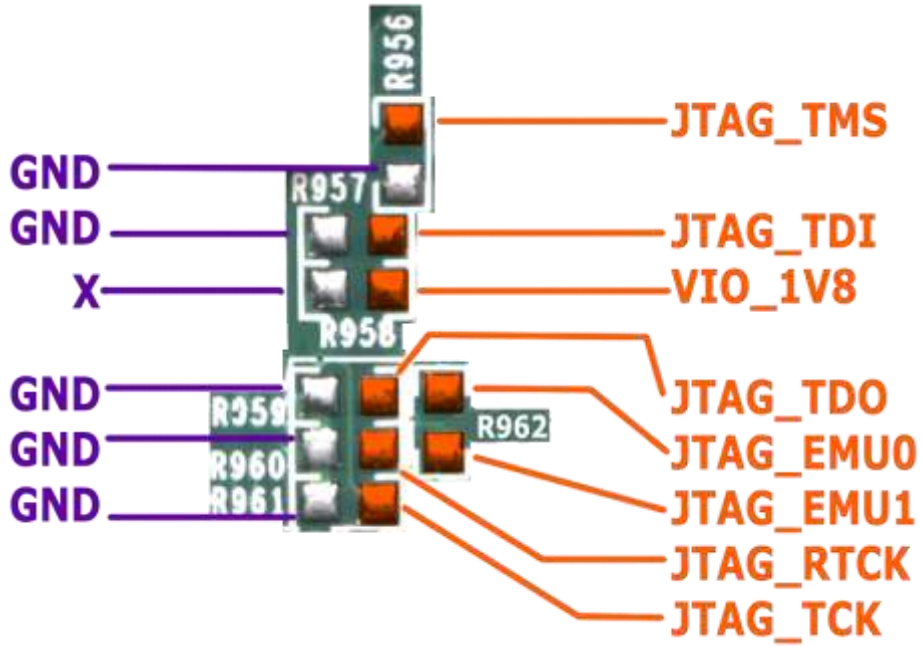
SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
DVI_nDISABLE	DVI/ Backlight control	IO	28
HOST nOC	HOST nOC	IO	15

8.12 Test Interfaces – JTAG Signals Description

The target debug interface of the device uses the five standard IEEE 1149.1 (JTAG) signals (nTRST, TCK, TMS, TDI, and TDO), a return clock (RTCK) to meet the clocking requirements of the ARM968 processor, and two instrumentations pins (EMU0, EMU1).



Schematic of the JTAG signals



See Photo for the location of the solder pads. Solder at the orange pads

SIGNAL NAME	DESCRIPTION	TYPE
Jtag_ntrst	Test reset	I
Jtag_tck	Test Clock	I
Jtag_rtck	ARM Clock emulation	O
Jtag_tms_tmsc	Test Mode Select	IO
Jtag_tdi	Test Data Input	I
Jtag_tfo	Test data Output	O
Jtag_emu0	Test emulation 0	IO
Jtag_emu1	Test emulation 1	IO

8.13 Power Supplies Signals description

Power Supply Signals

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
DC 5V	Power 5V	I	2
DC 5V	Power 5V	I	4
DC 5V	Power 5V	I	6
DC 5V	Power 5V	I	8
DC 5V	Power 5V	I	10
DC 5V	Power 5V	I	12
VBUS_5V	Power 5V	I	1
VIO_1V8	Power 1V8	O	27
VIO_1V8	Power 1V8	O	29
VIO_1V8	Power 1V8	O	31
VIO_1V8	Power 1V8	O	33
VMMC1	Power 1V8/ 3V3	O	39

Note1: All input 5V signals should be connected to the main 5V input power circuit. There is an acceptable tollerance of +/-5%.

Note2: The output 3V3 signals current is limited and therefore it's advisable to generate 3V3 voltage on the baseboard for optimal operation.

Ground Signals

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
GND	Power Ground	GND	3
GND	Power Ground	GND	19
GND	Power Ground	GND	79
GND	Power Ground	GND	125
GND	Power Ground	GND	167
GND	Power Ground	GND	177
GND	Power Ground	GND	199
GND	Power Ground	GND	70
GND	Power Ground	GND	130
GND	Power Ground	GND	168
GND	Power Ground	GND	180
GND	Power Ground	GND	200

Note 1: All GND pins must be connected and should not remain not connected .
Note 2: On a custom baseboard. Please connect GND signals to the mounting pose/nuts which are used to lock the module to the baseboard.

8.14 System and Miscellaneous Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
SYS_CLKOUT1	Configurable Output Clock 1	O	71
SYS_nRESPWRON	Power On Reset	I	14
SYSEN	System enable output	D	17

SYS_nRESPWRON will reset the module when pulled low, it will reset DM-3730, TPS65930, LAN controller, USB PHYand WiFi simultaneously.

8.15 Touch Interupt Signal Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
TS_nPEN_IRQ	Touch Interrupt	IO	67

8.16 Serial Communcication Interfaces – HDQ/ 1-Wire Signals Description

The HDQ/1-Wire module implements the hardware protocol of the master functions of the Benchmarq HDQ and the Dallas Semiconductor 1-Wire® protocols. These protocols use a single wire for communication between the master (HDQ/1-Wire controller) and the slaves (HDQ/1-Wire external compliant devices).

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Hdq_SIO	Bidirectional HDQ 1-Wire control and data Interface. Output is open drain.	IOD	133

8.17 PWM Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
PWR_ON	Input; detect a control command to start or stop the system	I	13

PWM Option on the TPS65930 instead of DVI_nDISABLE & LCD ENBKL

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
PWM1	Pulse width driver	O	28
PWM0	Pulse width driver 0	O	30

8.18 ADC Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
ADCIN2	General –purpose ADC Input	I	36
CHRG STATE	Battery type	IO	26

8.19 Analog Audio Signals Description

ANA.MIC Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
Mic_main_M	Main microphone left input (M)	I	23
Mic_main_P	Main microphone left input (P)	I	11

VMIC BIAS Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
MIC_BIAS	Analog microphone bias 1	PWR	25
MICBIAS_G	Dedicated ground for microphones	GND	9

Headset Signals description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
PreDriv.LEFT	Predriver output left P for external class-D amplifier	O	7
PreDriv.RIGHT	Predriver output right P for external class-D amplifier	O	5

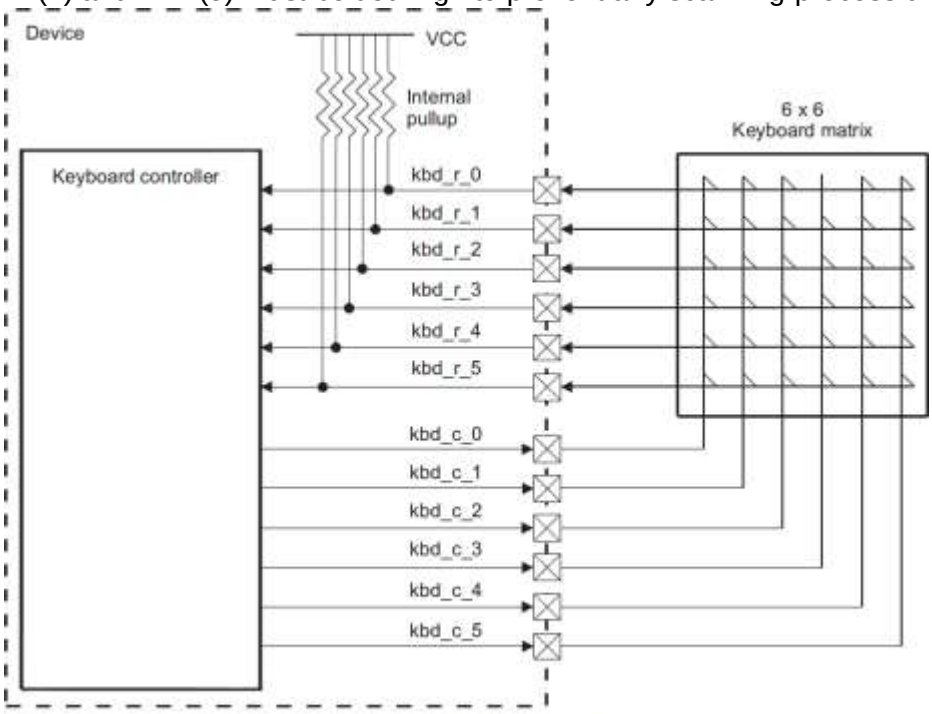
AUX input Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
AUXR	Auxiliary audio input right	I	24

8.20 Keypad Signals Description

The TDM-3730 supports a keypad interface up to a matrix of 6 x 6

When a key button of the keyboard matrix is pressed, the corresponding row and column lines are shorted together. To allow key press detection, all input pins (KBR) are pulled up to VCC and all output pins (KBC) are driven to a low level.
Any action on a button generates an interrupt to the sequencer.
The decoding sequence is written to allow detection of simultaneous press actions on several key buttons.
The keyboard interface can be used with a smaller keyboard area than 6 × 6. To use a 3 × 3 keyboard, KBR(4) and KBR(5) must be tied high to prevent any scanning process distribution.



Keyboard Connection

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
KPD.C0	Keypad column 0	D	50
KPD.C1	Keypad column 1	D	48
KPD.C2	Keypad column 2	D	46
KPD.C3	Keypad column 3	D	44
KPD.C4	Keypad column 4	D	42
KPD.C5	Keypad column 5	D	91
KPD.R0	Keypad row 0	I	60
KPD.R1	Keypad row 1	I	58
KPD.R2	Keypad row 2	I	56
KPD.R3	Keypad row 3	I	54
KPD.R4	Keypad row 4	I	52
KPD.R5	Keypad row 5	I	62

8.21 Ethernet Signals Description

TDM-3730 contains a SMSC LAN9220 Single chip Ethernet controller with the following features:

- Fully compliant with IEEE 802.3/802.3u standards
- Integrated Ethernet MAC and PHY
- 10BASE-T and 100BASE-TX support
- Full- and Half-duplex support
- Full-duplex flow control
- Backpressure for half-duplex flow control
- Preamble generation and removal
- Automatic 32-bit CRC generation and checking
- Automatic payload padding and pad removal
- Loop-back modes

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
ETHER_RXN	Receive Negative Input (normal)	AI	195
ETHER_RXP	Receive Positive Input (normal)	AI	197
ETHER_TXN	Transmit Negative Output (normal)	AO	191
ETHER_TXP	Transmit Positive Output (normal)	AO	193
LANLED_LINK	Link and Activity Indicator	O	198
LANLED_SPD	Speed Indicator	D	196

8.22 LED Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
LEDA	User definable LED Indicator	D	18

The TDM-3730 System on Module contains 5 onboard LEDs with following functions:

LED NAME	DESCRIPTION
LED1	Power ON
LED2	Power: System works
LED3	WiFi: Active
LED4	LAN: Active
LED5	Power ON

8.23 Pull-up or Pull-down Signals Description

Pin #	Signal Name	Mode	Voltage	Resistor	Pull up/down
73	I2C3_sda	0	1.8	4.7kΩ	Up
	GPIO_185	4			
	Safe mode	7			
75	I2C3 SCL	0	1.8	4.7kΩ	Up
	GPIO_184	4			
	safemode	7			
76	I2C2 SDA	0	1.8	4.7kΩ	Up
	GPIO_183	4			
	Safe_mode	7			
78	I2C2 SCL	0	1.8	4.7kΩ	Up
	GPIO_168	4			
	Safe_mode	7			

8.24 Boot Option

SIGNAL NAME	DESCRIPTION	TYPE	PIN TDM-3730
SYS_BOOT0	1		
SYS_BOOT1	1		
SYS_BOOT2	1		
SYS_BOOT3	1		
SYS_BOOT4	0		
SYS_BOOT5	Boot configuration mode bit 5	I	57
SYS_BOOT6	1		

9 Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
MMC Interface 3.0-V Mode					
V_{IH}	High-level input voltage	1.875		3.3	V
V_{IL}	Low-level input voltage	-0.3		0.75	V
V_{OH}	High-level output voltage with 100-µA sink current IOH	2.25			V
V_{OL}	Low-level output voltage with 100-µA source current at vdds_mmc1 minimum			0.375	V

PARAMETER		MIN	NOM	MAX	UNIT
GPIO 1.8-V Mode					
V_{IH}	High-level input voltage	1.26		2.1	V
V_{IL}	Low-level input voltage	-0.3		0.36	V
V_{OH}	High-level output voltage with 100-µA sink current IOH	1.44		2.1	V
V_{OL}	Low-level output voltage with 100-µA source current at vdds_mmc1 minimum	-0.3		0.4	V

PARAMETER			MIN	NOM	MAX	UNIT
Recommended Operating Conditions						
Vdds	Supply voltage for 1.8-V I/O macros		1.71	1.8	1.91	V
Vdds_mem	Supply voltage for memory buffers		1.71	1.8	1.91	V
Vdds_mmc1	Supply voltage range for mmc1 dual voltage IOs	1.8-V mode	1.71	1.8	1.91	V
		3.0-V mode	2.70	3.00 to 3.30	3.60	
Vdds_x	Supply voltage range for x dual voltage IOs	1.8-V mode	1.71	1.8	1.91	V
		3.0-V mode	2.70	3.00	3.60	
Vdda_dac	Analog supply voltage for Video DAC		1.71	1.8	1.91	V

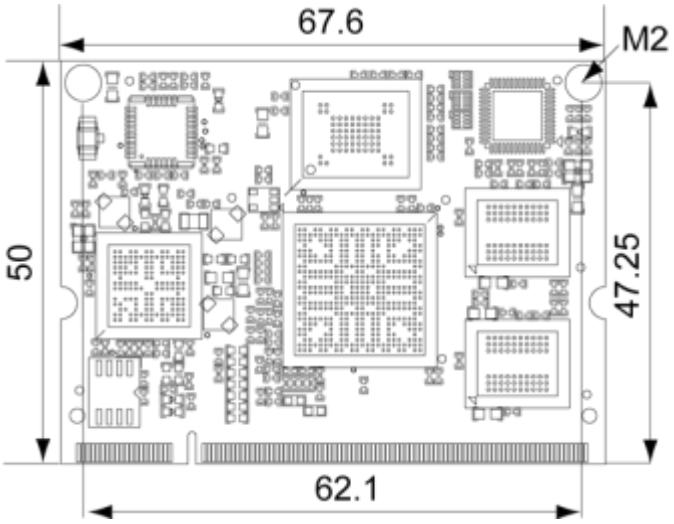
The Supply Voltage to the module is 5V ±5%

10 Environmental Specifications

Temperature	Commercial: 0° to 70° C
	Extended: -20° to 70° C (no WiFi)
	Industrial: -40° to 85° C (no WiFi)
Humidity	10-90%
Dimensions	67.6x 50x 3.4 mm (2⅝x 2x ¼ inch)
MTBF	>100,000 hours
Weight	12 grams
Shock	50G / 25ms
Vibration	20G / 0-600 Hz

11 Mechanical Dimensions

11.1 TDM-3730 System on Module Dimensions



Dimensions in mm

Note: 2D (DXF) and 3D(STEP) files are available for download at the Technexion website. (Service and support/ Downloads/ ARM CPU Modules/ TDM-3730)

12 Module Connection

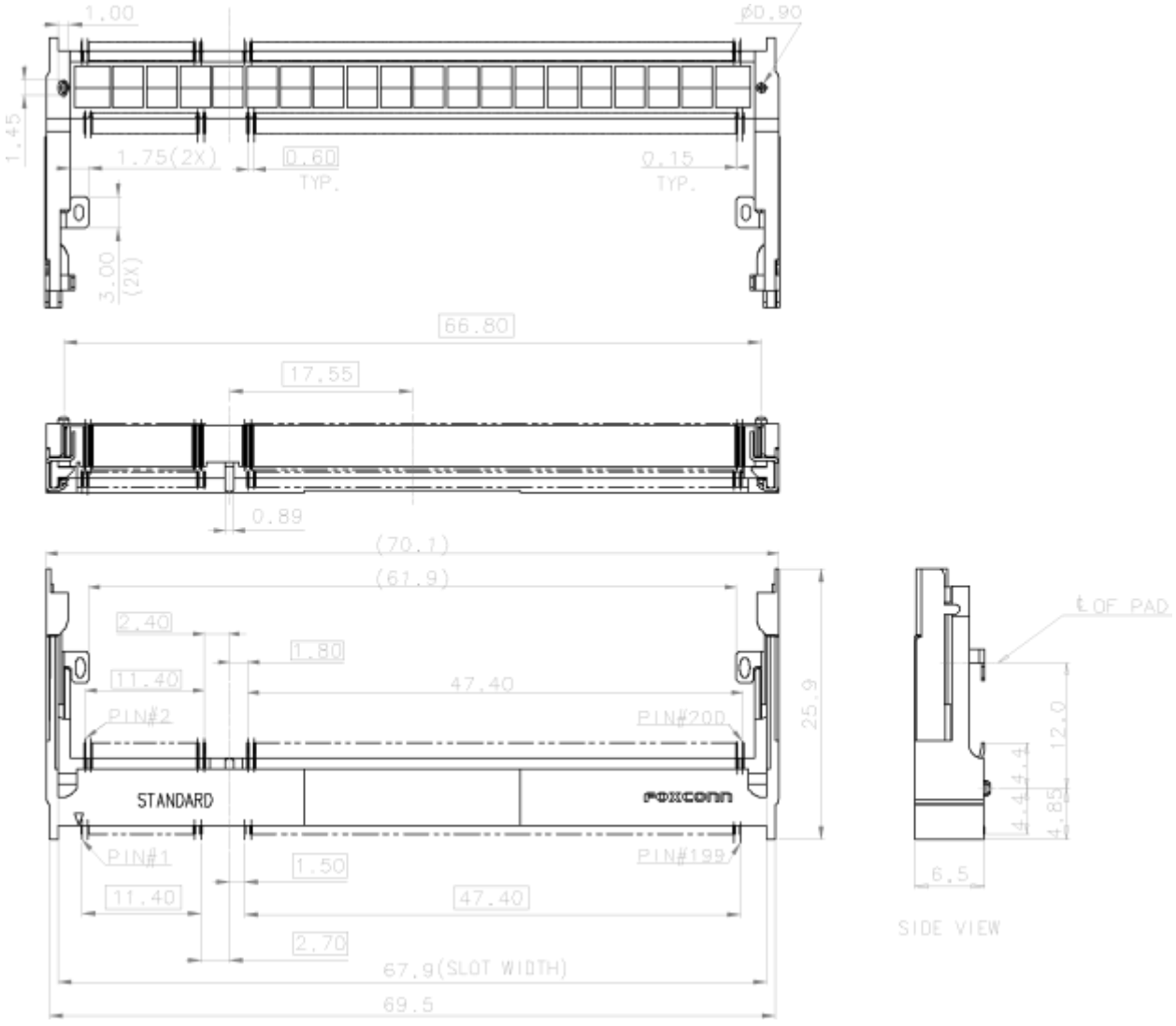
12.1 Module Connector DDR2 SO-DIMM

To mount the TDM-3730 module on the baseboard it isrecommended to use a connector with the following specifications:

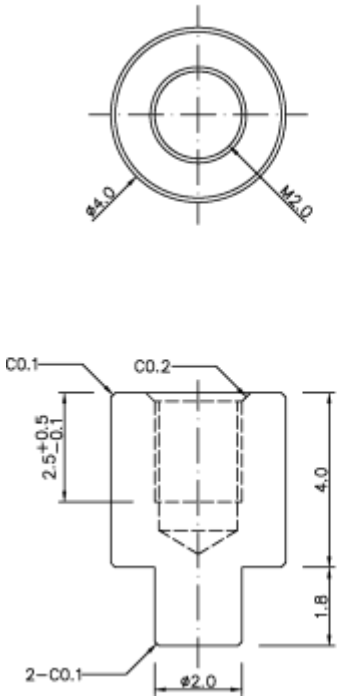
- DDR II SO-DIMM 200pin SMT
- Standard
- height 6.5 mm

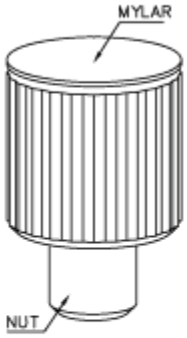
For example Foxconn AS0A426-N6SN-4F or Tyco 5-1746530-4

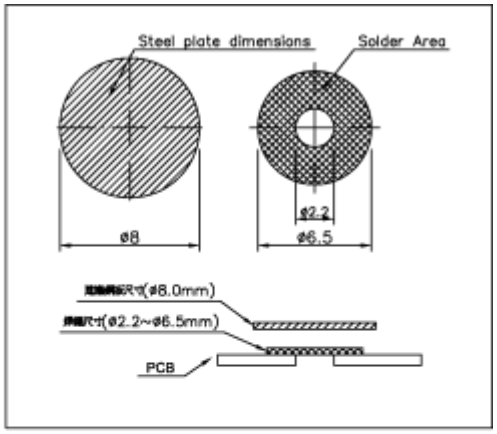
If you have difficulty purchasing these parts please contact sales@technexion.com, for assistance.



12.2 Nut to Fix TDM-3730 Module to the Baseboard







PCB Recommend Layout Pattern

Note 1: Always design the above mounting nut/pose on your custom baseboard and fasten the TDM-3730 to ensure a solid connection and counter vibration prone applications.

Note 2: On a custom baseboard always connect the mounting nut/pose to the baseboard general system GND section.

If you have difficulty purchasing these parts please contact sales@technexion.com, for assistance.

13 Disclaimer

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14 Warranty

TechNexion hardware products are warranted against defects in materials and workmanship. If TechNexion receives notice of such defects during the warranty period, TechNexion shall, at its option, either repair or replace hardware products that prove to be defective.

1. **Warranty Period**

   The warranty period shall commence on the invoice date. For TechNexion equipment the standard warranty period shall be two-year parts and labor.

2. **Warranty Coverage**

   2.1 This warranty does not apply to any Products that have been repaired or altered by other than TechNexion authorized service person or, which have been subjected to misuse, abuse, accident, or improper installation. TechNexion assumes no liability as a consequence of such events under the terms of this warranty.

   2.2 This warranty does not cover the damage due to the shipping of the Products and external causes, including accident, abuse, misuse or problems with electrical power, usage not in accordance with product instruction, and problems caused by use of parts and components not supplied by TechNexion upon request.

   2.3 This warranty does not cover any items that are in one or more of the following categories:

   a. Software and/or device drivers,
   b. External devices,
   c. Accessories or parts added to Products after the Products shipped from TechNexion and, Accessories, or parts that are not assembled in TechNexion facilities.
   d. All warranty is voided if the TechNexion warranty label or serial number is removed, illegible, or missing

15 Contact Information

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