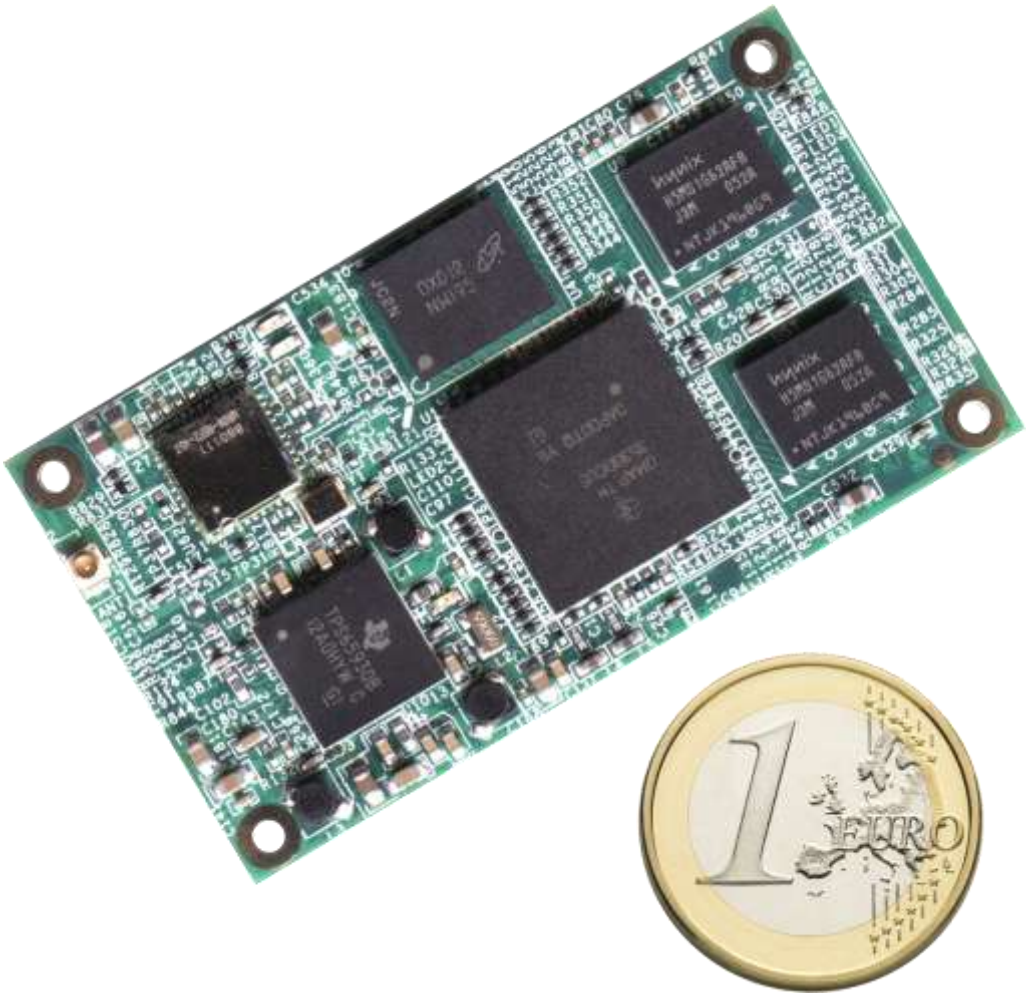
TechNexion

March 6th 2012



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TAO-3530 System on Module

TAO-3530 HARDWARE MANUAL rev C | TechNexion

TechNexion

TAO-3530

TDM-3530 System on Module

Hardware Manual

Rev C

1 Contents

2 Revision

Revision	Date	Description	Created by
0.90	14/07/2011	Preliminary Version	TechNexion
C	19/07/2011	First Public Version	TechNexion
C-01	11/08/2011	Change Wi-Fi signals description	TechNexion
C-02	20/09/2011	Change 24-18bit table	TechNexion
c-03	06/03/2012	Add Chapter about multiplexing in software	TechNexion

3 Care and Maintenance

3.1 General

Your device is a product of superior design and craftsmanship and should be treated with care. The following suggestions will help you.

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

These suggestions apply equally to your device, battery, charger, or any enhancement. If any device is not working properly, take it to the nearest authorized service facility for service.

3.2 Regulatory Information

Disposal of Waste Equipment by Users in Private Household in the European Union

This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service or the shop where you purchased the product.

We hereby declare that the product is in compliance with the essential requirements and other relevant provisions of European Directive 1999/5/EC (radio equipment and telecommunications terminal equipment Directive).

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The Compliance of RoHS New Requirement

According to the new requirements in directive 2002/95/EC, DecaBDE is added with specification starting by July 1, 2008 as follows:

Cadmium (Cd)	: Under 100ppm
Lead (Pb)	: Under 1000ppm
Mercury (Hg)	: Under 1000ppm
Hexavalent Chromium (Cr6)	: Under 1000ppm
PBB	: Under 1000ppm
PBDE (include DecaBDE)	: Under 1000ppm

Please confirm and send back, thanks.

RoHS Compliance Statement

We aware the change in this directive and our product can meet this new specification as above.

Company Stamp

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Federal Communications Commission (FCC) Unintentional emitter per FCC Part 15

This device has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio or television reception. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio and television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

■ Reorient or relocate the receiving antenna

■ Increase the separation between the equipment and receiver

■ Connect the equipment to an outlet on a different circuit from that to which the receiver is connected

■ Consult the dealer or an experienced radio/TV technician for help.

WARNING! To reduce the possibility of heat-related injuries or of overheating the computer, do not place the computer directly on your lap or obstruct the computer air vents. Use the computer only on a hard, flat surface. Do not allow another hard surface, such as an adjoining optional printer, or a soft surface, such as pillows or rugs or clothing, to block airflow. Also, do not allow the AC adapter to contact the skin or a soft surface, such as pillows or rugs or clothing, during operation. The computer and the AC adapter comply with the user-accessible surface temperature limits defined by the International Standard for Safety of Information Technology Equipment (IEC 60950).

4 Description

The OMAP35x family of high-performance, applications processors are based on the enhanced OMAP™3 architecture and are integrated on TI's advanced 65-nm process technology.

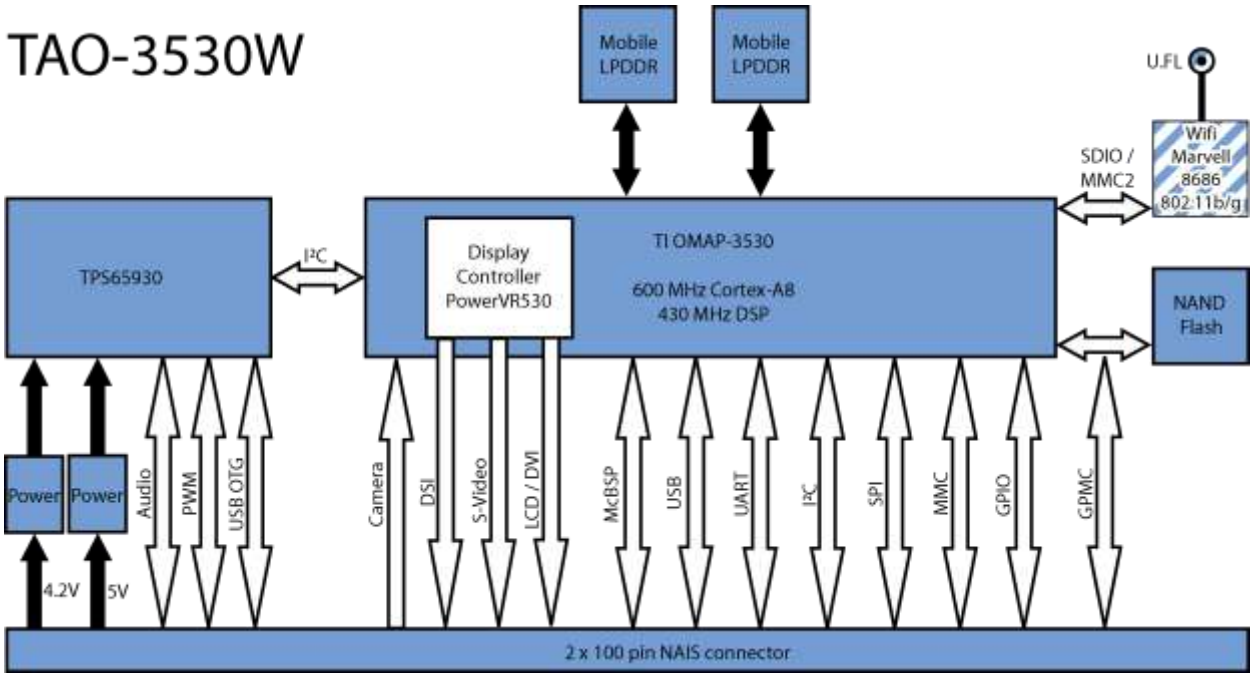
The architecture is designed to provide best-in-class video, image, and graphics processing sufficient to support the following:
• Streaming video
• 2D/3D mobile gaming
• Video conferencing
• High-resolution still image

The architecture of OMAP35xx is designed to provide maximum flexibility in a wide range of end applications including but not limited to:
• Portable Data Terminals
• Navigation
• Auto Infotainment
• Gaming
• Medical imaging
• Home Automation
• Human Interface
• Industrial Control
• Test and Measurement
• Single board Computers

The device can support numerous HLOS and RTOS solutions including Linux, Android and Windows Embedded CE by TechNexion and/ or third parties.

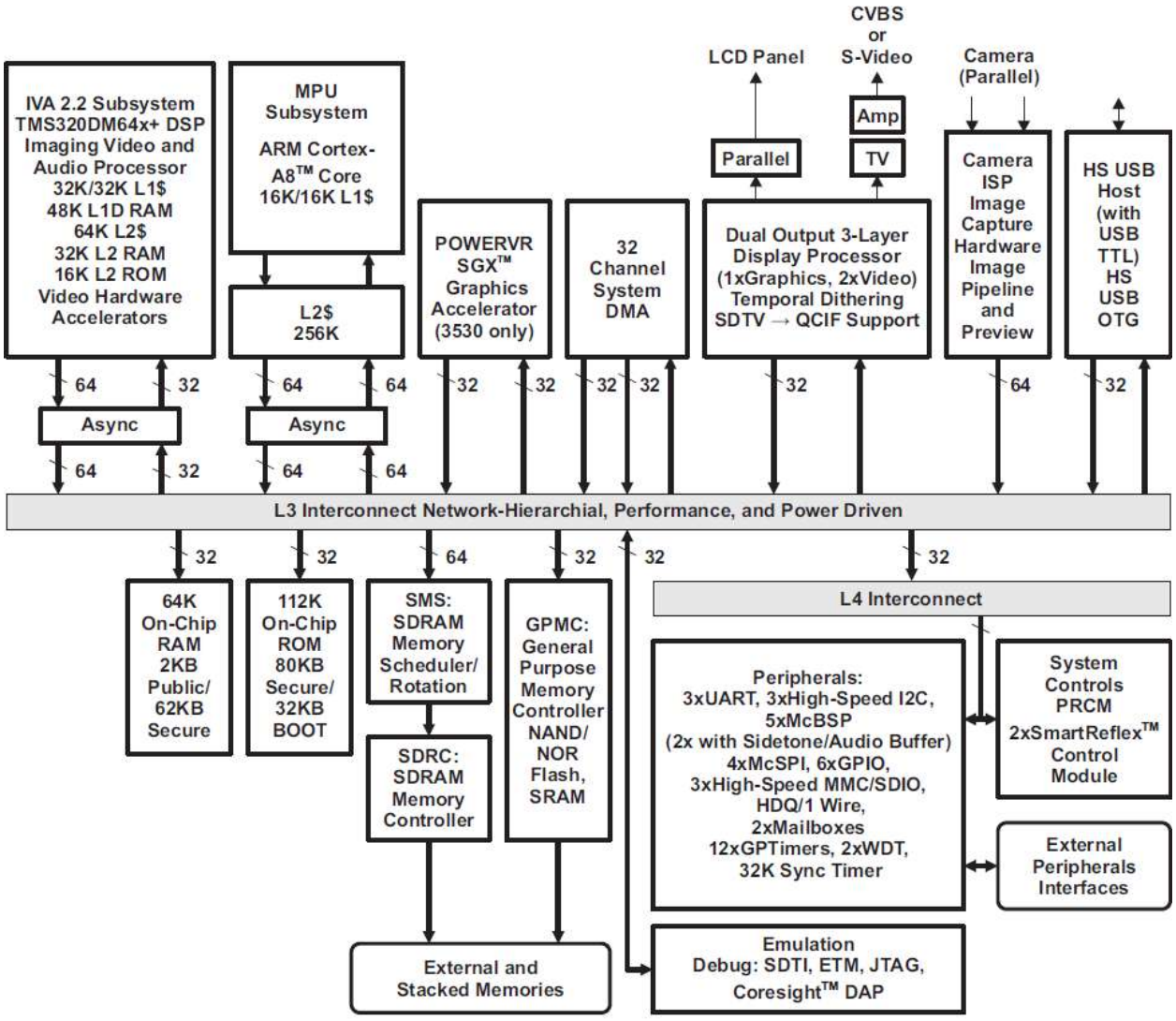
One can always check our website (www.technexion.com) for additional product detail information, mechanical design files, software programming guides, source code software and custom baseboard creation guideline.

4.1 Block Diagram TAO-3530 System on Module



4.2 Functional Block Diagram CPU

The functional block diagram of the OMAP3530 Applications Processor is shown below.



OMAP3530 Functional Block Diagram

5 System Components

5.1 CPU: OMAP-3530

5.1.1 OMAP-3530 Applications Processor Features

OMAP3530 Applications Processor:

- OMAP™ 3 Architecture
- MPU Subsystem
  - Up to 720-MHz ARM Cortex™-A8 Core
  - NEON™ SIMD Coprocessor
- High Performance Image, Video, Audio (IVA2.2™) Accelerator Subsystem
  - Up to 520-MHz TMS320C64x+™ DSP Core
  - Enhanced Direct Memory Access (EDMA) Controller (128 Independent Channels)
  - Video Hardware Accelerators
- POWERVR SGX™ Graphics Accelerator
  - Tile Based Architecture Delivering up to 10 MPoly/sec
  - Universal Scalable Shader Engine: Multi-threaded Engine Incorporating Pixel and Vertex Shader Functionality
  - Industry Standard API Support: OpenGLES 1.1 and 2.0, OpenVG1.0
  - Fine Grained Task Switching, Load Balancing, and Power Management
  - Programmable High Quality Image Anti-Aliasing
- Fully Software-Compatible With C64x and ARM9™
- Commercial and Extended Temperature Grades

Advanced Very-Long-Instruction-Word (VLIW) TMS320C64x+™ DSP Core

- Eight Highly Independent Functional Units
  - +Six ALUs (32-/40-Bit), Each Supports Single 32-Bit, Dual 16-Bit, or Quad 8-Bit Arithmetic per Clock Cycle
  - Two Multipliers Support Four 16 x 16-Bit Multiplies (32-Bit Results) per Clock Cycle or Eight 8 x 8-Bit Multiplies (16-Bit Results) per Clock Cycle
- Load-Store Architecture With Non-Aligned Support
- 64 32-Bit General-Purpose Registers
- Instruction Packing Reduces Code Size
- All Instructions Conditional
- Additional C64x+™ Enhancements
  - Protected Mode Operation
  - Exceptions Support for Error Detection and Program Redirection
  - Hardware Support for Modulo Loop Operation

C64x+ L1/L2 Memory Architecture

- 32K-Byte L1P Program RAM/Cache (Direct Mapped)
- 80K-Byte L1D Data RAM/Cache (2-Way Set-Associative)
- 64K-Byte L2 Unified Mapped RAM/Cache (4-Way Set-Associative)
- 32K-Byte L2 Shared SRAM and 16K-Byte L2 ROM

C64x+ Instruction Set Features

- Byte-Addressable (8-/16-/32-/64-Bit Data)
- 8-Bit Overflow Protection
- Bit-Field Extract, Set, Clear
- Normalization, Saturation. Bit-Counting
- Compact 16-Bit Instructions
- Additional Instructions to Support Complex Multiplies

ARM Cortex™-A8 Core

- ARMv7 Architecture
  - Trust Zone®
  - Thumb®-2
  - MMU Enhancements
- In-Order, Dual-Issue, Superscalar Microprocessor Core
- NEON™ Multimedia Architecture
- Over 2x Performance of ARMv6 SIMD
- Supports Both Integer and Floating Point SIMD
- Jazelle® RCT Execution Environment Architecture
- Dynamic Branch Prediction with Branch Target Address Cache, Global History Buffer, and 8-Entry Return Stack
- Embedded Trace Macrocell (ETM) Support for Non-Invasive Debug

ARM Cortex™-A8 Memory Architecture:

- 16K-Byte Instruction Cache (4-Way Set-Associative)
- 16K-Byte Data Cache (4-Way Set-Associative)
- 256K-Byte L2 Cache

112K-Byte ROM

64K-Byte Shared SRAM

Endianess:

- ARM Instructions - Little Endian
- ARM Data – Configurable
- DSP Instruction/Data - Little Endian

External Memory Interfaces:

- SDRAM Controller (SDRC)
  - 16, 32-bit Memory Controller With 1G-Byte Total Address Space
  - Interfaces to Low-Power Double Data Rate (LPDDR) SDRAM
  - SDRAM Memory Scheduler (SMS) and Rotation Engine
- General Purpose Memory Controller (GPMC)
  - 16-bit Wide Multiplexed Address/Data Bus
  - Up to 8 Chip Select Pins With 128M-Byte Address Space per Chip Select Pin

  - Glueless Interface to NOR Flash, NAND Flash (With ECC Hamming Code Calculation), SRAM and Pseudo-SRAM
  - Flexible Asynchronous Protocol Control for Interface to Custom Logic (FPGA, CPLD, ASICs, etc.)
  - Nonmultiplexed Address/Data Mode (Limited 2K-Byte Address Space)

System Direct Memory Access (sDMA) Controller (32 Logical Channels With configurable Priority)

Camera Image Signal Processing (ISP)

- CCD and CMOS Imager Interface
- Memory Data Input
- RAW Data Interface
- BT.601/BT.656 Digital YCbCr 4:2:2 (8-/10-Bit) Interface
- Law Compression and Decompression
- Preview Engine for Real-Time Image Processing
- Glueless Interface to Common Video Decoders
- Histogram Module/Auto-Exposure, Auto-White Balance, and Auto-Focus Engine
- Resize Engine
  - Resize Images From 1/4x to 4x
  - Separate Horizontal/Vertical Control

Display Subsystem

- Parallel Digital Output
  - Up to 24-Bit RGB
  - HD Maximum Resolution
  - Supports Up to 2 LCD Panels
  - Support for Remote Frame Buffer Interface (RFBI) LCD Panels
- 2 10-Bit Digital-to-Analog Converters (DACs) Supporting:
  - Composite NTSC/PAL Video
  - Luma/Chroma Separate Video (S-Video)
- Rotation 90-, 180-, and 270-degrees
- Resize Images From 1/4x to 8x
- Color Space Converter
- 8-bit Alpha Blending

Serial Communication

- Multichannel Buffered Serial Ports (McBSPs)
  - 512 Byte Transmit/Receive Buffer (McBSP3)
  - SIDETONE Core Support (McBSP2 and 3 Only) For Filter, Gain, and Mix Operations
  - Direct Interface to I2S and PCM Device and TDM Buses
  - 128 Channel Transmit/Receive Mode
- Master/Slave Multichannel Serial Port Interface (McSPI) Ports
- High-Speed/Full-Speed/Low-Speed USB OTG Subsystem (12-/8-Pin ULPI Interface)
- High-Speed/Full-Speed/Low-Speed Multiport USB Host Subsystem

    - 12-/8-Pin ULPI Interface or 6-/4-/3-Pin Serial Interface
    - Supports Transceiverless Link Logic (TLL)
- One HDQ/1-Wire Interface
- UARTs (One with Infrared Data Association [IrDA] and Consumer Infrared [CIR] Modes)
- Master/Slave High-Speed Inter-Integrated Circuit (I2C) Controllers

Removable Media Interfaces:

- Multimedia Card (MMC)/ Secure Digital (SD) With Secure Data I/O (SDIO)

Comprehensive Power, Reset, and Clock Management

- SmartReflex™ Technology
- Dynamic Voltage and Frequency Scaling (DVFS)

Test Interfaces

- IEEE-1149.1 (JTAG) Boundary-Scan Compatible
- Embedded Trace Macro Interface (ETM)
- Serial Data Transport Interface (SDTI)

12 32-bit General Purpose Timers

2 32-bit Watchdog Timers

1 32-bit 32-kHz Sync Timer

Up to 139 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions)

65-nm CMOS Technology

Discrete Memory Interface

Package

- 423-pin s-PBGA package (CUS Suffix), .65mm Ball Pitch

5.2 PMIC: TPS-65930

5.2.1 TPS-65930 – Introduction

The TPS65930 devices are power-management ICs for OMAP™ and other mobile applications. The devices include power-management, a universal serial bus (USB) high-speed (HS) transceiver, light -emitting diode (LED) drivers, an analog-to-digital converter (ADC), a real-time clock (RTC), and embedded power control (EPC). In addition, the TPS65930 includes a full audio codec with two digital-to-analog converters (DACs) and two ADCs to implement dual voice channels, and a stereo downlink channel that can play all standard audio sample rates through a multiple format inter-integrated sound (I2S™)/time division multiplexing (TDM) interface.

These optimized devices support the power and peripheral requirements of the OMAP application processors. The power portion of the devices contains three buck converters, two controllable by a dedicated SmartReflex™ class-3 interface, multiple low dropout (LDO) regulators, an EPC to manage the power sequencing requirements of OMAP, and an RTC and backup module. The RTC can be powered by a backup battery when the main supply is not present, and the devices include a coin-cell charger to recharge the backup battery as needed.

The USB module provides a HS 2.0 OTG transceiver suitable for direct connection to the OMAP UTMI+ low pin interface (ULPI), with an integrated charge pump and full support for the carkit CEA-936A specification. An ADC is provided for monitoring signals, such as supply voltage, entering the device, and two additional external ADC inputs are provided for system use.

The devices provide driver circuitry to power two LED circuits that can illuminate a panel or provide user indicators. The drivers also provide pulse width modulation (PWM) circuits to control the illumination levels of the LEDs. A keypad interface implements a built-in scanning algorithm to decode hardware-based key presses and reduce software use, with multiple additional general-purpose input/output devices (GPIOs) that can be used as interrupts when configured as inputs.

5.2.2 TPS-65930: Features

The TPS65930 devices offer the following features:

- Audio:
  - Differential input main microphones
  - Mono auxiliary input
  - External predrivers for class D (stereo)
  - Automatic level control (ALC)
  - Digital and analog mixing
  - 16-bit linear audio stereo DAC (96, 48, 44.1, and 32 kHz and derivatives)
  - 16-bit linear audio stereo ADC (48, 44.1, and 32 kHz and derivatives)
- USB:
  - USB 2.0 on-the-go (OTG)-compliant HS transceivers
  - 12-bit universal transceiver macro interface ULPI
  - USB power supply (5-V charge pump for VBUS)
- Additional Features:
  - Keypad Interface (up to 6 × 6)
- Backup battery charger

5.3 Memory Rev C

The TAO-3530 has a 32 bit External Memory Interfaces (EMI) controller.

The 32 bit wide channel is connected 16 bit wide to two Hynix H5MS1G62AFR MOBILE DDR SDRAM Chips.

The standard configuration is organized as 1Gbit (4Bank x 16M x 16bits). Therefore given 2 chips are used a total of 2Gbit or 256MB of memory is available.

Features:

- Mobile DDR SDRAM
  - Double data rate architecture: two data transfer per clock cycle
- Mobile DDR SDRAM INTERFACE
  - x16 bus width
  - Multiplexed Address (Row address and Column address)
- SUPPLY VOLTAGE
  - 1.8V device: VDD and VDDQ = 1.7V to 1.95V
- MEMORY CELL ARRAY
  - 1Gbit (x16 device) = 4Bank x 16Mb x 16 I/O
- DATA STROBE
  - x16 device: LDQS and UDQS
  - Bidirectional, data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
  - Data and data mask referenced to both edges of DQS
- LOW POWER FEATURES
  - PASR (Partial Array Self Refresh)
  - AUTO TCSR (Temperature Compensated Self Refresh)
  - DS (Drive Strength)
- INPUT CLOCK
  - Differential clock inputs (CK, CK)
- Data MASK
  - LDM and UDM: Input mask signals for write data
  - DM masks write data-in at the both rising and falling edges of the data strobe
- MODE and EXTENDED MODE REGISTER SET and STATUS REGISTER READ
  - Keep to the JEDEC Standard regulation (Low Power DDR SDRAM)
- CAS LATENCY
  - Programmable CAS latency 2 or 3 supported
- BURST LENGTH
  - Programmable burst length 2 / 4 / 8 with both sequential and interleave mode
- AUTO PRECHARGE
  - Option for each burst access
- AUTO REFRESH AND SELF REFRESH MODE
- CLOCK STOP MODE
  - Keep to the JEDEC Standard regulation
- INITIALIZING THE MOBILE DDR SDRAM
  - Occurring at device power up or interruption of device power

5.4 Memory Rev A and B

The TAO-3530 has a 32 bit External Memory Interfaces (EMI) controller.

The 32 bit wide channel is connected 32 bit wide to one Hynix H5MS1G22AFR or Micron MT46H32M32LFCM MOBILE DDR SDRAM Chip.

The standard configuration is organized as 1Gbit (4Bank x 8M x 32bits). Therefore given 1 chip is used a total of 1Gbit or 128MB of memory is available.

Features:

- Mobile DDR SDRAM
  - Double data rate architecture: two data transfer per clock cycle
- Mobile DDR SDRAM INTERFACE
  - X32 bus width
  - Multiplexed Address (Row address and Column address)
- SUPPLY VOLTAGE
  - 1.8V device: VDD and VDDQ = 1.7V to 1.95V
- MEMORY CELL ARRAY
  - 1Gbit (x32 device) = 8M x 4Bank 32 I/O
- DATA STROBE
  - X32 device: DQS0 ~ DQS3
  - Bidirectional, data strobe (DQS) is transmitted and received with data, to be used in capturing data at the receiver
  - Data and data mask referenced to both edges of DQS
- LOW POWER FEATURES
  - PASR (Partial Array Self Refresh)
  - AUTO TCSR (Temperature Compensated Self Refresh)
  - DS (Drive Strength)
- INPUT CLOCK
  - Differential clock inputs (CK, CK)
- Data MASK
  - DM0 ~ DM3: Input mask signals for write data
  - DM masks write data-in at the both rising and falling edges of the data strobe
- MODE and EXTENDED MODE REGISTER SET and STATUS REGISTER READ
  - Keep to the JEDEC Standard regulation (Low Power DDR SDRAM)
- CAS LATENCY
  - Programmable CAS latency 2 or 3 supported
- BURST LENGTH
  - Programmable burst length 2 / 4 / 8 with both sequential and interleave mode
- AUTO PRECHARGE
  - Option for each burst access
- AUTO REFRESH AND SELF REFRESH MODE
- CLOCK STOP MODE
  - Keep to the JEDEC Standard regulation
- INITIALIZING THE MOBILE DDR SDRAM
  - Occurring at device power up or interruption of device power

5.5 NAND Flash

NAND on the TAO-3530 is populated as Micron MT29F4G16ABBDAH4D and connected 16 bit wide to the OMAP3530 GPMC bus.

The default TAO-3530 supports the chip which provides 512MB of addressable space.

The GPMC_nCS0 signal is used for its selection.

Features:

- Open NAND Flash Interface (ONFI) 1.0-compliant
- Single-level cell (SLC) technology
- Organization
  - Page size x8: 2112 bytes (2048 + 64 bytes)
  - Page size x16: 1056 words (1024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Plane size: 2 planes x 2048 blocks per plane
  - Device size: 4Gb: 4096 blocks; 8Gb: 8192 blocks
- Asynchronous I/O performance
  - tRC/ tWC: 20ns (3.3V), 25ns (1.8V)
- Array performance
  - Read page: 25µs
  - Program page: 200µs (TYP: 1.8V, 3.3V)
  - Erase block: 700µs (TYP)
- Command set: ONFI NAND Flash Protocol
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Ready/Busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: Write protect entire device
- First block (block address 00h) is valid when shipped from factory with ECC. For minimum required ECC, see Error Management.
- Block 0 requires 1-bit ECC if PROGRAM/ERASE cycles are less than 1000
- RESET (FFh) required as first command after power on
- Alternate method of device initialization (Nand_Init) after power up (contact factory)
- Internal data move operations supported within the plane from which data is read
- Quality and reliability
  - Data retention: 10 years
  - Endurance: 100,000 PROGRAM/ERASE cycles

5.6 WiFi Module

The Marvell® 88W8686 is a low-power highly-integrated IEEE 802.11g/b MAC/Baseband/RF WLAN system-on-chip (SoC), designed to support IEEE 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps, as well as 802.11b data rates of 1, 2, 5.5, and 11 Mbps.

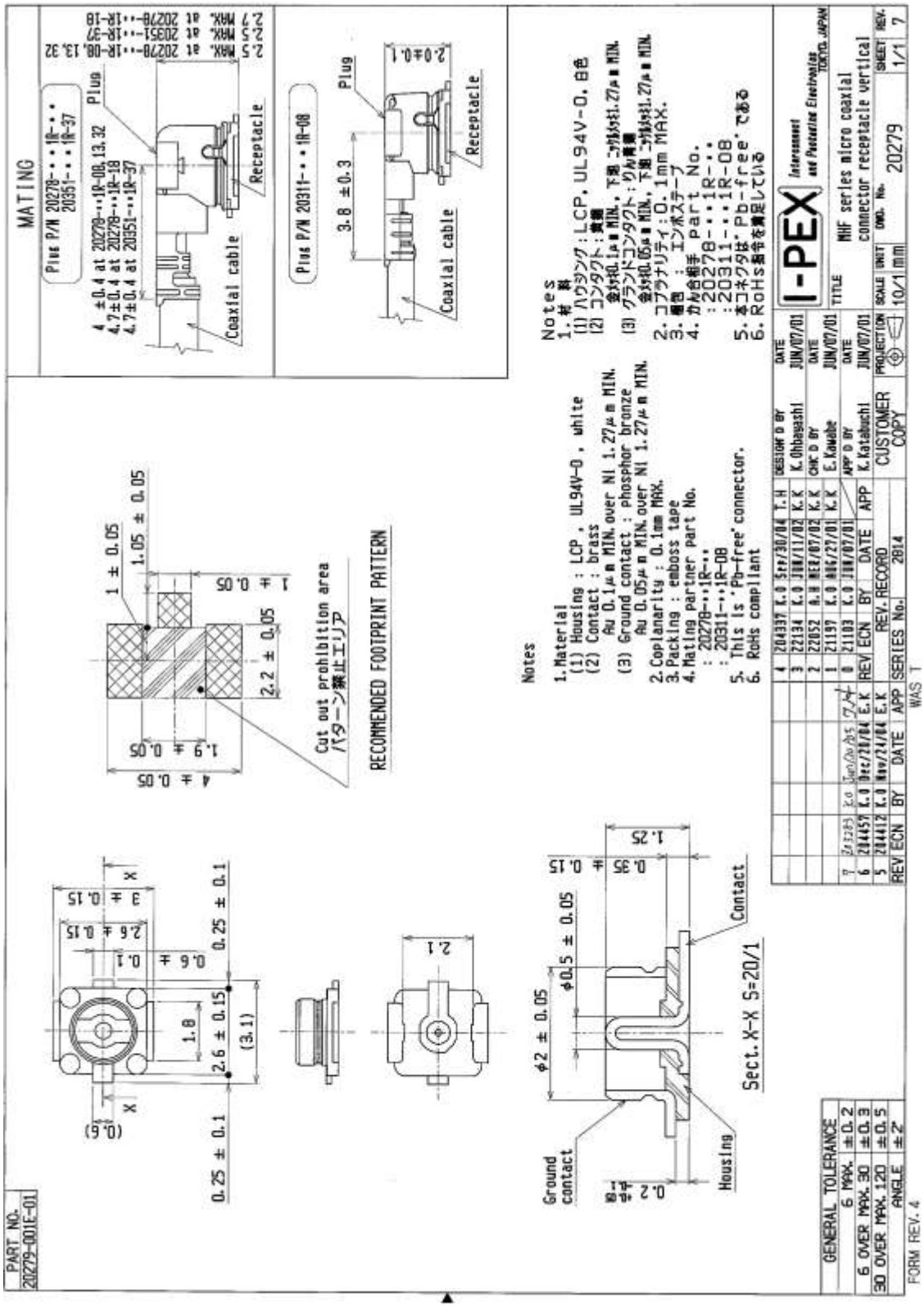
General features:

- Ultra low-power dissipation
- Single-chip integration of 802.11g/b wireless RF and baseband, MAC, CPU, memory, and host interfaces
- Integrates all RF to baseband transmit and receive operations, with support for external PAs
- Fully integrated frequency synthesizers with optimized phase noise performance for OFDM applications
- Integrated direct conversion WLAN RF radio
- Supports 19.2, 20, 24, 26, 38.4, and 40 MHz oscillator clock sources
- Software backward compatible with 88W8385 and 88W8015 devices

5.6.1 WiFi Signals Description

SIGNAL NAME	DESCRIPTION
MMC2_CLK	Clock
MMC2_CMD	Command
MMC2_d0	4 bit data
MMC2_d1	4 bit data
MMC2_d2	4 bit data
MMC2_d3	4 bit data
GPIO 15	Reserved
GPIO 157	Wifi enable - power on/ off

5.6.2 I-PEX Connector



6 How to use the Multiplex Mode

The function of the pins on the module can be changed by adjusting the multiplex mode (mux).

6.1 Multiplexing in u-boot

Multiplexing can be done in u-boot in the tao3530.h file

(Use the file in this directory: board/technexion/tao3530/tam3530.h)

Example of what it might look like:

MUX_VAL(CP(MCSPI2_CS1), (IEN|PTD|EN|M4))

The last part "M4" is the multiplex mode and you can change that according the table in Chapter 7.

The line of code is build up as follows:

- The name of the variable is the function in Mode 0; MCSPI2_CS1
- The current Multiplex mode is M4, which means that currently this pin is GPIO_182

Pin #	Ball #	Pin Name	mode	V	type	description
B1-A8	M4	Hsusb_data3	3	1.8	IO	Dedicated for external transceiver Bidirectional data bus
		Mcspi2_cs1	0		O	SPI Enable 1, polarity configured by software
		Gpt8_pwm_evt	1		IO	PWM or event for GP timer 8
		Hsusb2_tll_Data3	2		IO	Dedicated for external transceiver Bidirectional data bus
		GPIO_182	4		IO	General-purpose IO 182
		Mm2_txen_n	5		IO	
		Safe_mode	7			

Table 1: Example of pin B1-A8 on the TAO-3530 module and the different functions for each multiplex mode (see Chapter 7)

After this you will need to recompile:

```
Uboot#      make distclean
Uboot#      make tao3530_config
Uboot#      make tao3530
```

This will create the u-boot.bin

7 OMAP-3530 Module Pin Description

Pin #	Ball #	Pin Name	mode	V	type	description
B1-A1	V4	MCBSP3_FSX	0	1.8	IO	Combined frame synchronization
		UART2_RX	1		I	UART2 Receive data
		GPIO_143	4		IO	General-purpose IO 143
		Safe_mode	7			
B1-A2	V5	MCBSP3_DR	0	1.8	I	Received serial data
		UART2_RTS	1		O	UART2 Request To Send
		GPIO_141	4		IO	General-purpose IO 141
		Safe_mode	7			
B1-A3	V6	MCBSP3_DX	0	1.8	IO	Transmitted serial data
		UART2_CTS	1		I	UART2 Clear To Send
		GPIO_140	4		IO	General-purpose IO 140
		Safe_mode	7			
B1-A4	W4	MCBSP3_CLKX	0	1.8	IO	Combined serial clock
		UART2_TX	1		O	UART2 Transmit data
		GPIO_142	4		IO	General-purpose IO 142
		Safe_mode	7			
B1-A5	N5	Hsusb2_Data7	3	1.8	IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		MCSPI2_Clk	0		IO	SPI Clock
		Hsusb2_TLL_Data7	2		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		GPIO_178	4		IO	General-purpose IO 178
		Safe_mode	7			
B1-A6	N3	Hsusb_Data5	3	1.8	IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		Mcspi2_somi	0		IO	Slave data out, master data in
		Gpt10_pwm_evt	1		IO	PWM or event for GP timer 10
		Hsusb2_tll_data5	2		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		GPIO_180	4		IO	General-purpose IO 180
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B1-A7	N4	Hsusb2_Data4	3	1.8	IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		Mcspi2_simo	0		IO	Slave data in, master data out
		Gpt9_pwm_evt	1		IO	PWM or event for GP timer 9
		Hsusb2_tll_Data4	2		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		GPIO_179	4		IO	General-purpose IO 179
		Safe_mode	7			
B1-A8	M4	Hsusb_data3	3	1.8	IO	Dedicated for external transceiver Bidirectional data bus
		Mcspi2_cs1	0		O	SPI Enable 1, polarity configured by software
		Gpt8_pwm_evt	1		IO	PWM or event for GP timer 8
		Hsusb2_tll_Data3	2		IO	Dedicated for external transceiver Bidirectional data bus
		GPIO_182	4		IO	General-purpose IO 182
		Mm2_txen_n	5		IO	
		Safe_mode	7			
B1-A9	M5	Hsusb2_Data6	3	1.8	IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		Mcspi2_cs0	0		IO	SPI Enable 0, polarity configured by software
		Gpt11_pwm_evt	1		IO	PWM or event for GP timer 11
		Hsusb2_tll_Data6	2		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		GPIO_181	4		IO	General-purpose IO 181
		Safe_mode	7			
B1_A10	B23	UART3_RTS_SD	0	1.8	O	UART3 Request To Send, IR enable
		GPIO_164	4		IO	General-purpose IO 164
		Safe_mode	7			
B1_A11	A23	UART3_CTS_RCTX	0	1.8	IO	UART3 Clear To Send (input), Remote TX (output)
		GPIO_163	4		IO	General-purpose IO 163
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B1_A12	B24	UART3_RX_IRRX	0	1.8	I	UART3 Receive data, IR and Remote RX
		GPIO_165	4		IO	General-purpose IO 165
		Safe_mode	7			
B1_A13	C23	UART3_TX_IRTX	0	1.8	O	UART3 Transmit data, IR TX
		GPIO_166	4		IO	General-purpose IO 166
		Safe_mode	7			
B1_A14	W19	Mcspi4_clk	1	1.8	IO	SPI Clock
		Mcbsp1_clkr	0		IO	Receive Clock
		GPIO_156	4		IO	General-purpose IO 156
		Safe_mode	7			
B1_A15	W18	Mcspi4_simo	1	1.8	IO	Slave data in, master data out
		Mcbsp1_dx	0		IO	Transmitted serial data
		Mcbsp3_dx	1		IO	Transmitted serial data
		GPIO_158	4		IO	General-purpose IO 158
		Safe_mode	7			
B1_A16	Y18	Mcspi4_somi	1	1.8	IO	Slave data out, master data in
		Mcbsp1_dr	0		I	Received serial data
		Mcbsp3_dr	2		I	Received serial data
		GPIO_159	4		IO	General-purpose IO 159
		Safe_mode	7			
B1_A17	AA19	Mcspi4_cs0	1	1.8	IO	SPI Enable 0, polarity configured by software
		Mcbsp1_fsx	0		IO	Transmit frame synchronization
		Mcbsp3_fsx	2		IO	Combined frame synchronization
		GPIO_161	4		IO	General-purpose IO 161
		Safe_mode	7			
B1_A18	X	MICBIAS1		2.5/ 2.75	Pwr	Analog microphone bias 1
B1_A19	X	MIC_MAIN_M		2.5/ 2.75	I	Main microphone left input (M)
B1_A20	X	GND			GND	Ground
B1_A21	X	MIC_BIAS_G			GND	Dedicated ground for microphones
B1_A22	X	GND			GND	Ground
B1_A23	X	BKBAT		3.3	Pwr	Backup battery
B1_A24	X	GND			GND	Ground
B1_A25	X	GND			GND	Ground
B1_A26	X	GND			GND	Ground
B1_A27	X	GND			GND	Ground
B1_A28	X	GND			GND	Ground
B1_A29	X	GND			GND	Ground
B1_A30	X	GND			GND	Ground

Pin #	Ball #	Pin Name	mode	V	type	description
B1_A31	X	GND			GND	Ground
B1_A32	X	GND			GND	Ground
B1_A33	X	GND			GND	Ground
B1_A34	W7	UART1_TX	0	1.8	O	UART1 Transmit data
		GPIO_148	4		IO	General-purpose IO 148
		Safe_mode	7			
B1_A35	V7	UART1_RX	0	1.8	I	UART1 Receive data
		Mcbsp1_clkr	2		IO	Receive Clock
		Mcspi4_clk	3		IO	SPI Clock
		GPIO_151	4		IO	General-purpose IO 151
		Safe_mode	7			
B1_A36	W6	UART1_RTS	0	1.8	O	UART1 Request to Send
		GPIO_149	4		IO	General-purpose IO 149
		Safe_mode	7			
B1_A37	AC2	UART1_CTS	0	1.8	I	UART1 Clear to send
		GPIO_150	4		IO	General-purpose IO 150
		Safe_mode	7			
B1_A38	AA2	GPIO_137	4	1.8	IO	General-purpose IO 137
		MMC2_dat5	0		IO	MMC/SD Card Data bit 5
		MMC2_dir_dat1	1		O	Direction control for DAT1 and DAT3 signals case an external transceiver used
		Cam_global_reset	2		IO	Global reset is used strobe synchronization
		MMC3_dat1	3		IO	MMC/SD Card Data bit 1
		Safe_mode	7			
B1_A39	Y2	LCD_ENVDD	4	1.8	IO	General-purpose IO 138
		MMC2_dat6	0		IO	MMC/SD Card Data bit 6
		MMC2_dir_cmd	1		O	Direction control for CMD signal case an external transceiver is used
		Cam_shutter	2		O	Mechanical shutter control signal
		MMC3_dat2	3		IO	MMC/SD Card Data bit 2
		Safe_mode	7			
B1_A40	X	VBUS_5V0		5	I	Power
B1_A41	X	DC_5V		5	I	Power
B1_A42	X	HSUSB_DN			IO	USB data N/USB carkit transmit data
B1_A43	X	HSUSB_DP				USB data N/USB carkit receive data
B1_A44	X	PreDriv.LEFT			O	Predriver output left P for external class-D amplifier
B1_A45	X	PreDriv.RIGHT			O	Predriver output right P for external class-D amplifier

Pin #	Ball #	Pin Name	mode	V	type	description
B1_A46	X	VBAT		4.2	Pwr	Power
B1_A47	X	VBAT		4.2	Pwr	Power
B1_A48	X	VBAT		4.2	Pwr	Power
B1_A49	X	VBAT		4.2	Pwr	Power
B1_A50	X	VBAT		4.2	Pwr	Power
B1_B1	X	3.3V		3.3	I	Power (optional)
B1_B2	X	3.3V		3.3	I	Power (optional)
B1_B3	R4	c	0	1.8	IO	Slave data in, master data out
		MMC2_dat5	1		IO	MMC/SD Card Data bit 5
		GPIO_172	4		IO	General-purpose IO 172
		Safe_mode	7			
B1_B4	T4	Mcspi1_somi	0	1.8	IO	Slave data out, master data in
		MMC2_dat6	1		IO	MMC/SD Card Data bit 6
		GPIO_173	4		IO	General-purpose IO 173
		Safe_mode	7			
B1_B5	T5	Mcspi1_clk	0	1.8	IO	SPI Clock
		MMC2_dat4	1		IO	MMC/SD Card Data bit 4
		GPIO_171	4		IO	General-purpose IO 171
		Safe_mode	7			
B1_B6	T6	Mcspi1_cs0	0	1.8	IO	SPI Enable 0, polarity configured by software
		MMC2_dat7	1		IO	MMC/SD Card Data bit 7
		GPIO_174	4		IO	General-purpose IO 174
		Safe_mode	7			
B1_B7	R5	Hsusb2_data2	3	1.8	IO	Dedicated for external transceiver Bidirectional data bus
		Mcspi1_cs3	0		O	SPI Enable 3, polarity configured by software
		Hsusb2_tll_data2	2		IO	Dedicated for external transceiver Bidirectional data bus
		GPIO_177	4		IO	General-purpose IO 177
		Mm2_txdat	5		IO	USB data. Used as VP in 4-pin VP_VM mode.
		Safe_mode	7			
B1_B8	AB2	Touch Interrupt	4	1.8	IO	General-purpose IO 136
		MMC2_dat4	0		IO	MMC/SD Card Data bit 4
		MMC2_dir_dat0	1		O	Direction control for DAT0 signal case an external transceiver used
		MMC3_dat0	3		IO	MMC/SD Card Data bit 0 / SPI Serial Input
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B1_B9	A24	HDQ_SIO	0	1.8	IOD	Bidirectional HDQ 1-Wire control and data Interface. Output is open drain.
		Sys_altclk	1		I	Alternate clock source selectable for GPTIMERs (maximum 54 MHz), USB (48 MHz), or NTSC/PAL (54 MHz)
		I2C2_sccbe	2		O	Serial Camera Control Bus Enable
		I2C3_sccbe	3		O	Serial Camera Control Bus Enable
		GPIO_170	4		IO	General-purpose IO 170
		Safe_mode	7			
B1_B10	AB16	Sys_boot5	0	1.8	I	Boot configuration mode bit 5
		MMC2_dir_dat3	1		O	Direction control for DAT4, DAT5, DAT6, and DAT7 signals case an external transceiver used
		GPIO_7	4		IO	General-purpose IO 7
		Safe_mode	7			
B1_B11	AC12	I2C3_SDA	0	1.8	IOD	I2C Serial Bidirectional Data. Output is open drain
		GPIO_185	4		IO	General-purpose IO 185
		Safe_mode	7			
B1_B12	AC13	I2C3_SCL	0	1.8	IOD	I2C Master Serial clock. Output is open drain
		GPIO_184	4		IO	General-purpose IO 184
		Safe_mode	7			
B1_B13	AC14	I2C2_SDA	0	1.8	IOD	I2C Serial Bidirectional Data. Output is open drain
		GPIO_183	4		IO	General-purpose IO 183
		Safe_mode	7			
B1_B14	AC15	I2C2_SCL	0	1.8	IOD	I2C Master Serial clock. Output is open drain
		GPIO_168	4		IO	General-purpose IO 168
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B1_B15	AC1	GPIO_12	4	1.8	IO	General-purpose IO 12
		Etk_clk	0		O	ETK trace clock
		Mcbsp5_clkx	1		IO	Combined serial clock
		Mmc3_clk	2		O	MMC/SD Output Clock
		Hsusb1_stp	3		O	Dedicated for external transceiver Stop signal
		Mm1_rxdp	5		IO	Vplus receive data (not used in 3- or 4-pin configurations)
		Hsusb1_tll_stp	6		I	Dedicated for external transceiver Stop signal
B1_B16	AD3	GPIO_13	4	1.8	IO	General-purpose IO 13
		Etk_ctl	0		O	ETK trace ctl
		Mmc3_cmd	2		IO	MMC/SD command signal
		Hsusb1_clk	3		O	Dedicated for external transceiver 60-MHz clock input to PHY
		Hsusb1_tll_clk	6		O	Dedicated for external transceiver 60-MHz clock input to PHY
B1_B17	AD6	Mcbsp3_simo	1	1.8	IO	Slave data in, master data out
		Etk_d0	0		O	ETK data 0
		Mmc3_dat4	2		IO	MMC/SD Card Data bit 4
		Hsusb1_data0	3		IO	Dedicated for external transceiver Bidirectional data bus
		GPIO_14	4		IO	General-purpose IO 14
		Mm1_rxrcv	5		IO	Differential receiver signal input (not used in 3-pin mode)
		Hsusb1_tll_data0	6		IO	Dedicated for external transceiver Bidirectional data bus
B1_B18	AC6	Mcbsp3_somi	1	1.8	IO	Slave data out, master data in
		Etk_d1	0		O	ETK data 1
		Hsusb1_data1	3		IO	Dedicated for external transceiver Bidirectional data bus
		GPIO_15	4		IO	General-purpose IO 15
		Mm1_txse0	5		IO	Single-ended zero. Used as VM in 4-pin VP_VM mode.
		Hsusb1_tll_data1	6		IO	Dedicated for external transceiver Bidirectional data bus

Pin #	Ball #	Pin Name	mode	V	type	description
B1_B19	AC7	Mcspi3_cs0	1	1.8	IO	SPI Enable 0, polarity configured by software
		Etk_d2	0		O	ETK data 2
		Hsusb1_data2	3		IO	Dedicated for external transceiver Bidirectional data bus
		GPIO_16	4		IO	General-purpose IO 16
		Mm1_txdat	5		IO	USB data. Used as VP in 4-pin VP_VM mode.
		Hsusb_tll_data2	6		IO	Dedicated for external transceiver Bidirectional data bus
B1_B20	AD8	Mcspi3_clk	1	1.8	IO	SPI Enable 0, polarity configured by software
		Etk_d3	0		O	ETK data 3
		Mmc3_dat3	2		IO	MMC/SD Card Data bit 3
		Hsusb1_data7	3		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		GPIO_17	4		IO	General-purpose IO 17
		Hsusb1_tll_data7	6		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
B1_B21	AC5	GPIO_18	4	1.8	IO	General-purpose IO 18
		Etk_d4	0		O	ETK data 4
		Mcbsp5_dr	1		I	Received serial data
		Mmc3_dat0	2		IO	MMC/SD Card Data bit 0 / SPI Serial Input
		Hsusb1_data4	3		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		Hsusb1_tll_data4	6		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation

Pin #	Ball #	Pin Name	mode	V	type	description
B1_B22	AD2	GPIO_19	4	1.8	IO	General-purpose IO 19
		Etk_d5	0		O	ETK data 5
		Mcbsp5_fsx	1		IO	Combined frame synchronization
		Mmc3_dat1	2		IO	MMC/SD Card Data bit 1
		Hsusb1_data5	3		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		Hsusb1_tll_data5	6		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
B1_B23	AC8	GPIO_20	4	1.8	IO	General-purpose IO 20
		Etk_d6	0		O	ETK data 6
		Mcbsp5_dx	1		IO	Transmitted serial data
		Mmc3_dat2	2		IO	MMC/SD Card Data bit 2
		Hsusb1_data6	3		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
		Hsusb1_tll_data6	6		IO	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation
B1_B24	AD9	Mcspi3_cs1	1	1.8	O	SPI Enable 1, polarity configured by software
		Etk_d7	0		O	ETK data 7
		Mmc3_dat7	2		IO	MMC/SD Card Data bit 7
		Hsusb1_data3	3		IO	Dedicated for external transceiver Bidirectional data bus
		GPIO_21	4		IO	General-purpose IO 21
		Mm1_txen_n	5		IO	Transmit enable
		Hsusb1_tll_data3	6		IO	Dedicated for external transceiver Bidirectional data bus

Pin #	Ball #	Pin Name	mode	V	type	description
B1_B25	AD5	MMC1_WP	4	1.8	IO	General-purpose IO 23
		Etk_d9	0		O	ETK data 9
		Sys_secure_indicator	1		O	MSECURE transactions indicator
		Mmc3_dat5	2		IO	MMC/SD Card Data bit 5
		Hsusb1_nxt	3		I	Dedicated for external transceiver Next signal from PHY
		Mm1_rxdm	5		IO	Vminus receive data (not used in 3- or 4-pin configurations)
		Hsusb1_tll_nxt	6		O	Dedicated for external transceiver Next signal from PHY
B1_B26	AC4	GPIO_22	4	1.8	IO	General-purpose IO 22
		Etk_d8	0		O	ETK data 8
		Sys_drm_msecure	1		O	MSECURE output
		Mmc3_dat6	2		IO	MMC/SD Card Data bit 6
		Hsusb1_dir	3		I	Dedicated for external transceiver data direction control from PHY
		Hsusb1_tll_dir	6		O	Dedicated for external transceiver data direction control from PHY
B1_B27	AC3	Hsusb2_clk	3	1.8	O	Dedicated for external transceiver 60-MHz clock input to PHY
		Etk_d10	0		O	ETK data 10
		UART1_RX	2		I	UART1 Receive data
		GPIO_24	4		IO	General-purpose IO 24
		Hsusb2_tll_clk	6		O	Dedicated for external transceiver 60-MHz clock input to PHY
B1_B28	AC9	Hsusb2_stp	3	1.8	O	Dedicated for external transceiver Stop signal
		Etk_d11	0		O	ETK data 11
		GPIO_25	4		IO	General-purpose IO 25
		Mm2_rxdp	5		IO	Vplus receive data (not used in 3- or 4-pin configurations)
		Hsusb2_tll_stp	6		I	Dedicated for external transceiver Stop signal

Pin #	Ball #	Pin Name	mode	V	type	description
B1_B29	AC10	Hsusb2_dir	3	1.8	I	Dedicated for external transceiver Data direction control from PHY
		Etk_d12	0		O	ETK data 12
		GPIO_26	4		IO	General-purpose IO 26
		Hsusb2_tll_dir	6		O	Dedicated for external transceiver Data direction control from PHY
B1_B30	AD11	Hsusb2_nxt	3	1.8	I	Dedicated for external transceiver Next signal from PHY
		Etk_d13	0		O	ETK data 13
		GPIO_27	4		IO	General-purpose IO 27
		Mm2_rxdm	5		IO	Vminus receive data (not used in 3- or 4-pin configurations)
		Hsusb2_tll_nxt	6		O	Dedicated for external transceiver Next signal from PHY
B1_B31	AC11	Hsusb2_data0	3	1.8	IO	Dedicated for external transceiver Bidirectional data bus
		Etk_d14	0		O	ETK data 14
		GPIO_28	4		IO	General-purpose IO 28
		Mm2_rxrcv	5		IO	Differential receiver signal input (not used in 3-pin mode)
		Hsusb2_tll_data0	6		IO	Dedicated for external transceiver Bidirectional data bus
B1_B32	V18	GPIO_162	4	1.8	IO	General-purpose IO 162
		Mcbsp1_clkx	0		IO	Transmit clock
		Mcbsp3_clkx	2		IO	Combined serial clock
		Safe_mode	7			
B1_B33	X	Not connected			IO	TechNexion Internal test pin
B1_B34	X	ADCIN2		2.5/ 2.75	I	General-purpose ADC input
B1_B35	AA10	SYS_nRESPWRON	0	1.8	I	Power on reset
B1_B36	X	PWR_ON		4.2	I	detect a control command to start or stop the system
B1_B37	X	MIC_MAIN_P		2.5/ 2.75	I	Main microphone left input (P)
B1_B38	X	AUXR		2.5/ 2.75	I	Auxiliary audio input right
B1_B39	X	Hsusb_ID		4.2	IO	USB ID

Pin #	Ball #	Pin Name	mode	V	type	description
B1_B40	X	LCD_ENBKL		1.8	IO	GPIO_6
		PWM0			O	Pulse width driver 0
		TEST3			IO	TEST3 pin used in test mode only (controlled by JTAG)
B1_B41	X	HOST_nOC		1.8	IO	GPIO_1
		JTAG.TMS			I	JTAG test mode state
B1_B42	X	LEDA		4.2	OD	LED leg A
		VIBRA.P			OD	H-bridge vibrator P
B1_B43	X	SYSEN		1.8	IOD	System enable output
B1_B44	X	CHGR_STATE		1.8	IO	ADCIN0: Battery type
B1_B45	X	VIO_1V8		1.8	Pwr	Power
B1_B46	X	VIO_1V8		1.8	Pwr	Power
B1_B47	X	VIO_1V8		1.8	Pwr	Power
B1_B48	X	VIO_1V8		1.8	Pwr	Power
B1_B49	AB24	TV_OUT1		1.8	O	TV analog output Composite
B1_B50	AA23	TV_OUT2		1.8	O	TV analog output S-VIDEO
B2_A1	AB18	CAM_D0	0	1.8	I	Camera digital image data bit 0
		GPIO_99	4		I	General-purpose IO 99
		Safe_mode	7			
B2_A2	AC18	CAM_D1	0	1.8	I	Camera digital image data bit 1
		GPIO_100	4		IO	General-purpose IO 100
		Safe_mode	7			
B2_A3	G19	CAM_D2	0	1.8	I	Camera digital image data bit 2
		GPIO_101	4		IO	General-purpose IO 101
		Safe_mode	7			
B2_A4	F19	CAM_D3	0	1.8	I	Camera digital image data bit 3
		GPIO_102	4		IO	General-purpose IO 102
		Safe_mode	7			
B2_A5	G20	CAM_D4	0	1.8	I	Camera digital image data bit 4
		GPIO_103	4		IO	General-purpose IO 103
		Safe_mode	7			
B2_A6	B21	CAM_D5	0	1.8	I	Camera digital image data bit 5
		GPIO_104	4		IO	General-purpose IO 104
		Safe_mode	7			
B2_A7	L24	CAM_D6	0	1.8	I	Camera digital image data bit 6
		GPIO_105	4		IO	General-purpose IO 105
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B2_A8	K24	CAM_D7	0	1.8	I	Camera digital image data bit 7
		GPIO_106	4		IO	General-purpose IO 106
		Safe_mode	7			
B2_A9	A22	CAM_HS	0	1.8	IO	Camera Horizontal Synchronization
		GPIO_94	4		IO	General-purpose IO 94
		Safe_mode	7			
B2_A10	E18	CAM_VS	0	1.8	IO	Camera Vertical Synchronization
		GPIO_95	4		IO	General-purpose IO 95
		Safe_mode	7			
B2_A11	X	DVI_nDisable		1.8	IO	General-purpose IO 7
		VIBRA.SYNC			I	Vibrator on-off synchronization
		PWM1			O	Pulse width driver
		TEST4			IO	TEST4 pin used in test mode only (controlled by JTAG)
B2_A12	AA1	LCD_PON	4	1.8	IO	General-purpose IO 139
		MMC2_dat7	0		IO	MMC/SD Card Data bit 7
		MMC2_clkin	1		I	MMC/SD input Clock
		MMC3_dat3	3		IO	MMC/SD Card Data bit 3
		Safe_mode	7			
B2_A13	K4	GPMC_A1	0	1.8	O	General-purpose memory address bit 1
		GPIO_34 (2)	4		IO	General-purpose IO 34
		Safe_mode	7			
B2_A14	K3	GPMC_A2	0	1.8	O	General-purpose memory address bit 2
		Sys_ndmareq3	1		I	External DMA request 3 (system expansion). Level (active low) or edge (falling) selectable.
		GPIO_43 (2)	4		IO	General-purpose IO 43
		Safe_mode	7			
B2_A15	K2	GPMC_A3	0	1.8	O	General-purpose memory address bit 3
		GPIO_36 (2)	4		IO	General-purpose IO 36
		Safe_mode	7			
B2_A16	J4	GPMC_A4	0	1.8	O	General-purpose memory address bit 4
		GPIO_37 (2)	4		IO	General-purpose IO 37
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B2_A17	J3	GPMC_A5	0	1.8	O	General-purpose memory address bit 5
		GPIO_38 (2)	4		IO	General-purpose IO 38
		Safe_mode	7			
B2_A18	J2	GPMC_A6	0	1.8	O	General-purpose memory address bit 6
		GPIO_39 (2)	4		IO	General-purpose IO 39
		Safe_mode	7			
B2_A19	J1	GPMC_A7	0	1.8	O	General-purpose memory address bit 7
		GPIO_40 (2)	4		IO	General-purpose IO 40
		Safe_mode	7			
B2_A20	H1	GPMC_A8	0	1.8	O	General-purpose memory address bit 8
		GPIO_41 (2)	4		IO	General-purpose IO 41
		Safe_mode	7			
B2_A21	H2	GPMC_A9	0	1.8	O	General-purpose memory address bit 9
		Sys_ndmareq2	1		I	External DMA request 2 (system expansion). Level (active low) or edge (falling) selectable.
		GPIO_42 (2)	4		IO	General-purpose IO 42
		Safe_mode	7			
B2_A22	G2	GPMC_A10	0	1.8	O	General-purpose memory address bit 10
		Sys_ndmareq3	1		I	External DMA request 3 (system expansion). Level (active low) or edge (falling) selectable.
		GPIO_43 (2)	4		IO	General-purpose IO 43
		Safe_mode	7			
B2_A23	L2	GPMC_D0	0	1.8	IO	GPMC Data bit 0
B2_A24	M1	GPMC_D1	0	1.8	IO	GPMC Data bit 1
B2_A25	M2	GPMC_D2	0	1.8	IO	GPMC Data bit 2
B2_A26	N2	GPMC_D3	0	1.8	IO	GPMC Data bit 3
B2_A27	M3	GPMC_D4	0	1.8	IO	GPMC Data bit 4
B2_A28	P1	GPMC_D5	0	1.8	IO	GPMC Data bit 5
B2_A29	P2	GPMC_D6	0	1.8	IO	GPMC Data bit 6
B2_A30	R1	GPMC_D7	0	1.8	IO	GPMC Data bit 7
B2_A31	R2	GPMC_D8	0	1.8	IO	GPMC Data bit 8
		GPIO_44 (1)	4		IO	General-purpose IO 44
		Safe_mode	7			
B2_A32	T2	GPMC_D9	0	1.8	IO	GPMC Data bit 9
		GPIO_45 (1)	4		IO	General-purpose IO 45
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B2_A33	U1	GPMC_D10	0	1.8	IO	GPMC Data bit 10
		GPIO_46 (1)	4		IO	General-purpose IO 46
		Safe_mode	7			
B2_A34	R3	GPMC_D11	0	1.8	IO	GPMC Data bit 11
		GPIO_47 (1)	4		IO	General-purpose IO 47
		Safe_mode	7			
B2_A35	T3	GPMC_D12	0	1.8	IO	GPMC Data bit 12
		GPIO_48 (1)	4		IO	General-purpose IO 48
		Safe_mode	7			
B2_A36	U2	GPMC_D13	0	1.8	IO	GPMC Data bit 13
		GPIO_49 (1)	4		IO	General-purpose IO 49
		Safe_mode	7			
B2_A37	V1	GPMC_D14	0	1.8	IO	GPMC Data bit 14
		GPIO_50 (1)	4		IO	General-purpose IO 50
		Safe_mode	7			
B2_A38	V2	GPMC_D15	0	1.8	IO	GPMC Data bit 15
		GPIO_51 (1)	4		IO	General-purpose IO 51
		Safe_mode	7			
B2_A39	G3	GPMC_nWE	0	1.8	O	Write Enable
B2_A40	F2	GPMC_nOE	0	1.8	O	Output Enable
B2_A41	L1	GPMC_nBE1	0	1.8	O	Upper Byte Enable
		GPIO_61	4		IO	General-purpose IO 61
		Safe_mode	7			
B2_A42	C2	GPMC_WAIT3	0	1.8	I	External indication of wait
		Sys_ndmareq1	1		I	External DMA request 1 (system expansion). Level (active low) or edge (falling) selectable.
		GPIO_65	4		IO	General-purpose IO 65
		Safe_mode	7			
B2_A43	W2	GPMC_CLK	0	1.8	O	GPMC clock
		GPIO_59	4		IO	General-purpose IO 59
		Safe_mode	7			
B2_A44	D2	GPMC_nCS3	0	1.8	O	GPMC Chip Select bit 3
		Sys_ndmareq0	1		I	External DMA request 0 (system expansion). Level (active low) or edge (falling) selectable.
		GPIO_54	4		IO	General-purpose IO 54
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B2_A45	F4	GPMC_nCS4	0	1.8	O	GPMC Chip Select bit 4
		Sys_ndmareq1	1		I	External DMA request 1 (system expansion). Level (active low) or edge (falling) selectable.
		Mcbsp4_clkx	2		IO	Combined serial clock
		Gpt9_pwm_evt	3		IO	PWM or event for GP timer 9
		GPIO_55	4		IO	General-purpose IO 55
		Safe_mode	7			
B2_A46	G5	GPMC_nCS5	0	1.8	O	GPMC Chip Select bit 5
		Sys_ndmareq2	1		I	External DMA request 2 (system expansion). Level (active low) or edge (falling) selectable.
		Mcbsp4_dr	2		I	Received serial data
		Gpt10_pwm_evt	3		IO	PWM or event for GP timer 10
		GPIO_56	4		IO	General-purpose IO 56
		Safe_mode	7			
B2_A47	F3	GPMC_nCS6	0	1.8	O	GPMC Chip Select bit 6
		Sys_ndmareq3	1		I	External DMA request 3 (system expansion). Level (active low) or edge (falling) selectable.
		Mcbsp4_dx	2		IO	Transmitted serial data
		Gpt11_pwm_evt	3		IO	PWM or event for GP timer 11
		GPIO_57	4		IO	General-purpose IO 57
		Safe_mode	7			
B2_A48	G4	GPMC_nCS7	0	1.8	O	GPMC Chip Select bit 7
		GPMC_IO_dir	1		O	GPMC IO direction control for use with external transceivers
		Mcbsp4_fsx	2		IO	Combined frame synchronization
		Gpt8_pwm_evt	3		IO	PWM or event for GP timer 8
		GPIO_58	4		IO	General-purpose IO 58
		Safe_mode	7			
B2_A49	X	VIO_1V8		1.8	Pwr	Power
B2_A50	X	VMMC1		1.8	Pwr	Power
B2_B1	B22	Cam_xclka	0	1.8	O	Camera Clock Output a
		GPIO_96	4		IO	General-purpose IO 96
		Safe_mode	7			
B2_B2	C22	Cam_xclkb	0	1.8	O	Camera Clock Output b
		GPIO_111	4		IO	General-purpose IO 111
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B2_B3	J23	Cam_d8	0	1.8	I	Camera digital image data bit 8
		GPIO_107	4		IO	General-purpose IO 107
		Safe_mode	7			
B2_B4	K23	Cam_d9	0	1.8	I	Camera digital image data bit 9
		GPIO_108	4		IO	General-purpose IO 108
		Safe_mode	7			
B2_B5	F21	Cam_d10	0	1.8	I	Camera digital image data bit 10
		GPIO_109	4		IO	General-purpose IO 109
		Safe_mode	7			
B2_B6	G21	Cam_d11	0	1.8	I	Camera digital image data bit 11
		GPIO_110	4		IO	General-purpose IO 110
		Safe_mode	7			
B2_B7	J20	Cam_strobe	0	1.8	O	Flash strobe control signal
		GPIO_126	4		IO	General-purpose IO 126
		Safe_mode	7			
B2_B8	H24	Cam_fld	0	1.8	IO	Camera field identification
		Cam_global_reset	2		IO	Global reset is used strobe synchronization
		GPIO_98	4		IO	General-purpose IO 98
		Safe_mode	7			
B2_B9	F18	Cam_wen	0	1.8	I	Camera write enable
		Cam_shutter	2		O	Mechanical shutter control signal
		GPIO_167	4		IO	General-purpose IO 167
		Safe_mode	7			
B2_B10	J19	Cam_pclk	0	1.8	I	Camera pixel clock
		GPIO_97	4		IO	General-purpose IO 97
		Safe_mode	7			
B2_B11	AC19	Dss_data0	0	1.8	IO	LCD Pixel Data bit 0
		Uart1_cts	2		I	UART1 Clear To Send
		GPIO_70	4		IO	General-purpose IO 70
		Safe_mode	7			
B2_B12	AB19	Dss_data1	0	1.8	IO	LCD Pixel Data bit 1
		Uart1_rts	2		O	UART1 Request To Send
		GPIO_71	4		IO	General-purpose IO 71
		Safe_mode	7			
B2_B13	AD20	Dss_data2	0	1.8	IO	LCD Pixel Data bit 2
		GPIO_72	4		IO	General-purpose IO 72
		Safe_mode	7			
B2_B14	AC20	Dss_data3	0	1.8	IO	LCD Pixel Data bit 3
		GPIO_73	4		IO	General-purpose IO 73
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B2_B15	AD21	Dss_data4	0	1.8	IO	LCD Pixel Data bit 4
		Uart3_rx_irrx	2		I	UART3 Receive data, IR and Remote RX
		GPIO_74	4		IO	General-purpose IO 74
		Safe_mode	7			
B2_B16	AC21	Dss_Data5	0	1.8	IO	LCD Pixel Data bit 5
		Uart3_tx_irtx	2		O	UART3 Transmit data, IR TX
		GPIO_75	4		IO	General-purpose IO 75
		Safe_mode	7			
B2_B17	D24	Dss_data6	0	1.8	IO	LCD Pixel Data bit 6
		Uart1_tx	2		O	UART1 Transmit data
		GPIO_76	4		IO	General-purpose IO 76
		Safe_mode	7			
B2_B18	E23	Dss_data7	0	1.8	IO	LCD Pixel Data bit 7
		Uart1_rx	2		I	UART1 Receive data
		GPIO_77	4		IO	General-purpose IO 77
		Safe_mode	7			
B2_B19	E24	Dss_data8	0	1.8	IO	LCD Pixel Data bit 8
		GPIO_78	4		IO	General-purpose IO 78
		Safe_mode	7			
B2_B20	F23	Dss_data9	0	1.8	IO	LCD Pixel Data bit 9
		GPIO_79	4		IO	General-purpose IO 79
		Safe_mode	7			
B2_B21	AC22	Dss_data10	0	1.8	IO	LCD Pixel Data bit 10
		GPIO_80	4		IO	General-purpose IO 80
		Safe_mode	7			
B2_B22	AC23	Dss_data11	0	1.8	IO	LCD Pixel Data bit 11
		GPIO_81	4		IO	General-purpose IO 81
		Safe_mode	7			
B2_B23	AB22	Dss_data12	0	1.8	IO	LCD Pixel Data bit 12
		GPIO_82	4		IO	General-purpose IO 82
		Safe_mode	7			
B2_B24	Y22	Dss_data13	0	1.8	IO	LCD Pixel Data bit 13
		GPIO_83	4		IO	General-purpose IO 83
		Safe_mode	7			
B2_B25	W22	Dss_data14	0	1.8	IO	LCD Pixel Data bit 14
		GPIO_84	4		IO	General-purpose IO 84
		Safe_mode	7			
B2_B26	V22	Dss_data15	0	1.8	IO	LCD Pixel Data bit 15
		GPIO_85	4		IO	General-purpose IO 85
		Safe_mode	7			
B2_B27	J22	Dss_data16	0	1.8	IO	LCD Pixel Data bit 16
		GPIO_86	4		IO	General-purpose IO 86
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B2_B28	G23	Dss_data17	0	1.8	IO	LCD Pixel Data bit 17
		GPIO_87	4		IO	General-purpose IO 87
		Safe_mode	7			
B2_B29	G24	Dss_data18	0	1.8	IO	LCD Pixel Data bit 18
		Mcspi3_clk	2		IO	SPI Clock
		Dss_data0	3		IO	LCD Pixel Data bit 0
		GPIO_88	4		IO	General-purpose IO 88
		Safe_mode	7			
B2_B30	H23	Dss_data19	0	1.8	IO	LCD Pixel Data bit 19
		Mcspi3_simo	2		IO	Slave data in, master data out
		Dss_data1	3		IO	LCD Pixel Data bit 1
		GPIO_89	4		IO	General-purpose IO 89
		Safe_mode	7			
B2_B31	D23	Dss_data20	0	1.8	O	LCD Pixel Data bit 20
		Mcspi3_somi	2		IO	Slave data out, master data in
		Dss_data2	3		IO	LCD Pixel Data bit 2
		GPIO_90	4		IO	General-purpose IO 90
		Safe_mode	7			
B2_B32	K22	Dss_data21	0	1.8	O	LCD Pixel Data bit 21
		Mcspi3_cs0	2		IO	SPI Enable 0, polarity configured by software
		Dss_data3	3		IO	LCD Pixel Data bit 3
		GPIO_91	4		IO	General-purpose IO 91
		Safe_mode	7			
B2_B33	V21	Dss_data22	0	1.8	O	LCD Pixel Data bit 22
		Mcspi3_cs1	2		IO	SPI Enable 1, polarity configured by software
		Dss_data4	3		IO	LCD Pixel Data bit 4
		GPIO_92	4		IO	General-purpose IO 92
		Safe_mode	7			
B2_B34	W21	Dss_data23	0	1.8	O	LCD Pixel Data bit 23
		Dss_data5	3		IO	LCD Pixel Data bit 5
		GPIO_93	4		IO	General-purpose IO 93
		Safe_mode	7			
B2_B35	G22	Dss_pclk	0	1.8	O	LCD Pixel Clock
		GPIO_66	4		IO	General-purpose IO 66
		Safe_mode	7			
B2_B36	E22	Dss_hsync	0	1.8	O	LCD Horizontal Synchronization
		GPIO_67	4		IO	General-purpose IO 67
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B2_B37	F22	Dss_vsync	0	1.8	O	LCD Vertical Synchronization
		GPIO_68	4		IO	General-purpose IO 68
		Safe_mode	7			
B2_B38	J21	Dss_acbias	0	1.8	O	AC bias control (STN) or pixel data enable (TFT) output
		GPIO_69	4		IO	General-purpose IO 69
		Safe_mode	7			
B2_B39	X	MMC1_CD		1.8	IO	GPIO_0/ card detection
B2_B40	AD12	Hsusb2_data1	3	1.8	IO	Dedicated for external transceiver Bidirectional data bus
		Etk_d15	0		O	ETK data 15
		GPIO_29	4		IO	General-purpose IO 29
		Mm2_txse0	5		IO	Single-ended zero. Used as VM in 4-pin VP_VM mode.
		Hsusb2_tll_data1	6		IO	Dedicated for external transceiver Bidirectional data bus
B2_B41	L23	MMC1_cmd	0	1.8	IO	MMC/SD command signal
		GPIO_121	4		IO	General-purpose IO 121
		Safe_mode	7			
B2_B42	M23	MMC1_clk0	0	1.8	O	MMC/SD Output Clock
		GPIO_120	4		IO	General-purpose IO 120
		Safe_mode	7			
B2_B43	M22	MMC1_dat0	0	1.8	IO	MMC/SD Card Data bit 0 / SPI Serial Input
		GPIO_122	4		IO	General-purpose IO 122
		Safe_mode	7			
B2_B44	M21	MMC1_dat1	0	1.8	IO	MMC/SD Card Data bit 1
		GPIO_123	4		IO	General-purpose IO 123
		Safe_mode	7			
B2_B45	M20	MMC1_dat2	0	1.8	IO	MMC/SD Card Data bit 2
		GPIO_124	4		IO	General-purpose IO 124
		Safe_mode	7			
B2_B46	N23	MMC1_dat3	0	1.8	IO	MMC/SD Card Data bit 3
		GPIO_125	4		IO	General-purpose IO 125
		Safe_mode	7			
B2_B47	N22	MMC1_dat4	0	1.8	IO	MMC/SD Card Data bit 4
		GPIO_126	4		IO	General-purpose IO 126
		Safe_mode	7			
B2_B48	N21	MMC1_dat5	0	1.8	IO	MMC/SD Card Data bit 5
		GPIO_127	4		IO	General-purpose IO 127
		Safe_mode	7			

Pin #	Ball #	Pin Name	mode	V	type	description
B2_B49	N20	MMC1_dat6	0	1.8	IO	MMC/SD Card Data bit 6
		GPIO_128	4		IO	General-purpose IO 128
		Safe_mode	7			
B2_B50	P24	MMC1_dat7	0	1.8	IO	MMC/SD Card Data bit 7
		GPIO_129	4		IO	General-purpose IO 129
		Safe_mode	7			

7.1.1 Definitions

X=Pin on other chip than OMAP-3530

(1) The usage of local bus signals are resticted

(2) The local bus address signals can be used as GPIO, in case no ethernet PHY is assembled on the baseboard

1. **MODE:** Multiplexing mode number.
   - Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the pin corresponds to the name of the pin. There is always a function mapped on the primary mode. Notice that primary mode is not necessarily the default mode.
     Note: The default mode is the mode at the release of the reset; also see the RESET REL. MODE column.
   - Modes 1 to 7 are possible modes for alternate functions. On each pin, some modes are effectively used for alternate functions, while some modes are not used and do not correspond to a functional configuration.
2. **TYPE:** Signal direction
   - I = Input
   - O = Output
   - I/O = Input/output
   - D = Open drain
   - DS = Differential
   - A = Analog
   - PWR = Power
   - GND = Ground

   Note: In the safe mode, the buffer is configured in high-impedance.

8 Signal Description

8.1 External Memory Interfaces – GPMC Signals Description

The General Purpose Memory Controller (GPMC) is used to interface external memory devices: such as NOR Flash, NAND Flash, Pseudo SRAM, SRAM or Field programmable Gate Array (FPGA)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
GPMC A1	GPMC output address bit 1	O	B2 – A13
GPMC A2	GPMC output address bit 2	O	B2 – A14
GPMC A3	GPMC output address bit 3	O	B2 – A15
GPMC A4	GPMC output address bit 4	O	B2 – A16
GPMC A5	GPMC output address bit 5	O	B2 – A17
GPMC A6	GPMC output address bit 6	O	B2 – A18
GPMC A7	GPMC output address bit 7	O	B2 – A19
GPMC A8	GPMC output address bit 8	O	B2 – A20
GPMC A9	GPMC output address bit 9	O	B2 – A21
GPMC A10	GPMC output address bit 10	O	B2 – A22
GPMC CLK	GPMC Clock	O	B2 – A43
GPMC D0	GPMC data bit 0	IO	B2 – A23
GPMC D1	GPMC data bit 1	IO	B2 – A24
GPMC D2	GPMC data bit 2	IO	B2 – A25
GPMC D3	GPMC data bit 3	IO	B2 – A26
GPMC D4	GPMC data bit 4	IO	B2 – A27
GPMC D5	GPMC data bit 5	IO	B2 – A28
GPMC D6	GPMC data bit 6	IO	B2 – A29
GPMC D7	GPMC data bit 7	IO	B2 – A30
GPMC D8	GPMC data bit 8	IO	B2 – A31
GPMC D9	GPMC data bit 9	IO	B2 – A32
GPMC D10	GPMC data bit 10	IO	B2 – A33
GPMC D11	GPMC data bit 11	IO	B2 – A34
GPMC D12	GPMC data bit 12	IO	B2 – A35
GPMC D13	GPMC data bit 13	IO	B2 – A36
GPMC D14	GPMC data bit 14	IO	B2 – A37
GPMC D15	GPMC data bit 15	IO	B2 – A38
GPMC_nBE1	Upper Byte Enable	O	B2 – A41
GPMC nCS3	GPMC Chip Select bit 3	O	B2 – A44
GPMC nCS4	GPMC Chip Select bit 4	O	B2 – A45
GPMC nCS5	GPMC Chip Select bit 5	O	B2 – A46
GPMC nCS6	GPMC Chip Select bit 6	O	B2 – A47
GPMC nCS7	GPMC Chip Select bit 7	O	B2 – A48
GPMC nOE	Output Enable	O	B2 – A40
GPMC nWE	Write Enable	O	B2 – A39
GPMC WAIT3	External indication of wait	I	B2 – A42

Note 1: GPMC nCS0 is connected to NAND IC on TAO-3530.

8.2 Video Interfaces –CAM Signals description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
Cam_d0	Camera digital image data bit 0	I	B2 – A1
Cam_d1	Camera digital image data bit 1	I	B2 – A2
Cam_d2	Camera digital image data bit 2	I	B2 – A3
Cam_d3	Camera digital image data bit 3	I	B2 – A4
Cam_d4	Camera digital image data bit 4	I	B2 – A5
Cam_d5	Camera digital image data bit 5	I	B2 – A6
Cam_d6	Camera digital image data bit 6	I	B2 – A7
Cam_d7	Camera digital image data bit 7	I	B2 – A8
Cam_d8	Camera digital image data bit 8	I	B2 – B3
Cam_d9	Camera digital image data bit 9	I	B2 – B4
Cam_d10	Camera digital image data bit 10	I	B2 – B5
Cam_d11	Camera digital image data bit 11	I	B2 – B6
Cam_fld	Camera field identification	IO	B2 – B8
Cam_hs	Camera Horizontal Synchronization	IO	B2 – A9
Cam_pclk	Camera pixel clock	I	B2 – B10
Cam_strobe	Flash strobe control signal	O	B2 – B7
Cam_vs	Camera Vertical Synchronization	IO	B2 – A10
Cam_wen	Camera Write Enable	I	B2 – B9
Cam_xclka	Camera Clock Output a	O	B2 – B1
Cam_xclkb	Camera Clock Output b	O	B2 – B2

The camera ISP can support the following features:

- **Image sensor:**
  - Interface with various image sensors:
    - R, G, B primary colors
    - Ye, Cy, Mg, G complementary colors
  - Support for electronic rolling shutter (ERS) and global-release reset shutters
- **CSI1 serial interface:** The CSI1 receiver is compatible with the MIPI CSI1 specification.
- **MIPI CSI2 serial interface:** The camera ISP supports one MIPI CSI2 serial interface (CSIa) with 2 data lanes. MIPI CSI2 enables data transfer at up to 1.6G bps. It is based on the MIPI CSI2 Specification 1.0.
- **Parallel interface:** The camera parallel interface (CPI) supports two modes:
  - **SYNC mode:** In this mode, the image-sensor module provides horizontal and vertical synchronization signals to the parallel interface, along with the pixel clock. This mode works with 8-, 10-, 11-, and 12-bit data (above 10-bit RAW data, the processing pipe cannot be used; data must be transferred to memory). SYNC mode supports progressive and interlaced image-sensor modules.
  - **ITU mode:** In this mode, the image-sensor module provides an ITU-R BT 656-compatible data stream. The horizontal and vertical synchronization signals are not provided to the interface. Instead, the data stream embeds start-of-active video (SAV) and end-of-active video (EAV) synchronization code. This mode works in 8- and 10-bit configurations

- **Video processing hardware:** The Video processing hardware removes the need for expensive camera modules to perform processing functions. It consists of two parts: front end and back end:
  - **Video processing front end (VPFE)**
  - **Video processing back end (VPBE)**
- **Statistic collection modules (SCM):** The host CPU uses statistics to adjust various parameters for processing image data.
- **Central-resource shared buffer logic (SBL):** Buffers and schedules memory accesses requested by camera ISP modules
- **Circular buffer:** Prevents storage of full image frames in memory when data must be post-processed and/or preprocessed by software
- **Memory management unit (MMU):** Manages virtual-to-physical address translation for external addresses and solves the memory-fragmentation issue. Enables the camera driver to dynamically allocate and de-allocate memory; the MMU handles memory fragmentation.
- **Clock generator:** Generates two independent clocks that can be used by two external image sensors
- **Timing control:**
  - Generation clocks passed to the clock generator
  - Generation of signals for strobe flash, mechanical shutter, and global reset. Support for red-eye removal.
- **Open core protocol (OCP) compliant:**
  - One 64-bit master interface connected to L3
  - One 32-bit slave interface connected to L4
- Parallel Camera Interface (CPI) timing

  The parallel camera interface is a 12-bit interface which can be used in two modes:
  1. SYNC mode: progressive and interlaced image sensor modules for 8-, 10-, 11-, and 12-bit data. The pixel clock can be up to 75 MHz in 12-bit mode. The pixel clock can be up to 130 MHz in 8-bit packed mode.
  2. ITU mode provides an ITU-R BT 656 compatible data stream with progressive image sensor modules only in 8- and 10-bit configurations. The pixel clock can be up to 75 MHz

8.3 Video Interfaces – DSS Signals Description

The display subsystem provides the logic to display a video frame from the memory frame buffer (either SDRAM or SRAM) on a liquid-crystal display (LCD) panel or a TV set.

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
Dss_acbias	AC bias control (STN) or pixel data enable (TFT) output	O	B2 – B38
Dss_data0	LCD Pixel Data bit 0	O	B2 – B11
Dss_data1	LCD Pixel Data bit 1	O	B2 – B12
Dss_data2	LCD Pixel Data bit 2	O	B2 – B13
Dss_data3	LCD Pixel Data bit 3	O	B2 – B14
Dss_data4	LCD Pixel data bit 4	O	B2 – B15
Dss_data5	LCD Pixel Data bit 5	O	B2 – B16
Dss_data6	LCD Pixel Data bit 6	O	B2 – B17
Dss_data7	LCD Pixel Data bit 7	O	B2 – B18
Dss_data8	LCD Pixel Data bit 8	O	B2 – B19
Dss_data9	LCD Pixel Data bit 9	O	B2 – B20
Dss_data10	LCD Pixel Data bit 10	O	B2 – B21
Dss_data11	LCD Pixel Data bit 11	O	B2 – B22
Dss_data12	LCD Pixel Data bit 12	O	B2 – B23
Dss_data13	LCD Pixel Data bit 13	O	B2 – B24
Dss_data14	LCD Pixel Data bit 14	O	B2 – B25
Dss_data15	LCD Pixel Data bit 15	O	B2 – B26
Dss_data16	LCD Pixel Data bit 16	O	B2 – B27
Dss_data17	LCD Pixel Data bit 17	O	B2 – B28
Dss_data18	LCD Pixel Data bit 18	O	B2 – B29
Dss_data19	LCD Pixel Data bit 19	O	B2 – B30
Dss_data20	LCD Pixel Data bit 20	O	B2 – B31
Dss_data21	LCD Pixel Data bit 21	O	B2 – B32
Dss_data22	LCD Pixel Data bit 22	O	B2 – B33
Dss_data23	LCD Pixel Data bit 23	O	B2 – B34
Dss_hsync	LCD Horizontal Synchronization	O	B2 – B36
Dss_pclk	LCD Pixel Clock	O	B2 – B35
Dss_vsync	LCD Vertical Synchronization	O	B2 – B37
DVI_nDISABLE	DVI/ Backlight control	IO	B2 – A11
LCD ENBKL	LCD Backlight Control	IO	B1 – B40
LCD_ENVDD	LCD Voltage On	IO	B1 – A39
LCD_PON	LCD Enable	IO	B2 – A12

The TAO-3530 can easily be connected to a 18 or 24 bit TTL panel by following the following table.

DSS_D	24 bit	18 bit
Dss_data0	B0	B0
Dss_data1	B1	B1
Dss_data2	B2	B2
Dss_data3	B3	B3
Dss_data4	B4	B4
Dss_data5	B5	B5
Dss_data6	B6	G0
Dss_data7	B7	G1
Dss_data8	B0	G2
Dss_data9	G1	G3
Dss_data10	G2	G4
Dss_data11	G3	G5
Dss_data12	G4	R0
Dss_data13	G5	R1
Dss_data14	G6	R2
Dss_data15	G7	R3
Dss_data16	R0	R4
Dss_data17	R1	R5
Dss_data18	R2	
Dss_data19	R3	
Dss_data20	R4	
Dss_data21	R5	
Dss_data22	R6	
Dss_data23	R7	

8.4 Video Interfaces – TV Signals Description

The video encoder converts RGB video signals to conform to the NTSC/PAL standard analog video. The video encoder includes an integrated synchronization signal generator and a 2-channel video digital-to-analog converter (DAC) with video amplifiers, data manager, luma stage, chroma stage, modulator, and a control interface.

The output data to the TV set are the analog composite data from the video DAC stage. The following video standards are supported:

- NTSC-J, M
- PAL-B, D, G, H, I
- PAL-M

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
tv_out1	TV analog output Composite: tv_out1	AO	B1 – B49
tv_out2	TV analog output S-VIDEO: tv_out2	AO	B1 – B50

8.5 Serial Communication Interfaces – I²C Signals Description

The device contains multimaster high-speed (HS) inter-integrated circuit (I2C) ™ controllers), each of which provides an interface between a local host (LH), such as the microprocessor unit (MPU) subsystem, and any I2C-bus-compatible device that connects through the I2C serial bus. External components attached to the I2C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I2C interface.
Each HS I2C controller can be configured to act like a slave or master I2C-compatible device.

INTER-INTEGRATED CIRCUIT INTERFACE (I2C2)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
I2C2_SCL	I2C Master Serial clock. Output is open drain	IOD	B1 – B14
I2C2_SDA	I2C Serial Bidirectional Data. Output is open drain.	IOD	B1 – B13

Note: These signals have a 4.7kΩ pull up resistor to 1.8 V

INTER-INTEGRATED CIRCUIT INTERFACE (I2C3)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
I2C3_SCL	I2C Master Serial clock. Output is open drain	OD	B1 – B12
I2C3_SDA	I2C Serial Bidirectional Data. Output is open drain.	IOD	B1 – B11

Note: These signals have a 4.7kΩ pull up resistor to 1.8 V

8.6 Serial Communication Interfaces – McBSP LP Signals Description

The multichannel buffered serial port (McBSP) provides a full-duplex direct serial interface between the device and other devices in a system such as other application chips (digital base band), audio and voice codec, etc. Because of its high level of versatility, it can accommodate to a wide range of peripherals and clocked frame oriented protocols.

MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 3)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
Mcbsp3_clkx	Combined serial clock	IO	B1 – A4
Mcbsp3_dr	Received serial data	I	B1 – A2
Mcbsp3_dx	Transmitted serial data	IO	B1 – A3
Mcbsp3_fsx	Combined frame synchronization	IO	B1 – A1

8.7 Serial Communication Interfaces – McSPI Signals Description

The multichannel serial port interface (McSPI) is a master/slave synchronous serial bus. The McSPI modules differ as follows: SPI1 supports up to four peripherals, SPI3 supports up to two peripherals and SPI4 supports only one peripheral
The McSPI instances include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths ranging from 4 bits to 32 bits
- Up to four master channels or single channel in slave mode
- Master multichannel mode:
    - Full duplex/half duplex
    - Transmit-only/receive-only/transmit-and-receive modes
    - Flexible I/O port controls per channel
    - Two direct memory access (DMA) requests (read/write) per channel
- Single interrupt line for multiple interrupt source events
- Power management through wake-up capabilities
- Enable the addition of a programmable start-bit for SPI transfer per channel (start-bit mode)
- Support start-bit write command
- Support start-bit pause and break sequence
- 64 bytes built-in FIFO available for a single channel
- Force CS mode for continuous transfers

MULTICHANNEL SERIAL PORT INTERFACE (McSPI1)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
Mcspi1_clk	SPI Clock	IO	B1 – B5
Mcspi1_simo	Slave data in, master data out	IO	B1 – B3
Mcspi1_somi	Slave data out, master data in	IO	B1 – B4
Mcspi1_cs0	SPI Enable 0, polarity configured by software	IO	B1 – B6

MULTICHANNEL SERIAL PORT INTERFACE (McSPI3)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
Mcspi3_clk	SPI Clock	IO	B1 – B20
Mcspi3_simo	Slave data in, master data out	IO	B1 – B17
Mcspi3_somi	Slave data out, master data in	IO	B1 – B18
Mcspi3_cs0	SPI Enable 0, polarity configured by software	IO	B1 – B19
Mcspi3_cs1	SPI Enable 1, polarity configured by software	O	B1 – B24

MULTICHANNEL SERIAL PORT INTERFACE (McSPI4)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
Mcspi4_clk	SPI Clock	IO	B1 – A14
Mcspi4_simo	Slave data in, master data out	IO	B1 – A15
Mcspi4_somi	Slave data out, master data in	IO	B1 – A16
Mcspi4_cs0	SPI Enable 0, polarity configured by software	IO	B1 – A17

8.8 Serial Communication Interfaces – UARTs Signals Description

The module contains two universal asynchronous receiver/transmitter (UART) devices controlled by the microprocessor unit (MPU):

- UART1 is pinned out for use as UART devices only.
- UART3, which adds infrared communication support, is pinned out for use as a UART, infrared data association (IrDA), or consumer infrared (CIR) device, and can be programmed to any available operating mode.

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART1)

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
Uart1_cts	UART1 Clear To Send	I	B1 – A37
Uart1_rts	UART1 Request To Send	O	B1 – A36
Uart1_rx	UART1 Receive data	I	B1 – A35
Uart1_tx	UART1 Transmit data	O	B1 – A34

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART2)

Multiplex option instead of McBSP3 Signals

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
Uart2_cts	UART2 Clear To Send	I	B1 – A3
Uart2_rts	UART2 Request To Send	O	B1 – A2
Uart2_rx	UART2 Receive data	I	B1 – A1
Uart2_tx	UART2 Transmit data	O	B1 – A4

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART3) / IrDA

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
Uart3_cts_rctx	UART3 Clear To Send (input), Remote TX (output)	IO	B1 – A11
Uart3_rts_sd	UART3 Request To Send, IR enable	O	B1 – A10
Uart3_rx_irrx	UART3 Receive data, IR and Remote RX	I	B1 – A12
Uart3_tx_irtx	UART3 Transmit data, IR TX	O	B1 – A13

8.9 Serial Communication Interfaces – USB Signals Description

The high-speed universal serial bus (USB) host subsystem is composed of the high-speed multiport USB host controller and the USBTLL module.
The USB controller is a high-speed multiport USB2.0 host controller.

The EHCI controller is based on the *Enhanced Host Controller Interface (EHCI) specification for USB Release 1.0*, is in charge of high-speed traffic (480M bit/s), over the ULPI/UTMI interface

Note1: USB 1.1 devices can be connected to the USB 2.0 host port only through a USB 2.0 hub.

Note2: Single USB 1.1 devices can be connected directly to the USB OTG port. This port should however during boot up always be kept in OTG mode.

Note3: It's not advisable to connect a hub to the USB OTG port.

Note4: ESD decoupling circuits are advised on all USB devices and ports.

USB Host

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
HOST nOC	HOST nOC	IO	B1 – B41
HSUSB2_CLK	Dedicated for external transceiver 60-MHz clock input to PHY	O	B1 – B27
HSUSB2_Data0	Dedicated for external transceiver Bidirectional data bus	IO	B1 – B31
HSUSB2_Data1	Dedicated for external transceiver Bidirectional data bus	IO	B2 – B40
HSUSB2_Data2	Dedicated for external transceiver Bidirectional data bus	IO	B1 – B7
HSUSB2_Data3	Dedicated for external transceiver Bidirectional data bus	IO	B1 – A8
HSUSB2_data4	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	B1 – A7
HSUSB2_data5	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	B1 – A6
HSUSB2_Data6	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	B1 – A9
HSUSB2_Data7	Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation	IO	B1 – A5
HSUSB2_DIR	Dedicated for external transceiver Data direction control from PHY	I	B1 – B29
HSUSB2_NXT	Dedicated for external transceiver Next signal from PHY	I	B1 – B30
HSUSB2_STP	Dedicated for external transceiver Stop signal	O	B1 – B28

The USB OTG is connected to the TPS65930 USB Transceiver

The TPS65930 device includes a USB OTG transceiver that supports USB 480 Mbps HS, 12 Mbps full-speed (FS), and USB 1.5 Mbps low-speed (LS) through a 4-pin ULPI.

The device has a USB OTG transceiver that allows system implementation that complies with the following specifications:

- Universal Serial Bus 2.0 Specification
- On-The-Go Supplement to the USB 2.0 Specification
- UTMI+ Low Pin Interface Specification

USB OTG

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
HSUSB_DN	USB data N/USB carkit transmit data	IO	B1 – A42
HSUSB_DP	USB data P/USB carkit receive data	IO	B1 – A43
HSUSB_ID	USB ID	IO	B1 – B39
VBUS_5V0	Power	PWR	B1 – A40

Note: It is advised to use USB OTG only for USB OTG

8.10 Removable Media Interfaces – MMC/ SDIO Signals

The multimedia card high-speed/SD/SD I/O (MMC/SD/SDIO) host controller provides an interface between a local host (LH) such as a microprocessor unit (MPU) or digital signal processor (DSP) and either MMC, SD memory cards, or SDIO cards and handles MMC/SD/SDIO transactions with minimal LH intervention.
The application interface manages transaction semantics. The MMC/SD/SDIO host controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRC), start/end bit, and checking for syntactical correctness.
The application interface can send every MMC/SD/SDIO command and either poll for the status of the adapter or wait for an interrupt request, which is sent back in case of exceptions or to warn of end of operation.
The application interface can read card responses or flag registers. It can also mask individual interrupt sources. All these operations can be performed by reading and writing control registers. The MMC/SD/SDIO host controller also supports two DMA channels.

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
MMC1 CD	GPIO0: Card Detection1	IO	B2 – B39
MMC1 CLK0	MMC/SD Output Clock	O	B2 – B42
MMC1 CMD	MMC/SD command signal	IO	B2 – B41
MMC1 DAT0	MMC/SD Card Data bit 0 / SPI Serial Input	IO	B2 – B43
MMC1 DAT1	MMC/SD Card Data bit 1	IO	B2 – B44
MMC1 DAT2	MMC/SD Card Data bit 2	IO	B2 – B45
MMC1 DAT3	MMC/SD Card Data bit 3	IO	B2 – B46
MMC1 DAT3	MMC/SD Card Data bit 4	IO	B2 – B47
MMC1 DAT3	MMC/SD Card Data bit 5	IO	B2 – B48
MMC1 DAT3	MMC/SD Card Data bit 6	IO	B2 – B49
MMC1 DAT3	MMC/SD Card Data bit 7	IO	B2 – B50
MMC1 WP	MMC Write Protect	IO	B1 – B25
VMMC1	Power 1V8/ 3V3	O	B2 – A50

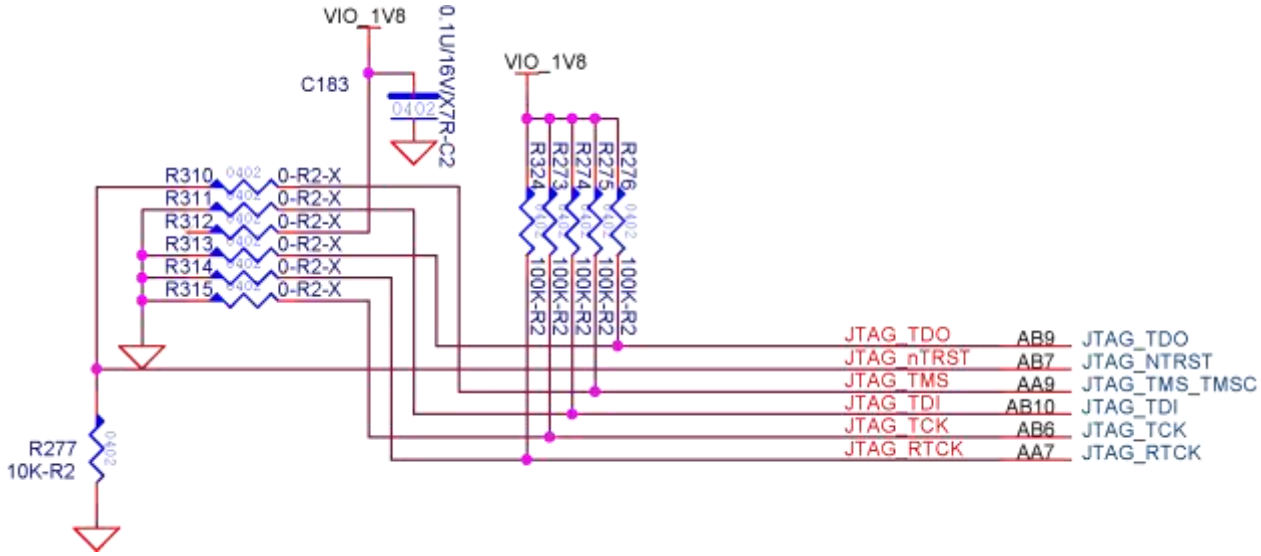
8.11 General Purpose IOs Signals Description

By using Multiplexing a maximum of **139 pins** on the module can be turned into GPIOs. By default the following GPIOs are already acting as GPIO as first function and do not need any software configuration.

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
GPIO 12	General-purpose IO 12	IO	B1 – B15
GPIO 13	General-purpose IO 13	IO	B1 – B16
GPIO 18	General-purpose IO 18	IO	B1 – B21
GPIO 19	General-purpose IO 19	IO	B1 – B22
GPIO 20	General-purpose IO 20	IO	B1 – B23
GPIO 22	General-purpose IO 22	IO	B1 – B26
GPIO_137	General-purpose IO 137	IO	B1 – A38
GPIO_162	General-purpose IO 162	IO	B1 – B32

8.12 Test Interfaces – JTAG Signals Description

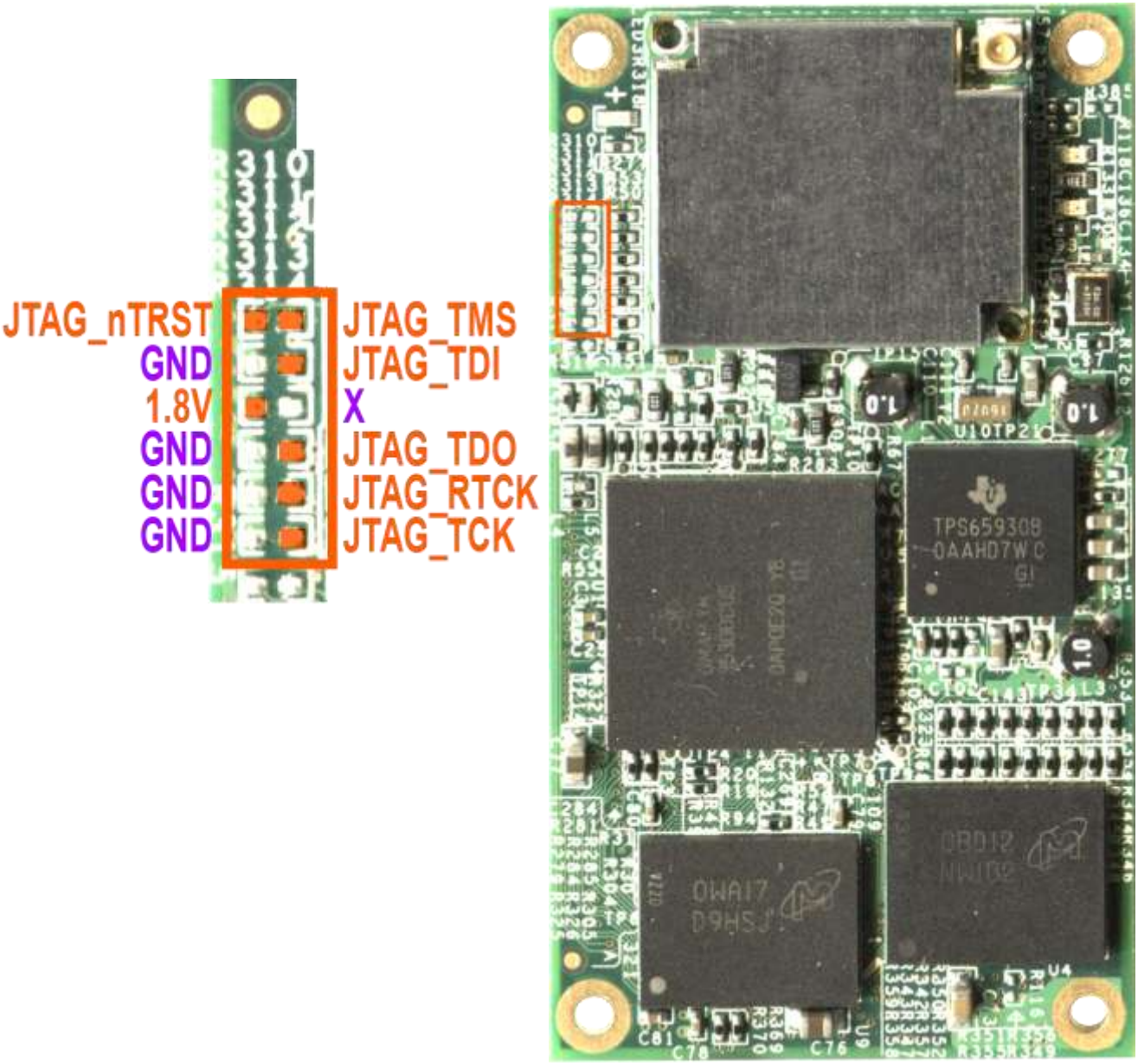
The target debug interface of the device uses the five standard IEEE 1149.1 (JTAG) signals (nTRST, TCK, TMS, TDI, and TDO), a return clock (RTCK) to meet the clocking requirements of the ARM968 processor.



Schematic of the JTAG signals

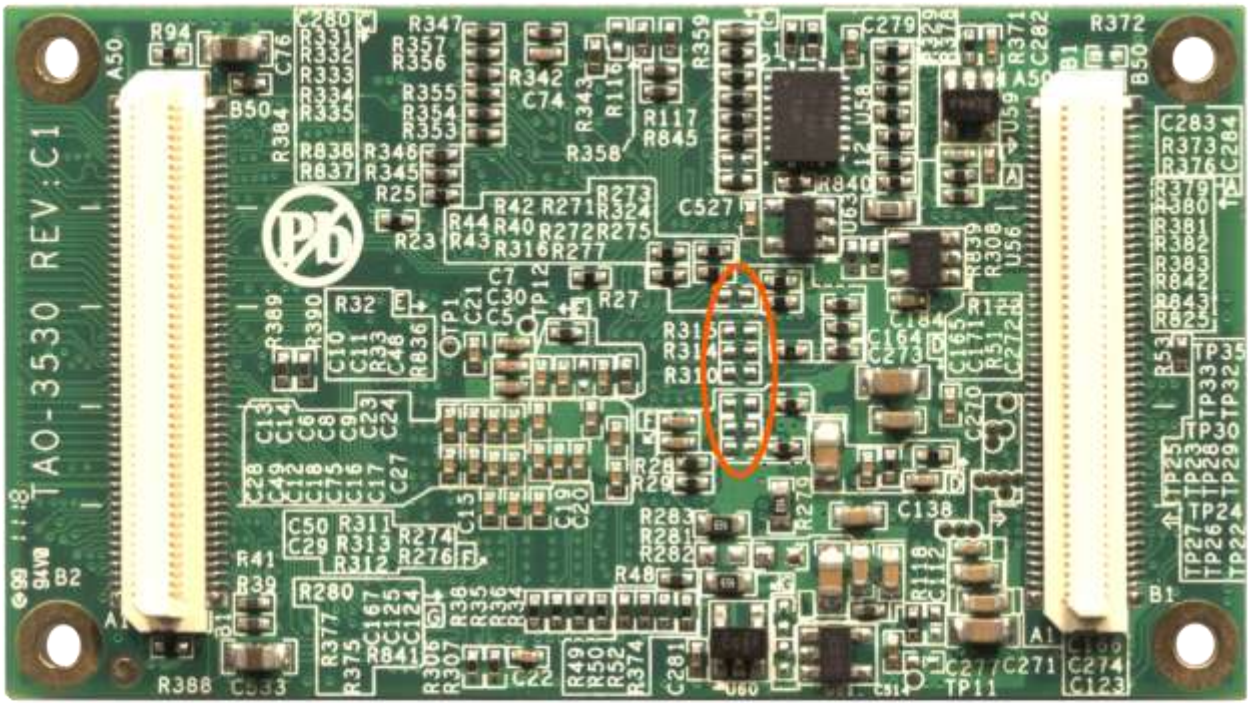
SIGNAL NAME	DESCRIPTION	TYPE
Jtag_ntrst	Test logic reset	I
Jtag_tck	Test Clock	I
Jtag_rtck	Returned Test Clock	O
Jtag_tms_tmsc	Test Mode Select	IO
Jtag_tdi	Test Data Input	I
Jtag_tdo	Test data Output	O

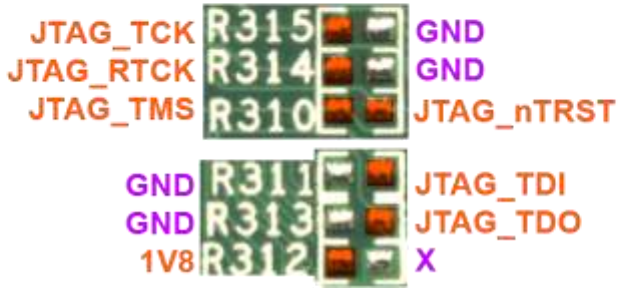
JTAG header in TAO-3530-rev A and rev B



Solder at the orange pads

JTAG header in TAO-3530-rev-C1





See Photo for the location of the solder pads. Solder at the orange pads

8.13 Power Supplies Signals description

Power Supply Signals

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
3.3V	Power 3.3 V (optional)	I	B1 – B1
3.3V	Power 3.3 V (optional)	I	B1 – B2
BKBAT	Backup battery	I	B1 – A23
DC_5V	Power 5V	I	B1 – A41
VBAT	Power 4.2V	I	B1 – A46
VBAT	Power 4.2V	I	B1 – A47
VBAT	Power 4.2V	I	B1 – A48
VBAT	Power 4.2V	I	B1 – A49
VBAT	Power 4.2V	I	B1 – A50
VBUS_5V	Power 5V	I	B1 – A40
VIO_1V8	Power 1V8	O	B1 – B45
VIO_1V8	Power 1V8	O	B1 – B46
VIO_1V8	Power 1V8	O	B1 – B47
VIO_1V8	Power 1V8	O	B1 – B48
VIO_1V8	Power 1V8	O	B2 – A49
VMMC1	Power 1V8/ 3V3	O	B2 – A50

Note1: All input 5V signals should be connected to the main 5V input power circuit. There is an acceptable tollerance of +/-5%.

Note2: The output 3V3 signals current is limited and therefore it's advisable to generate 3V3 voltage on the baseboard for optimal operation.

Note3: The 3.3 V input on pin B1-B1 and B1-B2 is mandatory for Rev A modules with Wifi

Ground Signals

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
GND	Power Ground	GND	B1 – A20
GND	Power Ground	GND	B1 – A22
GND	Power Ground	GND	B1 – A24
GND	Power Ground	GND	B1 – A25
GND	Power Ground	GND	B1 – A26
GND	Power Ground	GND	B1 – A27
GND	Power Ground	GND	B1 – A28
GND	Power Ground	GND	B1 – A29
GND	Power Ground	GND	B1 – A30
GND	Power Ground	GND	B1 – A31
GND	Power Ground	GND	B1 – A32
GND	Power Ground	GND	B1 – A33

Note 1: All GND pins must be connected and should not remain not connected .
Note 2: On a custom baseboard. Please connect GND signals to the mounting pose/nuts which are used to lock the module to the baseboard.

8.14 System and Miscellaneous Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
SYS_nRESPWRON	Power On Reset	I	B1 – B35
SYSEN	System enable output	D	B1 – B43

SYS_nRESPWRON will reset the module when pulled low, it will reset OMAP-3530, TPS65930, and WiFi simultaneously.

8.15 Touch Interupt Signal Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
TS_nPEN_IRQ	Touch Interrupt	IO	B1 – B8

8.16 Serial Communcication Interfaces – HDQ/ 1-Wire Signals Description

The HDQ/1-Wire module implements the hardware protocol of the master functions of the Benchmarq HDQ and the Dallas Semiconductor 1-Wire® protocols. These protocols use a single wire for communication between the master (HDQ/1-Wire controller) and the slaves (HDQ/1-Wire external compliant devices).

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
Hdq_SIO	Bidirectional HDQ 1-Wire control and data Interface. Output is open drain.	IOD	B1 – B9

8.17 PWM Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
PWR_ON	Input; detect a control command to start or stop the system	I	B1 – B36

PWM Option on the TPS65930 instead of DVI_nDISABLE & LCD ENBKL

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
PWM1	Pulse width driver	O	B2 – A11
PWM0	Pulse width driver 0	O	B1 –B40

8.18 ADC Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
ADCIN2	General –purpose ADC Input	I	B1 – B34
CHRG STATE	Battery type	IO	B1 – B44

8.19 Analog Audio Signals Description

ANA.MIC Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
Mic_main_M	Main microphone left input (M)	I	B1 – A19
Mic_main_P	Main microphone left input (P)	I	B1 – B37

VMIC BIAS Signals Description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
MIC_BIAS	Analog microphone bias 1	PWR	B1 – A18
MICBIAS_G	Dedicated ground for microphones	GND	B1 – A21

Headset Signals description

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
PreDriv.LEFT	Predriver output left P for external class-D amplifier	O	B1 – A44
PreDriv.RIGHT	Predriver output right P for external class-D amplifier	O	B1 – A45

AUX input Signals Description

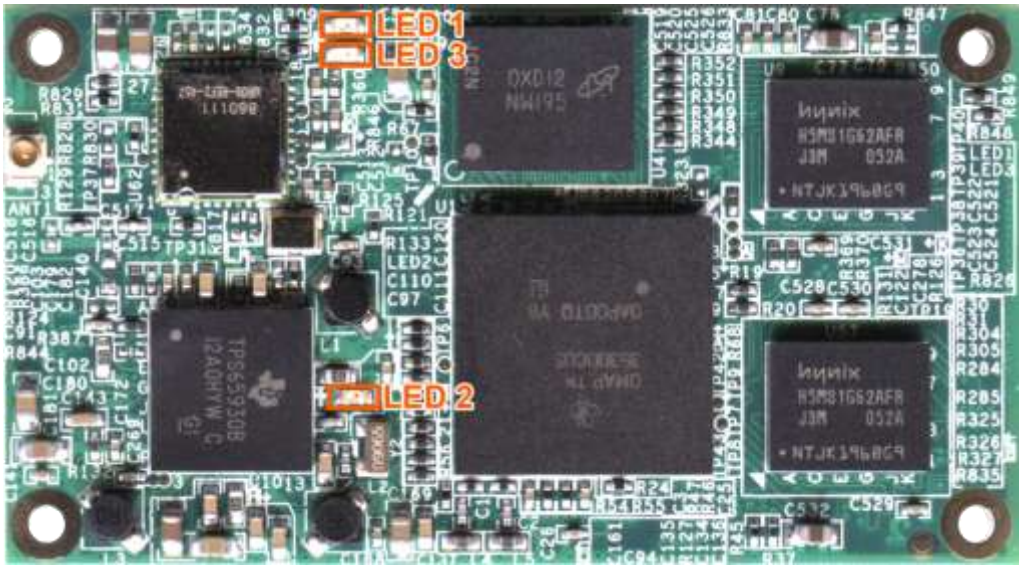
SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
AUXR	Auxiliary audio input right	I	B1 – B38

8.20 LED Signals Description

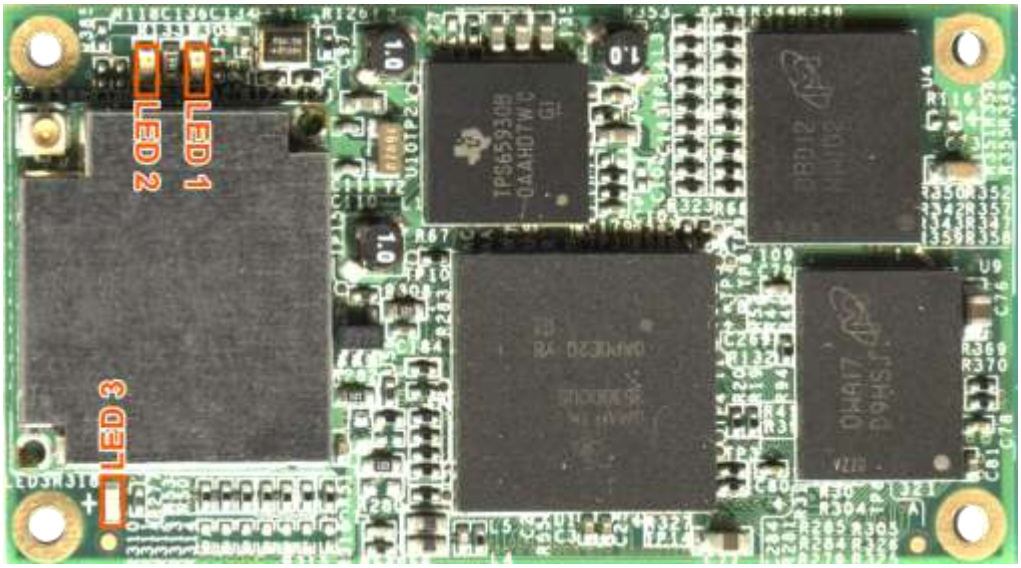
SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
LEDA	User definable LED leg A	D	B1 – B42

The TAO-3530 System on Module contains 3 onboard LEDs with following functions:

LED NAME	DESCRIPTION
LED1	Power ON
LED2	Power: System works
LED3	WiFi: Active



rev C



rev A & B

8.21 Pull-up or Pull-down Signals Description

Pin #	Signal Name	Mode	Voltage	Resistor	Pull up/down
B1 – B11	I2C3_sda	0	1.8	4.7kΩ	Up
	GPIO_185	4			
	Safe mode	7			
B1 – B12	I2C3 SCL	0	1.8	4.7kΩ	Up
	GPIO_184	4			
	safemode	7			
B1 – B13	I2C2 SDA	0	1.8	4.7kΩ	Up
	GPIO_183	4			
	Safe_mode	7			
B1 – B14	I2C2 SCL	0	1.8	4.7kΩ	Up
	GPIO_168	4			
	Safe_mode	7			

8.22 Boot Option

SIGNAL NAME	DESCRIPTION	TYPE	PIN TAO-3530
SYS_BOOT0	1		
SYS_BOOT1	1		
SYS_BOOT2	1		
SYS_BOOT3	1		
SYS_BOOT4	0		
SYS_BOOT5	Boot configuration mode bit 5	I	B1 – B10
SYS_BOOT6	1		

Six external pins (sys_boot[5:0]) are used to select interfaces or devices for booting. The sys_boot[6] pin is used to select whether the internal oscillator is bypassed.
These seven pins are sampled and latched onto the CONTROL.CONTROL_STATUS register after POR.

9 Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Absolute Maximum Ratings						
Vdds	Supply voltage range for 1.8-V I/O macros		-0.5		2.25	V
Vdds_mem	Supply voltage range for 1.8-V I/O macros		-0.5		2.25	V
Vdds_mmc1	Supply voltage range for MMC1 CMD, CLK and DAT[3:0] and for memory stick I/Os	1.8-V mode	-0.5		2.45	V
		3.0-V mode	-0.5		3.50	
Vdda_dac	Supply voltage range for Analog macros		-0.5		2.43	V

PARAMETER			MIN	NOM	MAX	UNIT
Recommended Operating Conditions						
Vdds	Supply voltage range for 1.8-V I/O macros		1.71	1.8	1.91	V
Vdds_mem	Supply voltage range for 1.8-V I/O macros		1.71	1.8	1.89	V
Vdds_mmc1	Supply voltage range for MMC1 CMD, CLK and DAT[3:0] and for memory stick I/Os	1.8-V mode	1.71	1.8	1.89	V
		3.0-V mode	2.7	3.0	3.3	
Vdda_dac	Supply voltage range for Analog macros		1.71	1.8	1.89	V

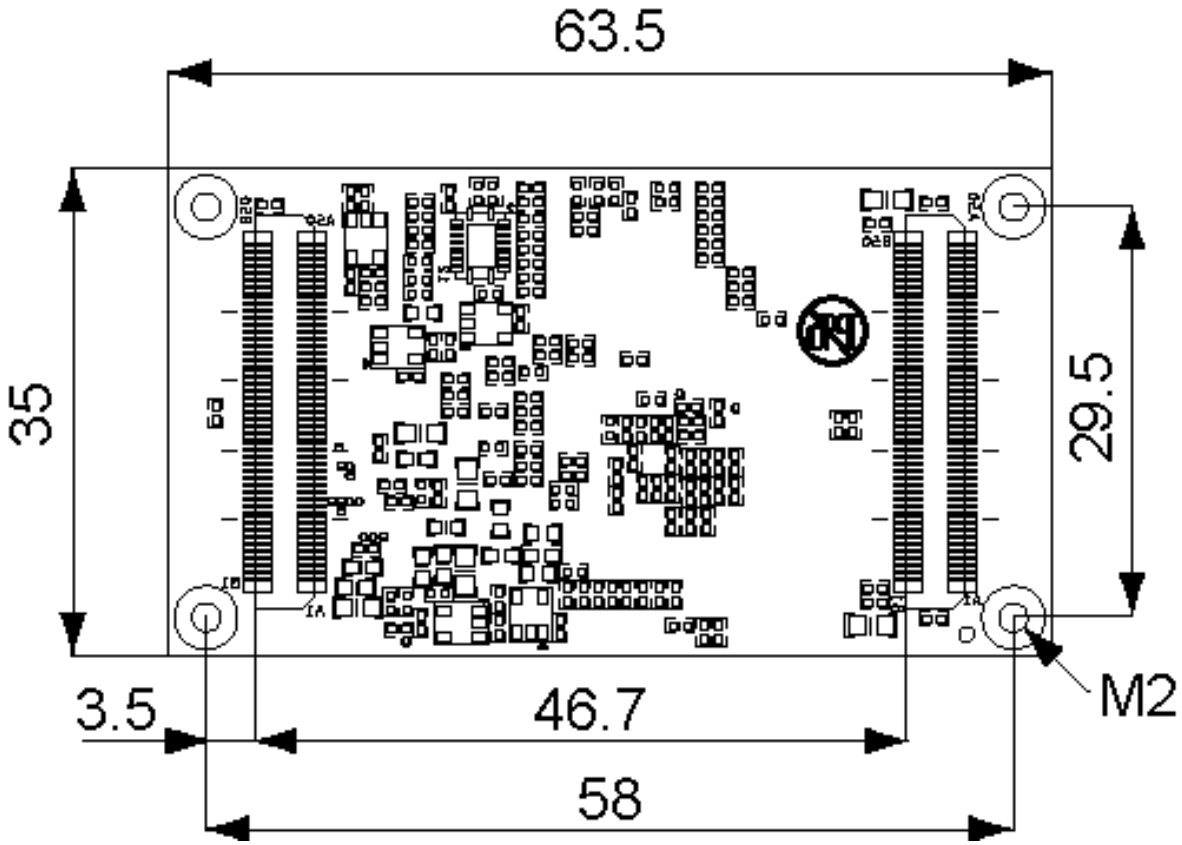
The Supply Voltage to the module is 5V ±5%

10 Environmental Specifications

Temperature	Commercial: 0° to 70° C
	Extended: -20° to 70° C (no WiFi)
	Industrial: -40° to 85° C (no WiFi)
Humidity	10-90%
Dimensions	63.5x 35x 6.4 mm (2 ½ x 1 $^{3}/_{8}$ x ¼ inch)
MTBF	>100,000 hours
Weight	10 grams
Shock	50G / 25ms
Vibration	20G / 0-600 Hz

11 Mechanical Dimensions

11.1 TAO-3530 System on Module Dimensions



Dimensions in mm, tolerance +/- 0.2 mm

Note: 2D (DXF) and 3D(STEP) files are available for download at the Technexion website. (Service and support/ Downloads/ ARM CPU Modules/ TAO-3530)

12 Module Connection

12.1 Module Connector 100 pin NAIS

To mount the TAO-3530 module on the baseboard it isrecommended to use a connector with the following specifications:

- 100 pin NAIS connector
- Mated height 4.5 mm

For example Panasonic AXK5S00247YG

P5KS: Mated height 4.5mm type

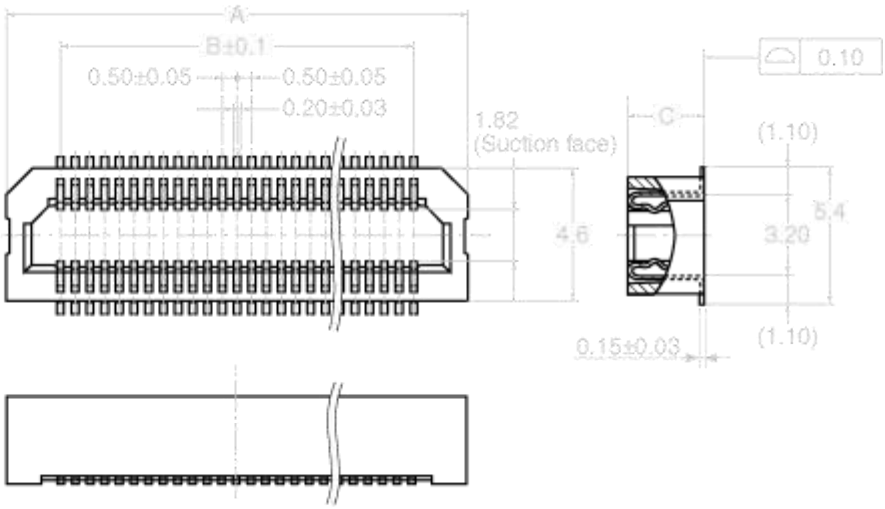
• Socket

CAD Data

Dimension table (mm)

No. of contacts	A	B
100	28.20	24.50

Mated height	C
4.5 mm	3.55

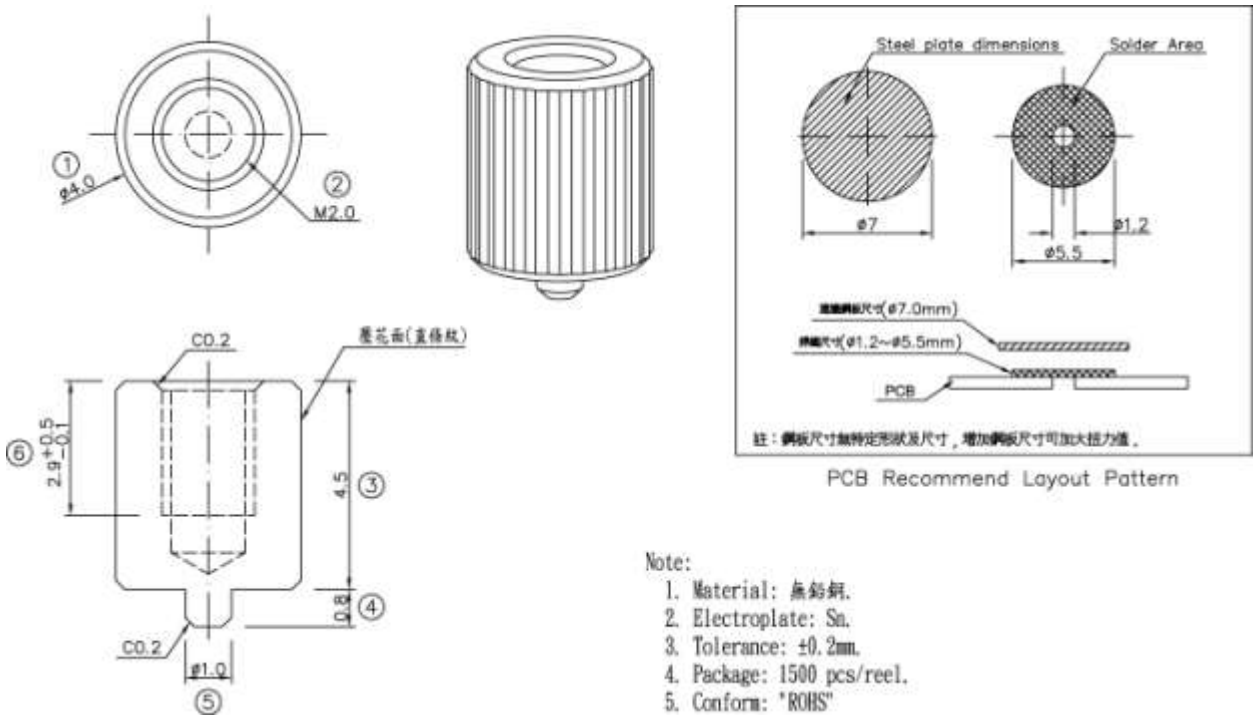


Panasonic Electric Works

General tolerance: ±0.2

If you have difficulty purchasing these parts please contact sales@technexion.com, for assistance.

12.2 Nut to Fix TAO-3530 Module to the Baseboard



Note 1: Always design the above mounting nut/pose on your custom baseboard and fasten the TAO-3530 to ensure a solid connection and counter vibration prone applications.

Note 2: On a custom baseboard always connect the mounting nut/pose to the baseboard general system GND section.

If you have difficulty purchasing these parts please contact sales@technexion.com, for assistance.

13 Disclaimer

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14 Warranty

TechNexion hardware products are warranted against defects in materials and workmanship. If TechNexion receives notice of such defects during the warranty period, TechNexion shall, at its option, either repair or replace hardware products that prove to be defective.

1. **Warranty Period**

   The warranty period shall commence on the invoice date. For TechNexion equipment the standard warranty period shall be two-year parts and labor.

2. **Warranty Coverage**

   2.1 This warranty does not apply to any Products that have been repaired or altered by other than TechNexion authorized service person or, which have been subjected to misuse, abuse, accident, or improper installation. TechNexion assumes no liability as a consequence of such events under the terms of this warranty.

   2.2 This warranty does not cover the damage due to the shipping of the Products and external causes, including accident, abuse, misuse or problems with electrical power, usage not in accordance with product instruction, and problems caused by use of parts and components not supplied by TechNexion upon request.

   2.3 This warranty does not cover any items that are in one or more of the following categories:

   a. Software and/or device drivers,
   b. External devices,
   c. Accessories or parts added to Products after the Products shipped from TechNexion and, Accessories, or parts that are not assembled in TechNexion facilities.
   d. All warranty is voided if the TechNexion warranty label or serial number is removed, illegible, or missing

15 Contact Information

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