Guidelines for Designing EDM Modules and Carrier Boards

Version 0.9-rc3 – Public Preview

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REVISION HISTORY

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1. Introduction

1.1. General Introduction

The EDM (Embedded Design Modules) is a versatile small form factor System on Module definition targeting applications that require low power, low costs and high performance. EDM is the first standard that bridges ARM SOCs and x86 CPU's in a single form factor to offer true scalability.

The EDM modules are typically being used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, booth flash, power sequencing, CPU power supplies, Gigabit Ethernet and display interfaces are concentrated on the module. The modules are used with application specific carrier boards that implement other features such as audio CODECs, touch controllers, sensors and etcetera.

The modular approach offered by the EDM standard gives your project scalability, fast time to market and upgradability while reducing engineering risk and maintain a competitive total cost of ownership.

1.2. Purpose of this Document

This document provides information for designing custom system carrier boards compliant with EDM modules. This design guide provides many examples, implementations and detailed documentation to design custom carrier boards for EDM modules and how to interconnect to additional peripherals and expansion buses.

1. 3. Intended Audience

This specification guideline is intended for electronics engineers and PCB layout engineers designing carrier boards for EDM modules. It is not intended for general audiences.

1.4. Correctness Disclaimer

The EDM consortium reserves the right to make corrections, modifications, enhancements, improvements, and other changes to the specifications at any time. Adaptors should obtain the latest relevant information before placing orders with their EDM module vendor and should verify that such information is current and complete. The EDM consortium assumes no liability for any damages incurred directly or indirectly from any technical or typographical errors or omissions contained herein or for discrepancies between the product and the EDM specification. In no event shall the EDM consortium be liable for any incidental consequential, special, or exemplary damages, whether based on tort, contract or otherwise, arising out of or in connection with the EDM specification or any other information contained herein or the use thereof.

The typical application circuits described in this document may not be suitable for all applications. In particular, additional components may need to be added to these circuits in order to meet specific EMI, EMC or safety isolation requirements. Such regulatory requirements and the techniques for meeting them vary by industry and are beyond the scope of this document.

The EDM consortium has made every attempt to ensure that the information in this document is accurate yet the information contained within is supplied "as-is".

1.5. Intellectual property

The EDM consortium draws attention to the fact that implementing recommendations made in this document could involve the use of one or more patent claims (“IPR”). The consortium takes no position concerning the evidence, validity, or scope of this IPR.

Attention is also drawn to the possibility that some of the elements of this specification could be the subject of unidentified IPR. The consortium is not responsible for identifying any or all such IPR.

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1.7. EDM Name and Logo Usage

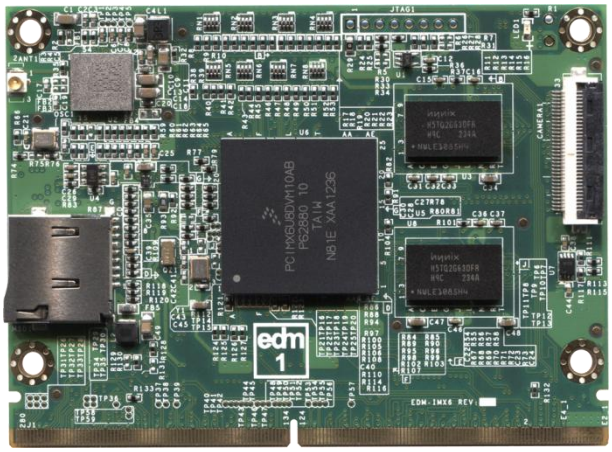
The EDM logo and name usage differs between EDM carrier boards and EDM modules.

1.7.1. EDM Marking Requirements for EDM Modules

Permission to use the EDM logo for EDM modules is only granted to designated members as stipulated on the most recent Membership Privileges document (available upon request at www.edm-standard.org) during the period of time for which their membership dues are paid. Nonmembers must not use the EDM module logo for product marking.

The EDM logo for EDM modules can only be applied to products that are fully compliant to the specifications of the EDM standard, are tested by the EDM consortium and are listed in the compliant product list on the www.edm-standard.org homepage.

Figure 1 - EDM Module Marking Example



Compliant EDM modules should bear a silkscreen printed EDM logo which is applied to the board during fabrication of the circuit board and have a minimum dimension of 6 mm.

Printing of the EDM logo on packaging and/or marketing materials is only permitted if the finished product contains a compliant EDM module

Figure 2 - EDM Module Compliance Marking

EDM Type 1 Compliant	EDM Type 2 Compliant
edm 1	edm 2

1.7.2. EDM Marking for EDM Carrier Boards

The use of the EDM logo on EDM carrier boards is a privilege granted without license to companies, organizations and individuals who believe their products comply with these specifications.

The company, organization or individual that maintains the EDM carrier board is encouraged to publish compliance test reports as part of the documentation covering the specific EDM carrier board.

Members of the EDM consortium can send EDM carrier boards for compliance testing against the latest EDM standards for inclusion on the Compliant EDM carrier boards list on the www.edm-standard.org.

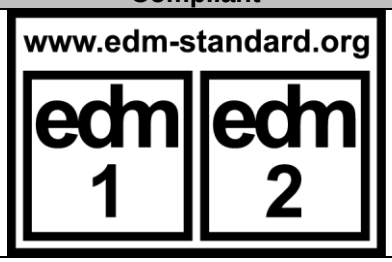
Compliance testing is voluntary and not a requirement to apply the EDM carrier board logo on products.

Figure 3 - EDM Carrier Board Marking Example

The EDM carrier board should bear a silkscreen printed EDM compliance logo which is printed during fabrication of the circuit board and have a minimum dimension of 20 mm by 40 mm and location should be next to the EDM connector where the EDM Module will be assembled.

Printing of the EDM logo on packaging and/or marketing materials is only permitted if the finished product contains a compliant EDM module. For products that are sold without an pre-assembled EDM module. The EDM carrier board logo's can be applied.

Figure 4 - EDM Carrier Board Compliance Marking

EDM Type 1 Compliant	EDM Type 2 Compliant	EDM Type 1 and Type 2 Compliant
		

1.8. EDM Connector

The EDM module utilizes a 314-pin card-edge connector to connect the EDM module. Originally this card-edge connector was designed for MXM graphic modules that are used for PCI Express capable notebook graphics cards. The card-edge connector is also known as a MXM Type III connector.

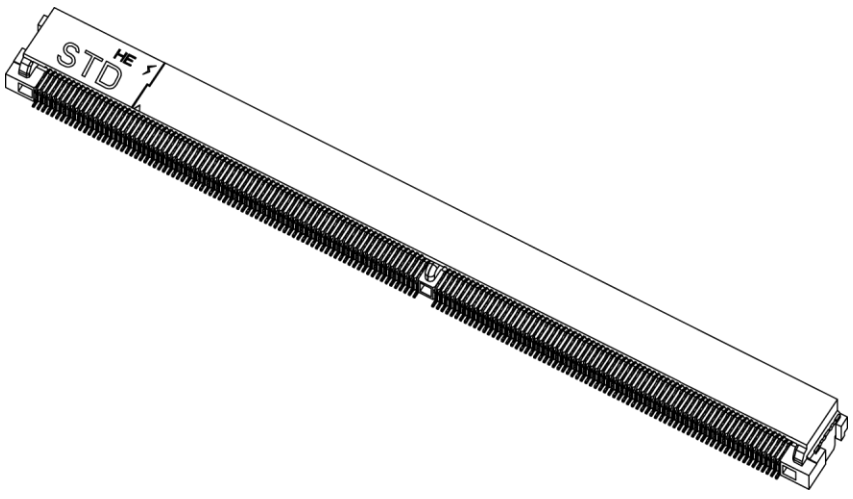
The MXM edge connector is the result of an extensive collaborative design effort with the industry's leading notebook manufacturers and graphic IC design houses. This collaboration has produced a robust, low-cost, vibration resistance edge connector that is capable of handling high-speed serialized signals as is shown in "Table 1 - Environmental characteristics", "Table 2 - Electrical characteristics", "Figure 5 - Differential Insertion Loss", "Figure 6 - Differential Return Loss" and "Figure 7 - Differential Near End Crosstalk" below.

1.8.1. EDM Connector Vendors

The MXM type III connector is produced by multiple connector manufacturers in a wide variety of heights with a maximum stacking height of 11 mm. The following is a partial list of what is offered by a selection of the manufacturers.

For more information about additional variants contact the manufacturer.

Manufacturer	Part Number	Clearance between Module / Carrier Board	Overall height of the connector
Foxconn	AS0B826-S43B-7H	1.5 mm	4.3 mm
Foxconn	AS0B826-S55B-7H	2.7 mm	5.5 mm
Foxconn	AS0B821-S78B-7H	5.0 mm	7.8 mm
Speedtech	B35P101-01111-H	1.56 mm	4.0 mm
Speedtech	B35P101-01121-H	2.76 mm	5.2 mm
Speedtech	B35P101-01131-H	5.06 mm	7.5 mm



1.8.2. EDM Connector Environmental Characteristics

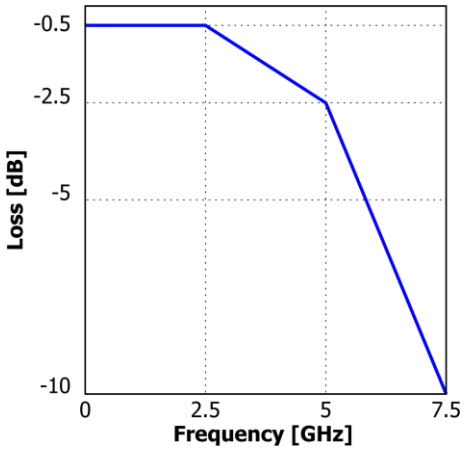
Table 1 - Environmental characteristics

Parameter	Specification
Durability	EIA-364-9 30 cycles
Mating and Unmating Force	EIA-364-13C LIF/angled insertion styled cards: Maximum insertion force: 55 N Maximum extraction force: 60 N Slide-in/side insertion styled cards: Maximum insertion force: 55 N Maximum extraction force: 60 N Note: numbers tabulated using a velocity of 25 mm/min
Vibration	EIA-364-28D - Test condition VII condition D With a 40 x 40 mm block of 100 grams fastened and centered at the GPU center of a Type B PCB
Shock	EIA-364-27B - Test condition A With a 40 x 40 mm block of 100 grams fastened and centered at the GPU center of a Type B PCB

Table 2 - Electrical characteristics

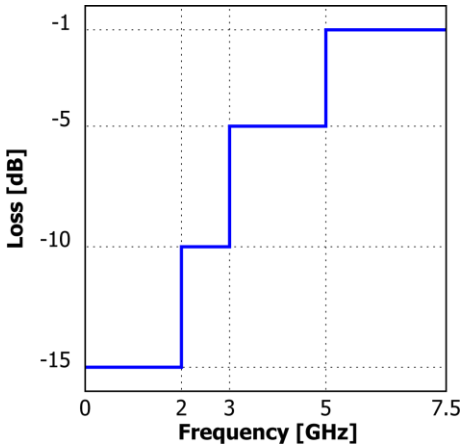
Parameter	Specification
Low Level Contact Resistance	EIA-364-23B 55mΩ MAX
Insulation Resistance	EIA-364-21C Initial testing 250 MΩ. 50 MΩ after other test procedures
Dielectric Withstanding Voltage	EIA-364-20B - Method B on one pair of upper adjacent contacts and on one pair of lower adjacent contacts. Connector is unmated and unmounted. Barometric pressure at sea level. Apply 0.25 KV AC, (50 Hz) for 1 minute. Current leakage 0.5mA MAX
Current Rating	0.5 A per pin MIN
Voltage Rating	50VDC per contact
Differential Impedance	EIA-364-108 85Ω±12.75Ω at Trise=35ps
Differential Insertion Loss	EIA-364-101
Differential Return Loss	EIA-364-108
Differential Near End Crosstalk	EIA-364-90

Figure 5 - Differential Insertion Loss



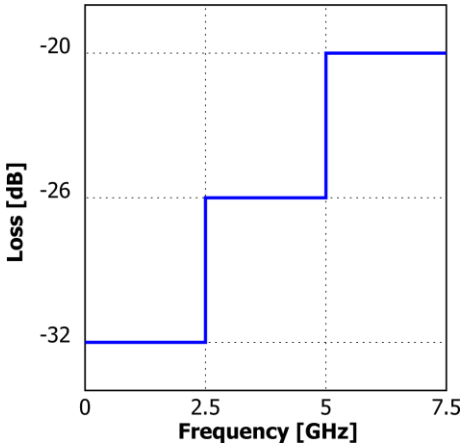
Point	F (Ghz)	Loss (dB)
1	0	-0.5
2	2.5	-0.5
3	5.0	-2.5
4	7.5	-10

Figure 6 - Differential Return Loss



Segment	F (Ghz)	Loss (dB)
1	0-2	-15
2	2-3	-10
3	3-5	-5
4	5-7.5	-1

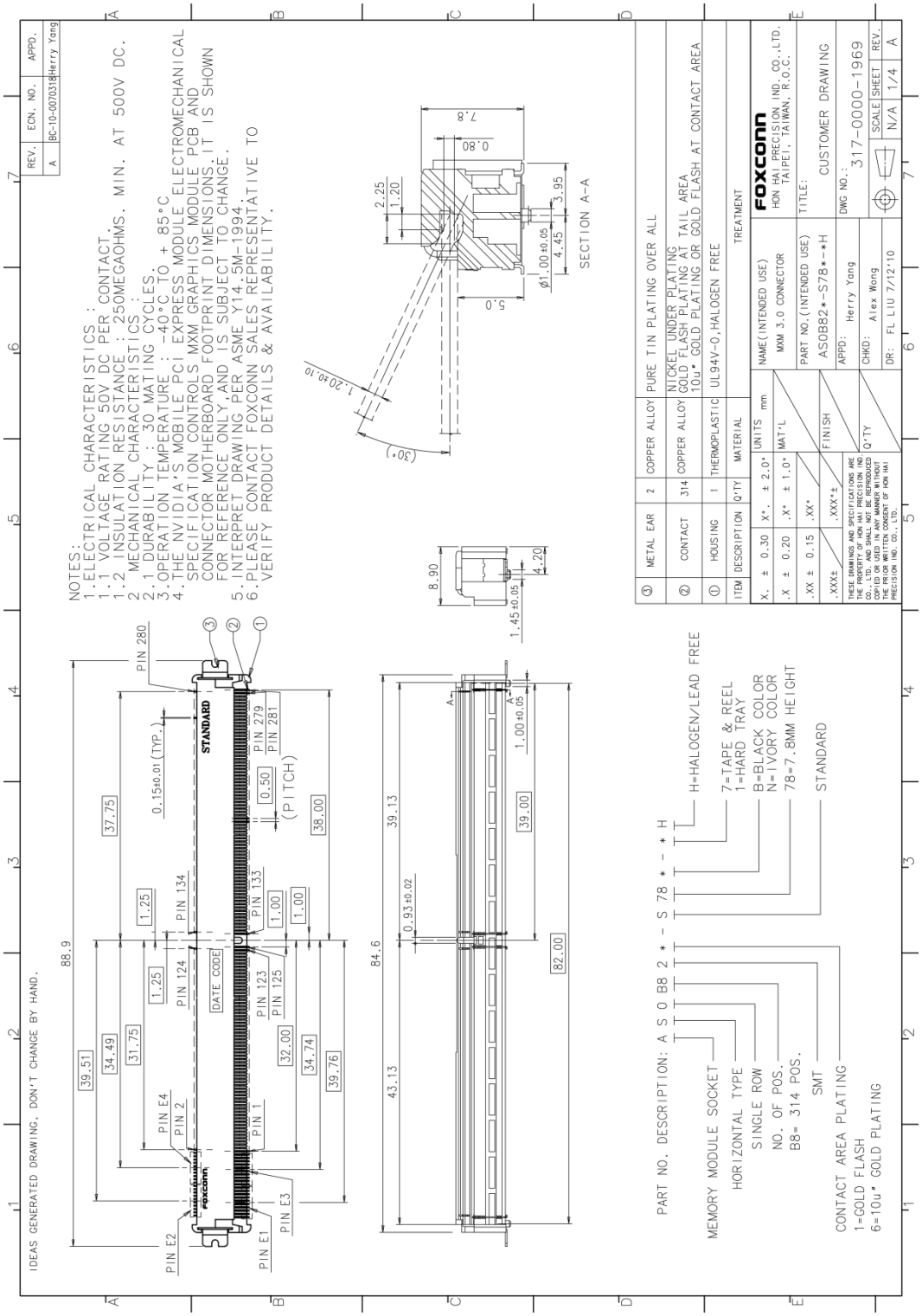
Figure 7 - Differential Near End Crosstalk



Segment	F (Ghz)	Loss (dB)
1	0-2.5	-32
2	2.5-5	-26
3	5-7.5	-20

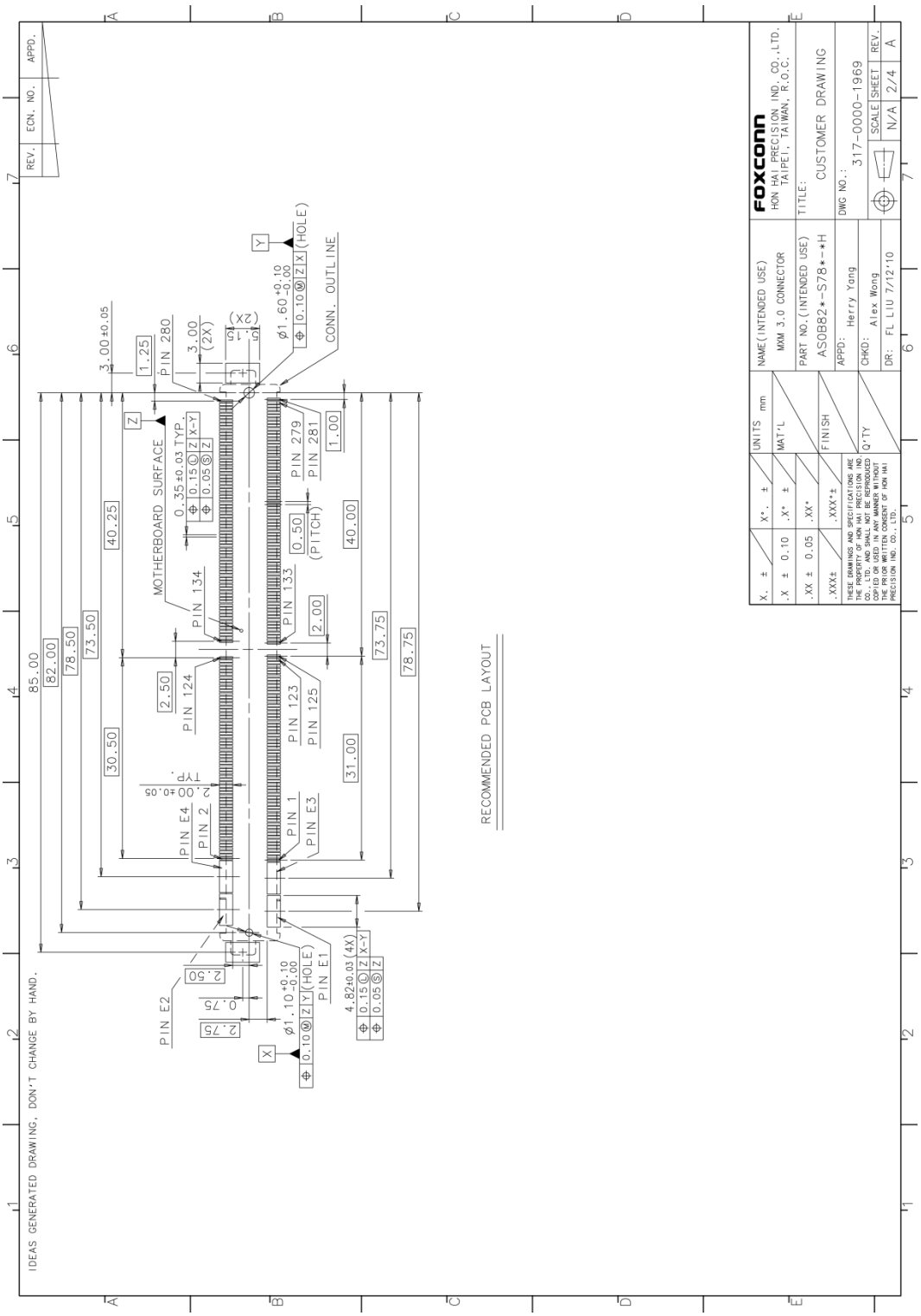
1.9. EDM Connector Details

Figure 8 - EDM Connector Details



1.10. EDM Connector PCB footprint

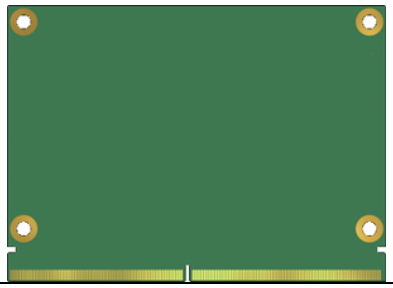
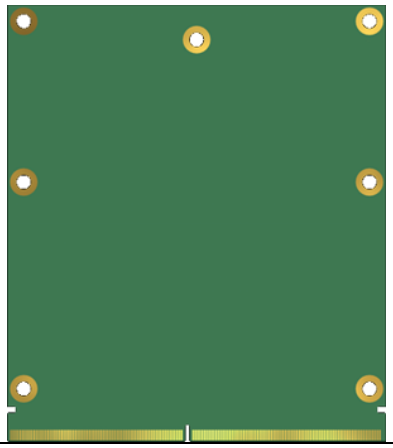
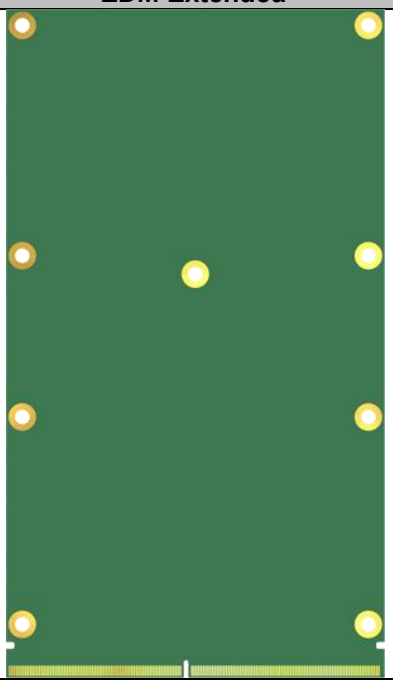
Figure 9 - EDM Connector PCB footprint



1.11. EDM Form Factor and Dimensions

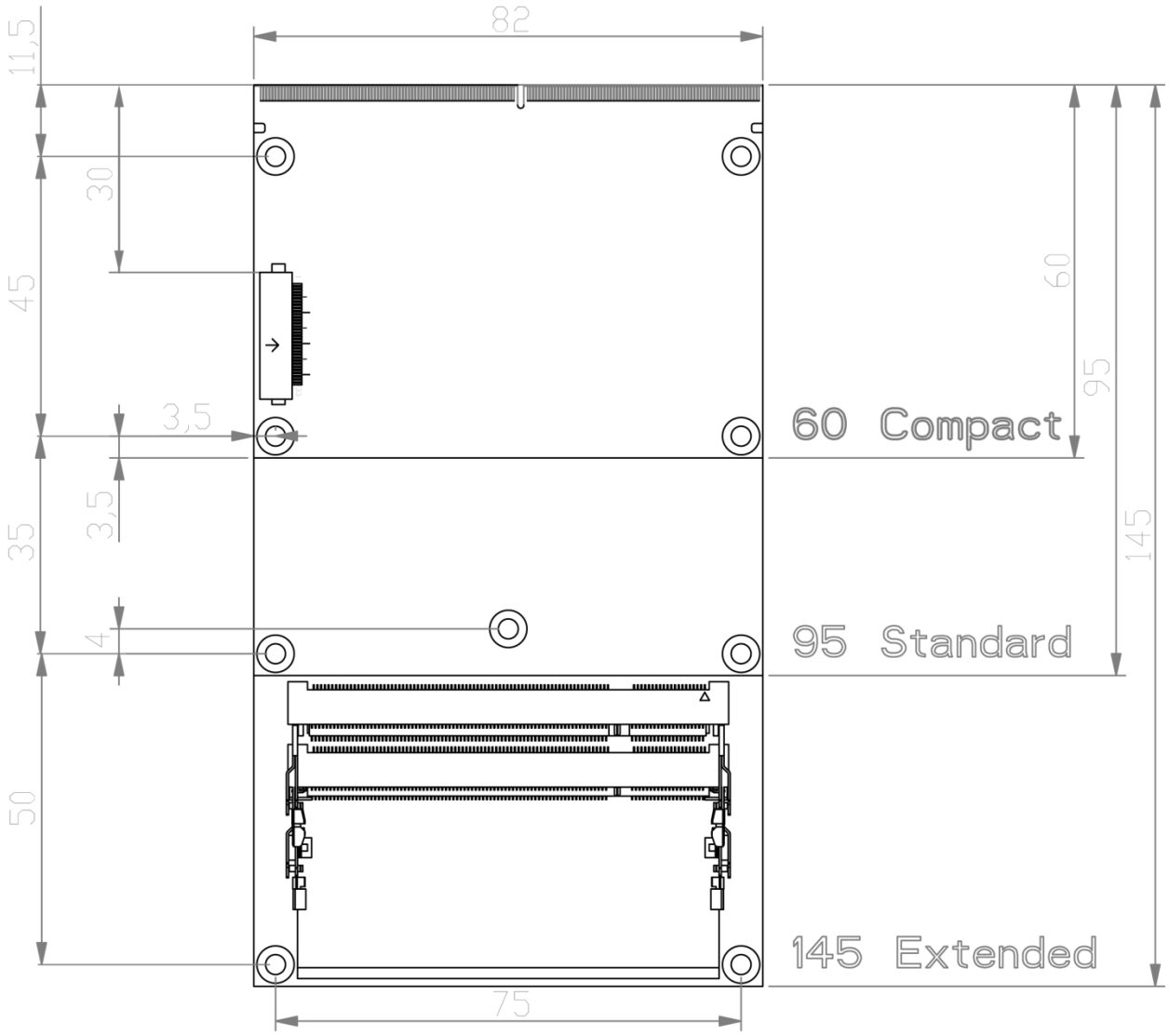
The EDM specification describes 3 different size EDM modules. EDM Compact (82x60mm), EDM Standard (82x95mm) and EDM Extended (82x145mm).

Figure 10 - EDM Module Form Factor and Dimensions

EDM Compact	EDM Standard	EDM Extended
		
82 mm * 60 mm	82 mm * 95 mm	82 mm * 145 mm

1.12. EDM Module Mechanical Dimensions

Figure 11 - EDM Module Mechanical Dimensions



1.13. EDM Heatspreader

An important factor for system integration is thermal design. The heatspreader acts as a thermal coupling device to the Module. Usually a 2mm thick aluminum or copper plate is used.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some Modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the Module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the Module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

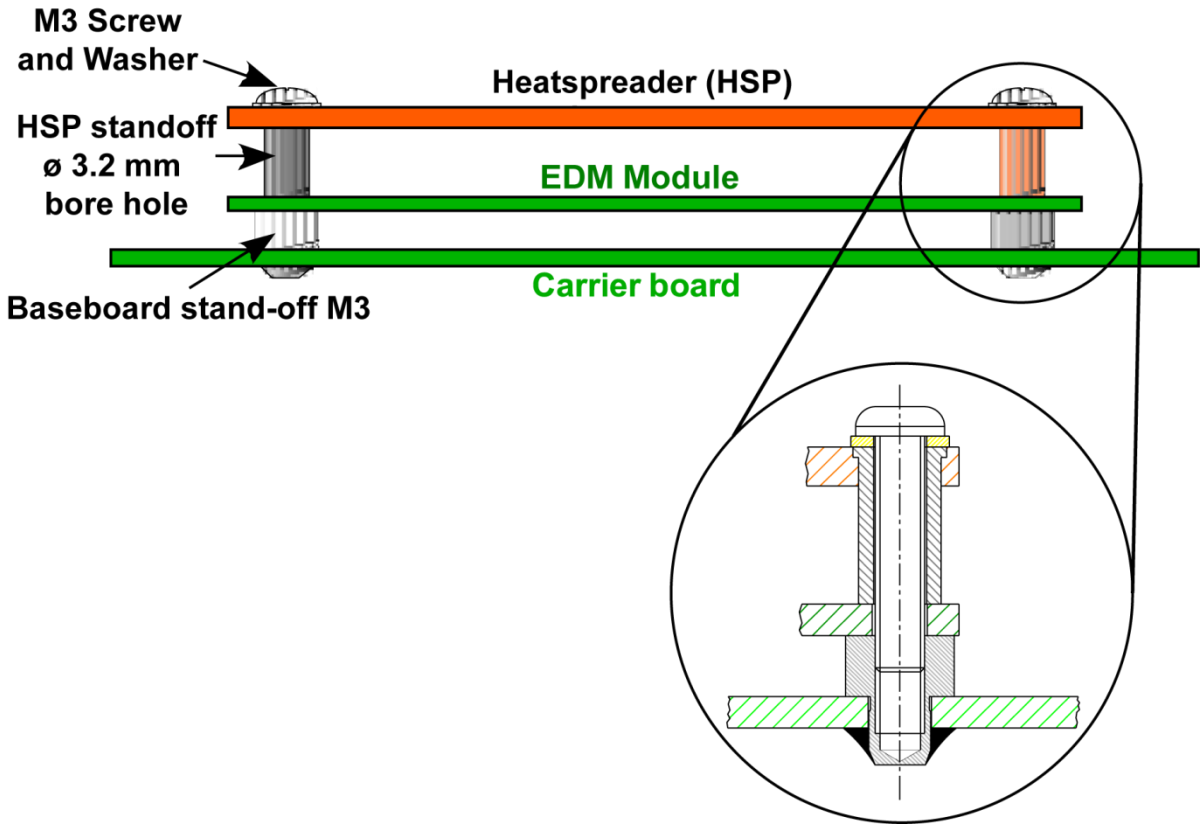
The main mechanical mounting solutions for systems based on EDM modules have proven to be the 'top-mounting' and 'bottom-mounting' solutions. The decision as to which solution will be used is determined by the mechanical construction and the cooling solution of the customer's system. There are two variants of the heatspreader, one for each mounting possibility. One version has threaded standoffs and the other has non-threaded standoffs (bore hole). The following sections describe these two common mounting possibilities and the additional components (standoffs, screws, etc...) that are necessary to implement the respective solution.

1.13.1. Top Mounting

For top mounting heatspreaders with non-threaded standoffs (bore hole) are used.

This variant of the heatspreader was designed to be used in a system where the heatspreader screws need to be inserted from the top side of the complete assembly. In this case the threads for securing the screws are in the carrier board's standoffs. This is the reason why the heatspreader must have non-threaded (bore hole) standoffs.

Figure 12 - Complete assembly using non-threaded (bore hole) heatspreader



Note: The torque specification for heatspreader screws is 0.5 Nm.

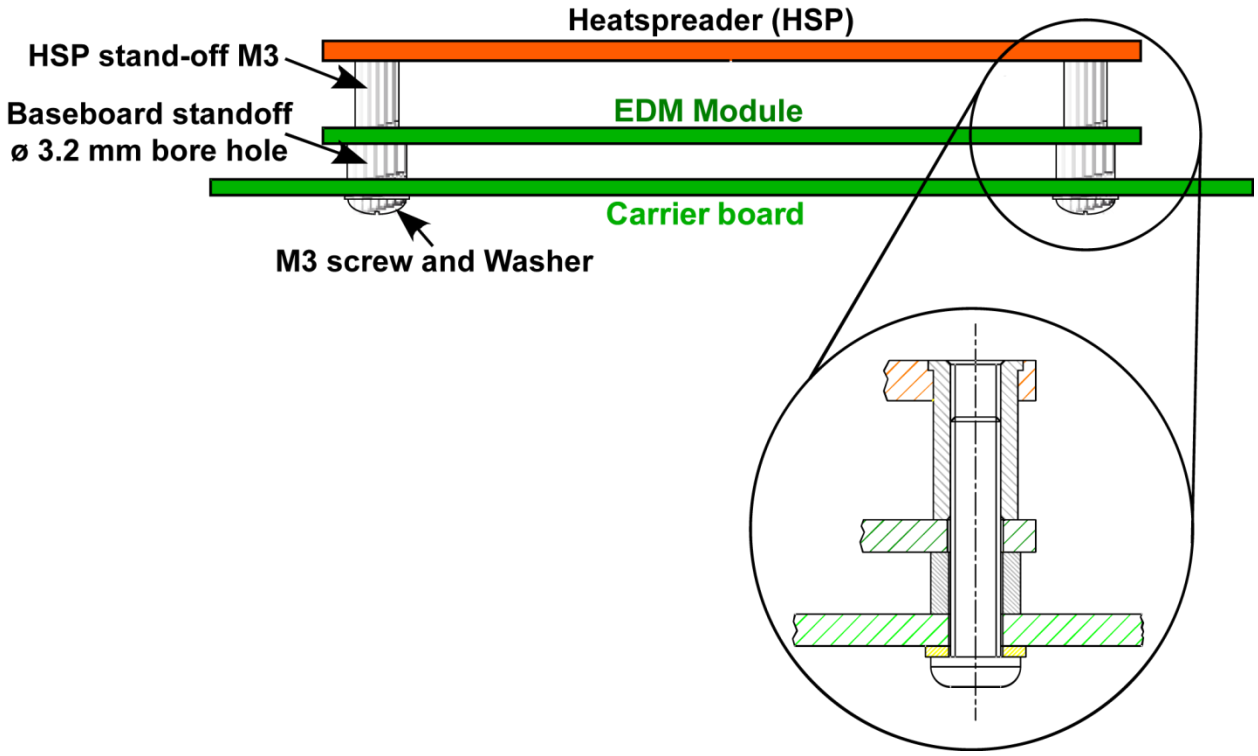
Caution: Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

1.13.2. Bottom Mounting

Heatspreaders with threaded standoffs are used for bottom-mounting solutions.

This variant of the heatspreader has been designed to be used in systems where the heatspreader screws need to be inserted from the bottom side of the complete assembly. For this solution a heatspreader version with threaded standoffs must be used. In this case, the standoffs used on the carrier board are not threaded.

Figure 13 - Complete assembly using threaded heatspreader

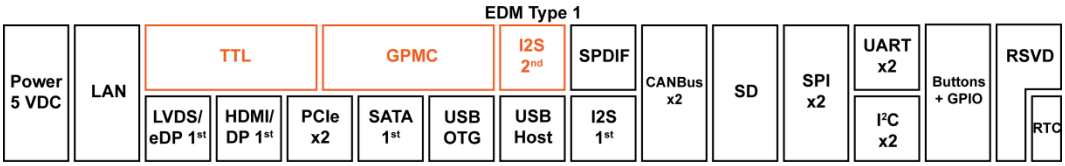


Note: The torque specification for heatspreader screws is 0.5 Nm.

Caution: Do not use a threaded heatspreader together with threaded carrier board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or carrier board.

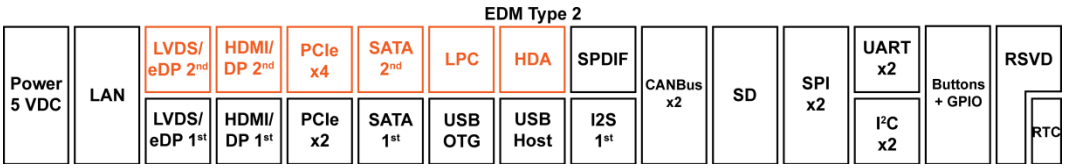
1.14. EDM Interfaces Overview

Figure 14 - EDM Type 1 Overview



EDM type 1 modules are typically used for small compact embedded devices.

Figure 15 - EDM Type 2 Overview



EDM type 2 modules are typically used for multimedia applications that require multiple internal and/or external displays.

For applications that only utilize interfaces that are shared between both EDM types, and where all different signal pins are kept not connected, both EDM type modules could be used in the final product.

2. Connector Pin Assignment

The EDM connector 314 pin assignment for type 1 and type 2 are listed in the table below.

Pin #	EDM	Signal	V	I/O	Description
E1_1	1 / 2	5VSB	5VSB	P	Standby Power Supply 5VDC ± 5%
E2_1	1 / 2	5VSB	5VSB	P	Standby Power Supply 5VDC ± 5%
E1_2	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E2_2	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E1_3	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E2_3	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E1_4	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E2_4	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E1_5	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E2_5	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E1_6	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E2_6	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E1_7	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E2_7	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E1_8	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E2_8	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E1_9	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E2_9	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E1_10	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E2_10	1 / 2	VCC	5V	P	Power Supply 5VDC ± 5%
E3_1	1 / 2	GND	GND	P	Ground
E4_1	1 / 2	GND	GND	P	Ground
E3_2	1 / 2	GBE_MDI2+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 positive signal
E4_2	1 / 2	GBE_MDI0+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 positive signal
E3_3	1 / 2	GBE_MDI2-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 negative signal
E4_3	1 / 2	GBE_MDI0-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 negative signal
E3_4	1 / 2	GND	GND	P	Ground
E4_4	1 / 2	GND	GND	P	Ground
E3_5	1 / 2	GBE_MDI3+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 positive signal
E4_5	1 / 2	GBE_MDI1+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 positive signal
E3_6	1 / 2	GBE_MDI3-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 negative signal
E4_6	1 / 2	GBE_MDI1-	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 negative signal

Pin #	EDM	Signal	V	I/O	Description
E3_7	1 / 2	LED1_ACT	CMOS 3.3V	O	Gigabit Ethernet LED Activity indicator
E4_7	1 / 2	GND	GND	P	Ground
E3_8	1 / 2	GND	GND	P	Ground
E4_8	1 / 2	LED1_nLink100	CMOS 3.3V	O	Gigabit Ethernet 100Mbit/sec LED link indicator
E3_9	1 / 2	LVDS_A0-	LVDS	O	LVDS primary channel differential pair 0 negative signal
		eDP0_LANE0-	eDP	O	Embedded Display Port primary channel differential lane 0 negative signal
E4_9	1 / 2	LED1_nLink1000	CMOS 3.3V	O	Gigabit Ethernet 1000Mbit/sec LED link indicator
E3_10	1 / 2	LVDS_A0+	LVDS	O	LVDS primary channel differential pair 0 positive signal
		eDP0_LANE0+	eDP	O	Embedded Display Port primary channel differential lane 0 positive signal
E4_10	1 / 2	GND	GND	P	Ground
1	1 / 2	GND	GND	P	Ground
2	1	LCD_D0	TTL	O	LCD Pixel Data bit 0
	2	LVDS_B0-	LVDS	O	LVDS secondary channel differential pair 0 negative signal
		eDP1_LANE0-	eDP	O	Embedded Display Port secondary channel differential lane 0 negative signal
3	1 / 2	LVDS_A1-	LVDS	O	LVDS primary channel differential pair 1 negative signal
		eDP0_LANE1-	eDP	O	Embedded Display Port primary channel differential lane 1 negative signal
4	1	LCD_D1	TTL	O	LCD Pixel Data bit 1
	2	LVDS_B0+	LVDS	O	LVDS secondary channel differential pair 0 positive signal
		eDP1_LANE0+	eDP	O	Embedded Display Port secondary channel differential lane 0 positive signal
5	1 / 2	LVDS_A1+	LVDS	O	LVDS primary channel differential pair 1 positive signal
		eDP0_LANE1+	eDP	O	Embedded Display Port primary channel differential lane 1 positive signal
6	1 / 2	GND	GND	P	Ground
7	1 / 2	GND	GND	P	Ground
8	1	LCD_D2	TTL	O	LCD Pixel Data bit 2
	2	LVDS_B1-	LVDS	O	LVDS secondary channel differential pair 1 negative signal
		eDP1_LANE1-	eDP	O	Embedded Display Port secondary channel differential lane 1 negative signal
9	1 / 2	LVDS_A2-	LVDS	O	LVDS primary channel differential pair 2 negative signal
		eDP0_LANE2-	eDP	O	Embedded Display Port primary channel differential lane 2 negative signal

Pin #	EDM	Signal	V	I/O	Description
10	1	LCD_D3	TTL	O	LCD Pixel Data bit 3
	2	LVDS_B1+	LVDS	O	LVDS secondary channel differential pair 1 positive signal
		eDP1_LANE1+	eDP	O	Embedded Display Port secondary channel differential lane 1 positive signal
11	1 / 2	LVDS_A2+	LVDS	O	LVDS primary channel differential pair 2 positive signal
		eDP0_LANE2+	eDP	O	Embedded Display Port primary channel differential lane 2 positive signal
12	1 / 2	GND	GND	P	Ground
13	1 / 2	GND	GND	P	Ground
14	1	LCD_D4	TTL	O	LCD Pixel Data bit 4
	2	LVDS_B2-	LVDS	O	LVDS secondary channel differential pair 2 negative signal
		eDP1_LANE2-	eDP	O	Embedded Display Port secondary channel differential lane 2 negative signal
15	1 / 2	LVDS_A3-	LVDS	O	LVDS primary channel differential pair 3 negative signal
		eDP0_LANE3-	eDP	O	Embedded Display Port primary channel differential lane 3 negative signal
16	1	LCD_D5	TTL	O	LCD Pixel Data bit 5
	2	LVDS_B2+	LVDS	O	LVDS secondary channel differential pair 2 positive signal
		eDP1_LANE2+	eDP	O	Embedded Display Port secondary channel differential lane 2 positive signal
17	1 / 2	LVDS_A3+	LVDS	O	LVDS primary channel differential pair 3 positive signal
		eDP0_LANE3+	eDP	O	Embedded Display Port primary channel differential lane 3 positive signal
18	1 / 2	GND	GND	P	Ground
19	1 / 2	GND	GND	P	Ground
20	1	LCD_D6	TTL	O	LCD Pixel Data bit 6
	2	LVDS_B3-	LVDS	O	LVDS secondary channel differential pair 3 negative signal
		eDP1_LANE3-	eDP	O	Embedded Display Port secondary channel differential lane 3 negative signal
21	1 / 2	LVDS_ACLK-	LVDS	O	LVDS primary channel clock negative signal
		eDP0_AUX-	eDP	O	Embedded Display Port primary differential pair Auxiliary negative signal
22	1	LCD_D7	TTL	O	LCD Pixel Data bit 7
	2	LVDS_B3+	LVDS	O	LVDS secondary channel differential pair 3 positive signal
		eDP1_LANE3+	eDP	O	Embedded Display Port secondary channel differential lane 3 positive signal
23	1 / 2	LVDS_ACLK+	LVDS	O	LVDS primary channel clock positive signal
		eDP0_AUX+	eDP	O	Embedded Display Port primary differential pair Auxiliary positive signal
24	1 / 2	GND	GND	P	Ground
25	1 / 2	GND	GND	P	Ground

Pin #	EDM	Signal	V	I/O	Description
26	1	LCD_D8	TTL	O	LCD Pixel Data bit 8
	2	LVDS_BCLK-	LVDS	O	LVDS secondary channel clock negative signal
		eDP1_AUX-	eDP	O	Embedded Display Port secondary differential pair Auxiliary negative signal
27	1 / 2	LVDS_ABL_CTRL	CMOS 3.3V	O	LVDS primary channel panel backlight control
28	1	LCD_D9	TTL	O	LCD Pixel Data bit 9
	2	LVDS_BCLK+	LVDS	O	LVDS secondary channel clock positive signal
		eDP1_AUX+	eDP	O	Embedded Display Port secondary differential pair Auxiliary positive signal
29	1 / 2	LVDS_AEN	CMOS 3.3V	O	LVDS primary channel panel backlight enable
30	1 / 2	GND	GND	P	Ground
31	1 / 2	LVDS_AVDD_EN	CMOS 3.3V	O	LVDS primary channel panel power enable
32	1	LCD_D10	TTL	O	LCD Pixel Data bit 10
	2	LVDS_BBL_CTRL	CMOS 3.3V	O	LVDS secondary channel panel backlight control
33	1 / 2	eDP0_SELFTEST	CMOS 3.3V	I	Embedded Display Port Detection pin
34	1	LCD_D11	TTL	O	LCD Pixel Data bit 11
	2	LVDS_BEN	CMOS 3.3V	O	LVDS secondary channel panel backlight enable
35	1 / 2	eDP0_HPD	CMOS 3.3V	I	Embedded Display Port Hot Plug Detection pin
36	1	LCD_D12	TTL	O	LCD Pixel Data bit 12
	2	LVDS_BVDD_EN	CMOS 3.3V	O	LVDS secondary channel panel power enable
37	1 / 2	I2C_SDA	CMOS 3.3V	I/O	Display ID DDC data line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I^2C bus data line
38	1	LCD_D13	TTL	O	LCD Pixel Data bit 13
	2	eDP1_SELFTEST	CMOS 3.3V	I	Embedded Display Port Detection pin
39	1 / 2	I2C_SCL	CMOS 3.3V	I/O	Display ID DDC clock line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I^2C bus clock line
40	1	LCD_D14	TTL	O	LCD Pixel Data bit 14
	2	eDP1_HPD	CMOS 3.3V	I	Embedded Display Port Hot Plug Detection pin
41	1 / 2	GND	GND	P	Ground
42	1 / 2	GND	GND	P	Ground
43	1 / 2	HDMI1_CLK+	HDMI	O	HDMI differential pair clock positive signal
		DP1_LANE3+	DP	O	Display Port differential pair lane 3 positive signal

Pin #	EDM	Signal	V	I/O	Description
44	1	LCD_D15	TTL	O	LCD Pixel Data bit 15
	2	HDMI2_CLK+	HDMI	O	HDMI differential pair clock positive signal
		DP2_LANE3+	DP	O	Display Port differential pair lane 3 positive signal
45	1 / 2	HDMI1_CLK-	HDMI	O	HDMI differential pair clock negative signal
		DP1_LANE3-	DP	O	Display Port differential pair lane 3 negative signal
46	1	LCD_D16	TTL	O	LCD Pixel Data bit 16
	2	HDMI2_CLK-	HDMI	O	HDMI differential pair clock negative signal
		DP2_LANE3-	DP	O	Display Port differential pair lane 3 negative signal
47	1 / 2	GND	GND	P	Ground
48	1 / 2	GND	GND	P	Ground
49	1 / 2	HDMI1_D0+	HDMI	O	HDMI differential pair 0 positive signal
		DP1_LANE2+	DP	O	Display Port differential pair lane 2 positive signal
50	1	LCD_D17	TTL	O	LCD Pixel Data bit 17
	2	HDMI2_D0+	HDMI	O	HDMI differential pair 0 positive signal
		DP2_LANE2+	DP	O	Display Port differential pair lane 2 positive signal
51	1 / 2	HDMI1_D0-	HDMI	O	HDMI differential pair 0 negative signal
		DP1_LANE2-	DP	O	Display Port differential pair lane 2 negative signal
52	1	LCD_D18	TTL	O	LCD Pixel Data bit 18
	2	HDMI2_D0-	HDMI	O	HDMI differential pair 0 negative signal
		DP2_LANE2-	DP	O	Display Port differential pair lane 2 negative signal
53	1 / 2	GND	GND	P	Ground
54	1 / 2	GND	GND	P	Ground
55	1 / 2	HDMI1_D1+	HDMI	O	HDMI differential pair 1 positive signal
		DP1_LANE1+	DP	O	Display Port differential pair lane 1 positive signal
56	1	LCD_D19	TTL	O	LCD Pixel Data bit 19
	2	HDMI1_D1+	HDMI	O	HDMI differential pair 1 positive signal
		DP2_LANE1+	DP	O	Display Port differential pair lane 1 positive signal
57	1 / 2	HDMI1_D1-	HDMI	O	HDMI differential pair 1 negative signal
		DP1_LANE1-	DP	O	Display Port differential pair lane 1 negative signal
58	1	LCD_D20	TTL	O	LCD Pixel Data bit 20
	2	HDMI2_D1-	HDMI	O	HDMI differential pair 1 negative signal
		DP2_LANE1-	DP	O	Display Port differential pair lane 1 negative signal
59	1 / 2	GND	GND	P	Ground
60	1 / 2	GND	GND	P	Ground
61	1 / 2	HDMI1_D2+	HDMI	O	HDMI differential pair 2 positive signal
		DP1_LANE0+	DP	O	Display Port differential pair lane 0 positive signal

Pin #	EDM	Signal	V	I/O	Description
62	1	LCD_D21	TTL	O	LCD Pixel Data bit 21
	2	HDMI2_D2+	HDMI	O	HDMI differential pair 2 positive signal
		DP2_LANE0+	DP	O	Display Port differential pair lane 0 positive signal
63	1 / 2	HDMI1_D2-	HDMI	O	HDMI differential pair 2 negative signal
		DP1_LANE0-	DP	O	Display Port differential pair lane 0 negative signal
64	1	LCD_D22	TTL	O	LCD Pixel Data bit 22
	2	HDMI2_D2-	HDMI	O	HDMI differential pair 2 negative signal
		DP2_LANE0-	DP	O	Display Port differential pair lane 0 negative signal
65	1 / 2	GND	GND	P	Ground
66	1 / 2	GND	GND	P	Ground
67	1 / 2	HDMI1_HPD DP1_HPD	CMOS 3.3V	I	HDMI/DP Hot plug detection signal that serves as an interrupt request
68	1	LCD_D23	TTL	O	LCD Pixel Data bit 23
	2	HDMI2_HPD DP2_HPD	CMOS 3.3V	I	HDMI/DP Hot plug detection signal that serves as an interrupt request
69	1 / 2	HDMI1_CAD	HDMI	I / O	Cable Adaptor Detect
		DP1_CONFIG1	DP	I / O	Display Port Config 1 signal
70	1	LCD_CLK	TTL	O	LCD Pixel Clock
	2	HDMI2_CAD	HDMI	I / O	Cable Adaptor Detect
		DP2_CONFIG1	DP	I / O	Display Port Config 1 signal
71	1 / 2	HDMI1_CEC	HDMI	I / O	HDMI Consumer Electronics Control
		DP1_CONFIG2	DP	I / O	Display Port Config 2 signal
72	1	LCD_HSYNC	TTL	O	LCD Horizontal Synchronization
	2	HDMI2_CEC	HDMI	I / O	HDMI Consumer Electronics Control
		DP2_CONFIG2	DP	I / O	Display Port Config 2 signal
73	1 / 2	I2C_SCL	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus clock line
		DP1_AUX+	DP	O	Display Port differential pair Auxiliary positive signal
74	1	LCD_VSYNC	TTL	O	LCD Vertical Synchronization
	2	I2C_SCL	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus clock line
		DP2_AUX+	DP	O	Display Port differential pair Auxiliary positive signal
75	1 / 2	I2C_SDA	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus data line
		DP1_AUX-	DP	O	Display Port differential pair Auxiliary negative signal

Pin #	EDM	Signal	V	I/O	Description
76	1	LCD_CNTRST	TTL	O	LCD backlight control
	2	I2C_SDA	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus data line
		DP2_AUX-	DP	O	Display Port differential pair Auxiliary negative signal
77	1 / 2	GND	GND	P	Ground
78	1	LCD_DRD Y	TTL	O	LCD dot enable pin signal
	2	PCIECLK_OE0	PCIE	O	PCI Express channel 0 hot plug detection signal
79	1 / 2	PCIEB_CLK+	PCIE	O	PCI Express channel B clock differential pair positive signal
80	1	LCD_VDDEN	TTL	O	LCD Voltage On
	2	PCIE0_CLK+	PCIE	O	PCI Express channel 0 clock differential pair positive signal
81	1 / 2	PCIEB_CLK-	PCIE	O	PCI Express channel B clock differential pair negative signal
82	1	LCD_BKLEN	TTL	O	LCD Backlight Control
	2	PCIE0_CLK-	PCIE	O	PCI Express channel 0 clock differential pair negative signal
83	1 / 2	GND	GND	P	Ground
84	1	RSVD			Reserved
	2	PCIE1_CLK+	PCIE	O	PCI Express channel 1 clock differential pair positive signal
85	1 / 2	PCIEA_CLK+	PCIE	O	PCI Express channel A clock differential pair positive signal
86	1	GPMC_nCSA	CMOS 3.3V	O	GPMC Chip Select bit A
	2	PCIE1_CLK-	PCIE	O	PCI Express channel 1 clock differential pair negative signal
87	1 / 2	PCIEA_CLK-	PCIE	O	PCI Express channel A clock differential pair negative signal
88	1 / 2	GND	GND	P	Ground
89	1 / 2	GND	GND	P	Ground
90	1	GPMC_nCSB	CMOS 3.3V	O	GPMC Chip Select bit B
	2	PCIE0_TX+	PCIE	O	PCI Express channel 0 Transmit output differential pair positive signal
91	1 / 2	PCIEA_TX+	PCIE	O	PCI Express channel A Transmit output differential pair positive signal
92	1	GPMC_nCSC	CMOS 3.3V	O	GPMC Chip Select bit C
	2	PCIE0_TX-	PCIE	O	PCI Express channel 0 Transmit output differential pair negative signal
93	1 / 2	PCIEA_TX-	PCIE	O	PCI Express channel A Transmit output differential pair negative signal
94	1 / 2	GND	GND	P	Ground
95	1 / 2	GND	GND	P	Ground

Pin #	EDM	Signal	V	I/O	Description
96	1	GPMC_nCSD	CMOS 3.3V	O	GPMC Chip Select bit D
	2	PCIE0_RX+	PCIE	I	PCI Express channel 0 Receive input differential pair positive signal
97	1 / 2	PCIEA_RX+	PCIE	I	PCI Express channel A Receive input differential pair positive signal
98	1	GPMC_nCSE	CMOS 3.3V	O	GPMC Chip Select bit E
	2	PCIE0_RX-	PCIE	I	PCI Express channel 0 Receive input differential pair negative signal
99	1 / 2	PCIEA_RX-	PCIE	I	PCI Express channel A Receive input differential pair negative signal
100	1 / 2	GND	GND	P	Ground
101	1 / 2	GND	GND	P	Ground
102	1	GPMC_WAIT	CMOS 3.3V	I	External indication of wait
	2	PCIE1_TX+	PCIE	O	PCI Express channel 1 Transmit output differential pair positive signal
103	1 / 2	PCIEB_TX+	PCIE	O	PCI Express channel B Transmit output differential pair positive signal
104	1	GPMC_WP	CMOS 3.3V	O	GPMC Write Protect / Enable
	2	PCIE1_TX-	PCIE	O	PCI Express channel 1 Transmit output differential pair negative signal
105	1 / 2	PCIEB_TX-	PCIE	O	PCI Express channel B Transmit output differential pair negative signal
106	1	GPMC_CLE	CMOS 3.3V	O	GPMC Lower Byte Enable. Also used for Command Latch Enable
	2	PCIECLK_OE1	PCIE	O	PCI Express channel 1 hot plug detection signal
107	1 / 2	PCIE_PRST#	PCIE	I	PCI Express interface presence detection pin
108	1	GPMC_ALE	CMOS 3.3V	O	GPMC Address Valid or Address Latch Enable
	2	PCIE1_RX+	PCIE	I	PCI Express channel 1 Receive input differential pair positive signal
109	1 / 2	PCIEB_RX+	PCIE	I	PCI Express channel B Receive input differential pair positive signal
110	1	GPMC_WE	CMOS 3.3V	I	GPMC Write Enable
	2	PCIE1_RX-	PCIE	I	PCI Express channel 1 Receive input differential pair negative signal
111	1 / 2	PCIEB_RX-	PCIE	I	PCI Express channel B Receive input differential pair negative signal
112	1	GPMC_RE	CMOS 3.3V	O	GPMC Read Enable
	2	PCIE_CPPE#	PCIE	O	PCI Express module detection and power control
113	1 / 2	PCIECLK_OEA	PCIE	O	PCI Express channel A hot plug detection signal
114	1	RSVD			Reserved
	2	PCIE2_TX+	PCIE	O	PCI Express channel 2 Transmit output differential pair positive signal

Pin #	EDM	Signal	V	I/O	Description
115	1 / 2	PCIECLK_OEB	PCIE	O	PCI Express channel B hot plug detection signal
116	1	GPMC_A10	CMOS 3.3V	O	GPMC output address bit 10
	2	PCIE2_TX-	PCIE	O	PCI Express channel 2 Transmit output differential pair negative signal
117	1 / 2	PCIE_WAKE#	CMOS 3.3V	I	PCI Express Wake Event: Sideband wake signal asserted by components requesting wake up
118	1	GPMC_A9	CMOS 3.3V	O	GPMC output address bit 9
	2	PCIECLK_OE2	PCIE	O	PCI Express channel 2 hot plug detection signal
119	1 / 2	PCIE_RST#	CMOS 3.3V	O	PCI Express Reset signal for external devices
120	1	GPMC_A8	CMOS 3.3V	O	GPMC output address bit 8
	2	PCIE2_RX+	PCIE	I	PCI Express channel 2 Receive input differential pair positive signal
121	1 / 2	GND	GND	P	Ground
122	1	GPMC_A7	CMOS 3.3V	O	GPMC output address bit 7
	2	PCIE2_RX-	PCIE	I	PCI Express channel 2 Receive input differential pair negative signal
123	1 / 2	SATA1_RXP	SATA	I	Serial ATA channel 1 Receive differential pair positive signal
124	1 / 2	GND	GND	P	Ground
125	1 / 2	SATA1_RXN	SATA	I	Serial ATA channel 1 Receive differential pair negative signal
126		KEY			
127		KEY			
128		KEY			
129		KEY			
130		KEY			
131		KEY			
132		KEY			
133	1 / 2	SATA1_nACT	SATA	I/O	Serial ATA LED. Open collector output pin driven during SATA command activity
134	1	GPMC_A6	CMOS 3.3V	O	GPMC output address bit 6
	2	PCIE2_CLK+	PCIE	O	PCI Express channel 2 clock differential pair positive signal
135	1 / 2	SATA1_TXP	SATA	O	Serial ATA channel 1 Transmit differential pair positive signal
136	1	GPMC_A5	CMOS 3.3V	O	GPMC output address bit 5
	2	PCIE2_CLK-	PCIE	O	PCI Express channel 2 clock differential pair negative signal
137	1 / 2	SATA1_TXN	SATA	O	Serial ATA channel 1 Transmit differential pair negative signal

Pin #	EDM	Signal	V	I/O	Description
138	1	GPMC_A4	CMOS 3.3V	O	GPMC output address bit 4
	2	PCIE3_TX+	PCIE	O	PCI Express channel 3 Transmit output differential pair positive signal
139	1 / 2	USB1_HUB_RST	USB	O	Universal Serial Bus carrier board hub reset pin
140	1	GPMC_A3	CMOS 3.3V	O	GPMC output address bit 3
	2	PCIE3_TX-	PCIE	O	PCI Express channel 3 Transmit output differential pair negative signal
141	1 / 2	USB2_OC	CMOS 3.3V	I	Over current detect input pin to monitor USB power over current
142	1	GPMC_A2	CMOS 3.3V	O	GPMC output address bit 2
	2	PCIECLK_OE3	PCIE	O	PCI Express channel 3 hot plug detection signal
143	1 / 2	StdB2_SSRX+	USB	I	Universal Serial Bus Superspeed receiver differential pair positive signal
144	1	GPMC_A1	CMOS 3.3V	O	GPMC output address bit 1
	2	PCIE3_RX+	PCIE	I	PCI Express channel 3 Receive input differential pair positive signal
145	1 / 2	StdB2_SSRX-	USB	I	Universal Serial Bus Superspeed receiver differential pair negative signal
146	1	GPMC_D15	CMOS 3.3V	I/O	GPMC data bit 15
	2	PCIE3_RX-	PCIE	I	PCI Express channel 3 Receive input differential pair negative signal
147	1 / 2	GND2_DRAIN	USB	P	Universal Serial Bus ground for signal return
148	1 / 2	GND	GND	P	Ground
149	1 / 2	StdB2_SSTX+	USB	O	Universal Serial Bus Superspeed transmitter differential pair positive signal
150	1	GPMC_D14	CMOS 3.3V	I/O	GPMC data bit 14
	2	PCIE3_CLK+	PCIE	O	PCI Express channel 3 clock differential pair positive signal
151	1 / 2	StdB2_SSTX-	USB	O	Universal Serial Bus Superspeed transmitter differential pair negative signal
152	1	GPMC_D13	CMOS 3.3V	I/O	GPMC data bit 13
	2	PCIE3_CLK-	PCIE	O	PCI Express channel 3 clock differential pair negative signal
153	1 / 2	GND	GND	P	Ground
154	1 / 2	GND	GND	P	Ground
155	1 / 2	USB2_OTG_ID	USB	I	Universal Serial Bus On-The-Go detection signal

Pin #	EDM	Signal	V	I/O	Description
156	1	GPMC_D12	CMOS 3.3V	I/O	GPMC data bit 12
	2	SATA2_RXP	SATA	I	Serial ATA channel 2 Receive differential pair positive signal
157	1 / 2	USB2_D+	USB	I/O	Universal Serial Bus port 2 differential pair positive signal
158	1	GPMC_D11	CMOS 3.3V	I/O	GPMC data bit 11
	2	SATA2_RXN	SATA	I	Serial ATA channel 2 Receive differential pair negative signal
159	1 / 2	USB2_D-	USB	I/O	Universal Serial Bus port 2 differential pair negative signal
160	1	GPMC_D10	CMOS 3.3V	I/O	GPMC data bit 10
	2	SATA2_ODD	SATA	I/O	Serial ATA channel 2 ODD signal
161	1 / 2	USB2_VBUS	5V	I/O	Universal Serial Bus port 2 power
162	1	GPMC_D9	CMOS 3.3V	I/O	GPMC data bit 9
	2	SATA2_TXN	SATA	O	Serial ATA channel 2 Transmit differential pair negative signal
163	1 / 2	USB2_PWR_EN	USB	O	Universal Serial Bus power enable
164	1	GPMC_D8	CMOS 3.3V	I/O	GPMC data bit 8
	2	SATA2_TXP	SATA	O	Serial ATA channel 2 Transmit differential pair positive signal
165	1 / 2	USB1_OC	CMOS 3.3V	I	Over current detect input pin to monitor USB power over current
166	1 / 2	GND	GND	P	Ground
167	1 / 2	StdB1_SSRX+	USB	I	Universal Serial Bus Superspeed receiver differential pair positive signal
168	1	GPMC_D7	CMOS 3.3V	I/O	GPMC data bit 7
	2	LPC_AD0	CMOS 3.3V	I/O	Low Pin Count Interface multiplex Address and Data line 0
169	1 / 2	StdB1_SSRX-	USB	I	Universal Serial Bus Superspeed receiver differential pair negative signal
170	1	GPMC_D6	CMOS 3.3V	I/O	GPMC data bit 6
	2	LPC_AD1	CMOS 3.3V	I/O	Low Pin Count Interface multiplex Address and Data line 1
171	1 / 2	GND1_DRAIN	USB	P	Universal Serial Bus ground for signal return
172	1	GPMC_D5	CMOS 3.3V	I/O	GPMC data bit 5
	2	LPC_AD2	CMOS 3.3V	I/O	Low Pin Count Interface multiplex Address and Data line 2
173	1 / 2	StdB1_SSTX+	USB	O	Universal Serial Bus Superspeed transmitter differential pair positive signal
174	1	GPMC_D4	CMOS 3.3V	I/O	GPMC data bit 4
	2	LPC_AD3	CMOS 3.3V	I/O	Low Pin Count Interface multiplex Address and Data line 3

Pin #	EDM	Signal	V	I/O	Description
175	1 / 2	StdB1_SSTX-	USB	O	Universal Serial Bus Superspeed transmitter differential pair negative signal
176	1	GPMC_D3	CMOS 3.3V	I/O	GPMC data bit 3
	2	LPC_CLK	CMOS 3.3V	O	Low Pin Count Interface clock
177	1 / 2	GND	GND	P	Ground
178	1	GPMC_D2	CMOS 3.3V	I/O	GPMC data bit 2
	2	LPC_nFRAME	CMOS 3.3V	O	Low Pin Count Interface frame
179	1 / 2	USB1_D-	USB	I/O	Universal Serial Bus port 1 differential pair negative signal
180	1	GPMC_D1	CMOS 3.3V	I/O	GPMC data bit 1
	2	LPC_nLDDRQ	CMOS 3.3V	I	Low Pin Count Interface DMA request
181	1 / 2	USB1_D+	USB	I/O	Universal Serial Bus port 1 differential pair positive signal
182	1	GPMC_D0	CMOS 3.3V	I/O	GPMC data bit 0
	2	LPC_nSERIRQ	CMOS 3.3V	I/O	Low Pin Count Interface serialized interrupt
183	1 / 2	USB1_VBUS	5V	I/O	Universal Serial Bus port 1 power
184	1 / 2	GND	GND	P	Ground
185	1 / 2	GND	GND	P	Ground
186	1	I2S2_RXD	CMOS 3.3V	I	Secondary Integrated Interchip Sound (I^2S) channel receive data line
	2	HDA_SYNC	CMOS 3.3V	O	HD Audio/AC'97 Serial Bus Synchronization
187	1 / 2	I2S1_RXD	CMOS 3.3V	I	Primary Integrated Interchip Sound (I^2S) channel receive data line
188	1	I2S2_TXFS	CMOS 3.3V	O	Secondary Integrated Interchip Sound (I^2S) channel frame synchronization signal
	2	HDA_BITCLK	CMOS 3.3V	O	HD Audio/AC'97 24Mhz Serial bit Clock from Codec
189	1 / 2	I2S1_TXFS	CMOS 3.3V	O	Primary Integrated Interchip Sound (I^2S) channel frame synchronization signal
190	1	I2S2_TXD	CMOS 3.3V	O	Secondary Integrated Interchip Sound (I^2S) channel transmit data line
	2	HDA_nRST	CMOS 3.3V	O	HD Audio/AC'97 Codec reset
191	1 / 2	I2S1_TXD	CMOS 3.3V	O	Primary Integrated Interchip Sound (I^2S) channel transmit data line
192	1	I2S2_TXC	CMOS 3.3V	O	Secondary Integrated Interchip Sound (I^2S) channel word clock signal
	2	HDA_SDI	CMOS 3.3V	I	HD Audio/AC'97 Serial Data Input from Codec
193	1 / 2	I2S1_TXC	CMOS 3.3V	O	Primary Integrated Interchip Sound (I^2S) channel word clock signal

Pin #	EDM	Signal	V	I/O	Description
194	1	I2S2_CLK	CMOS 3.3V	O	Secondary Integrated Interchip Sound (I^2S) channel master clock signal
	2	HDA_SDO	CMOS 3.3V	O	HD Audio/AC'97 Serial Data Output to Codec
195	1 / 2	I2S1_CLK	CMOS 3.3V	O	Primary Integrated Interchip Sound (I^2S) channel master clock signal
196	1 / 2	SPDIF_OUT	SPDIF	O	Sony / Philips Digital Interconnect Format Audio output
197	1 / 2	CAN2+	CAN	I/O	Secondary CAN (controller Area Network) differential pair positive signal
198	1 / 2	GND	GND	P	Ground
199	1 / 2	CAN2-	CAN	I/O	Secondary CAN (controller Area Network) differential pair negative signal
200	1 / 2	CAN1+	CAN	I/O	Primary CAN (controller Area Network) differential pair positive signal
201	1 / 2	GND	GND	P	Ground
202	1 / 2	CAN1-	CAN	I/O	Primary CAN (controller Area Network) differential pair negative signal
203	1 / 2	SDIO_CD	CMOS 3.3V	I/O	MMC/SDIO Card Detect
204	1 / 2	GND	GND	P	Ground
205	1 / 2	SDIO_CMD	CMOS 3.3V	I/O	MMC/SDIO Command
206	1 / 2	SDIO_CLK	CMOS 3.3V	O	MMC/SDIO Clock
207	1 / 2	SDIO_WP	CMOS 3.3V	I/O	MMC/SDIO Write Protect
208	1 / 2	SDIO_LED	CMOS 3.3V	O	MMC/SDIO LED
209	1 / 2	SDIO_DAT1	CMOS 3.3V	I/O	MMC/SDIO Data bit 1
210	1 / 2	SDIO_PWR	CMOS 3.3V	O	MMC/SDIO Power Enable
211	1 / 2	SDIO_DAT3	CMOS 3.3V	I/O	MMC/SDIO Data bit 3
212	1 / 2	SDIO_DAT0	CMOS 3.3V	I/O	MMC/SDIO Data bit 0
213	1 / 2	SDIO_DAT5	CMOS 3.3V	I/O	MMC/SDIO Data bit 5
214	1 / 2	SDIO_DAT2	CMOS 3.3V	I/O	MMC/SDIO Data bit 2
215	1 / 2	SDIO_DAT7	CMOS 3.3V	I/O	MMC/SDIO Data bit 7
216	1 / 2	SDIO_DAT4	CMOS 3.3V	I/O	MMC/SDIO Data bit 4
217	1 / 2	GND	GND	P	Ground
218	1 / 2	SDIO_DAT6	CMOS 3.3V	I/O	MMC/SDIO Data bit 6
219	1 / 2	SPI2_MOSI	CMOS 3.3V	O	Serial Peripheral Interface primary channel master output slave input signal
220	1 / 2	GND	GND	P	Ground

Pin #	EDM	Signal	V	I/O	Description
221	1 / 2	SPI2_MISO	CMOS 3.3V	I	Serial Peripheral Interface primary channel master input slave output signal
222	1 / 2	SPI1_MOSI	CMOS 3.3V	O	Serial Peripheral Interface secondary channel master output slave input signal
223	1 / 2	SPI2_CLK	CMOS 3.3V	O	Serial Peripheral Interface primary channel clock signal
224	1 / 2	SPI1_MISO	CMOS 3.3V	I	Serial Peripheral Interface secondary channel master input slave output signal
225	1 / 2	SPI2_CS0	CMOS 3.3V	O	Serial Peripheral Interface primary channel Chip Select 0 signal
226	1 / 2	SPI1_CLK	CMOS 3.3V	O	Serial Peripheral Interface secondary channel clock signal
227	1 / 2	SPI2_CS1	CMOS 3.3V	O	Serial Peripheral Interface primary channel Chip Select 1 signal. Do not use if only 1 SPI device is used
228	1 / 2	SPI1_CS0	CMOS 3.3V	O	Serial Peripheral Interface secondary channel Chip Select 0 signal
229	1 / 2	GND	GND	P	Ground
230	1 / 2	SPI1_CS1	CMOS 3.3V	O	Serial Peripheral Interface secondary channel Chip Select 1 signal. Do not use if only 1 SPI device is used
231	1 / 2	I2C2_SCL	CMOS 3.3V	I/O	I^2C bus clock line
232	1 / 2	GND	GND	P	Ground
233	1 / 2	I2C2_SDA	CMOS 3.3V	I/O	I^2C bus data line
234	1 / 2	UART2_CTS	UART	O	Universal Asynchronous Receive Transmit secondary channel clear to send signal
235	1 / 2	I2C3_SCL	CMOS 3.3V	I/O	I^2C bus clock line
236	1 / 2	UART2_TXD	UART	O	Universal Asynchronous Receive Transmit secondary channel transmit data signal
237	1 / 2	I2C3_SDA	CMOS 3.3V	I/O	I^2C bus data line
238	1 / 2	UART2_RXD	UART	I	Universal Asynchronous Receive Transmit secondary channel receive data signal
239	1 / 2	GND	GND	P	Ground
240	1 / 2	UART2_RTS	UART	O	Universal Asynchronous Receive Transmit secondary channel request to send signal
241	1 / 2	UART1_CTS	UART	O	Universal Asynchronous Receive Transmit secondary channel clear to send signal
242	1 / 2	UART2_DCD	UART	I	Universal Asynchronous Receive Transmit secondary channel carrier detect signal

Pin #	EDM	Signal	V	I/O	Description
243	1 / 2	UART1_TXD	UART	O	Universal Asynchronous Receive Transmit secondary channel transmit data signal
244	1 / 2	UART2_DSR	UART	I	Universal Asynchronous Receive Transmit secondary channel data set ready signal
245	1 / 2	UART1_RXD	UART	I	Universal Asynchronous Receive Transmit secondary channel receive data signal
246	1 / 2	UART2_DTR	UART	O	Universal Asynchronous Receive Transmit secondary channel data terminal ready signal
247	1 / 2	UART1_RTS	UART	O	Universal Asynchronous Receive Transmit secondary channel request to send signal
248	1 / 2	UART2_RI	UART	I	Universal Asynchronous Receive Transmit secondary channel ring indication signal
249	1 / 2	GND	GND	P	Ground
250	1 / 2	GND	GND	P	Ground
251	1 / 2	S3	CMOS 3.3V	O	S3 signal shuts off power to all runtime system components that are not maintained during S3 state (suspend to RAM)
252	1 / 2	ON/OFF	CMOS 3.3V	I	Power ON button input signal
253	1 / 2	S5	CMOS 3.3V	O	S5 signal shuts off power to the system. Restart is only possible with power button or by a system wake up event
254	1 / 2	RESET	CMOS 3.3V	I	Reset button input signal
255	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
256	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
257	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
258	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
259	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
260	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
261	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
262	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
263	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
264	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
265	1 / 2	GND	GND	P	Ground
266	1 / 2	GND	GND	P	Ground

Pin #	EDM	Signal	V	I/O	Description
267	1 / 2	RSVD			Reserved
268	1 / 2	RSVD			Reserved
269	1 / 2	RSVD			Reserved
270	1 / 2	RSVD			Reserved
271	1 / 2	RSVD			Reserved
272	1 / 2	RSVD			Reserved
273	1 / 2	RSVD			Reserved
274	1 / 2	RSVD			Reserved
275	1 / 2	RSVD			Reserved
276	1 / 2	RSVD			Reserved
277	1 / 2	RSVD			Reserved
278	1 / 2	RSVD			Reserved
279	1 / 2	Watchdog	CMOS 3.3V	O	Watchdog event indication signal
280	1 / 2	RSVD			Reserved
281	1 / 2	VCC_RTC	3.3V	I	Input power for RTC clock

3. Signal Descriptions

3.1. LVDS Interface

EDM type 1 module provide up to single-channel LVDS which is defined as LVDS_A and EDM type 2 module provide up to two single-channel LVDS or one dual-channel LVDS which are defined as LVDS_A and LVDS_B.

Systems normally use a single-channel LVDS for most displays. Dual LVDS channels are used for very high-bandwidth displays. Single-channel LVDS means that one complete RGB pixel is transmitted per display input clock (also known as the shift clock. Dual-channel LVDS means that two complete RGB pixels are transmitted per display input clock. The two pixels are adjacent along a display line.

A module that supports dual-channel LVDS does not automatically support two separate LVDS displays. This is EDM module dependent and should be checked in the EDM module vendors' documentation.

Each EDM LVDS channel consists of four differential data pairs and a differential clock pair for a total of five differential pairs per channel. Certain EDM module processors or chipsets may not use all pairs. For example, with 18-bit TFT displays, only three of the four data pairs on the LVDS_A channel are used, along with the LVDS_A clock. The LVDS_B lines are not used. The manner in which RGB data is packed onto the LVDS pairs (including packing order and color depth) is not specified by the EDM specification. This may be module-dependent and please check your EDM module vendors' documentation.

There are five single-ended signals included to support the LVDS interface: two lines are used for an I^2C interface that may be used to support EDID or other panel information and identification schemes. Additionally, there are an LVDS power enable (LVDS_xVDD_EN) and backlight control and enable lines (LVDS_xBL_CTRL and LVDS_xEN).

3.1.1. LVDS Signal Description

Table 3 - LVDS_A Signal Description

Pin #	EDM	Signal	V	I/O	Description
E3_9	1 / 2	LVDS_A0-	LVDS	O	LVDS primary channel differential pair 0 signal
E3_10	1 / 2	LVDS_A0+	LVDS	O	
3	1 / 2	LVDS_A1-	LVDS	O	LVDS primary channel differential pair 1 signal
5	1 / 2	LVDS_A1+	LVDS	O	
9	1 / 2	LVDS_A2-	LVDS	O	LVDS primary channel differential pair 2 signal
11	1 / 2	LVDS_A2+	LVDS	O	
15	1 / 2	LVDS_A3-	LVDS	O	LVDS primary channel differential pair 3 signal
17	1 / 2	LVDS_A3+	LVDS	O	
21	1 / 2	LVDS_ACLK-	LVDS	O	LVDS primary channel clock signal
23	1 / 2	LVDS_ACLK+	LVDS	O	
27	1 / 2	LVDS_ABL_CTRL	CMOS 3.3V	O	LVDS primary channel panel backlight control
29	1 / 2	LVDS_AEN	CMOS 3.3V	O	LVDS primary channel panel backlight enable
31	1 / 2	LVDS_AVDD_EN	CMOS 3.3V	O	LVDS primary channel panel power enable
37	1 / 2	I2C_SDA	CMOS 3.3V	I/O	Display ID DDC data line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I^2C bus data line
39	1 / 2	I2C_SCL	CMOS 3.3V	I/O	Display ID DDC clock line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I^2C bus clock line

Note : Signals with gray background are shared with the embedded Display Port signals.

Table 4 - LVDS_B Signal Description

Pin #	EDM	Signal	V	I/O	Description
2	2	LVDS_B0-	LVDS	O	LVDS secondary channel differential pair 0 signal
4	2	LVDS_B0+	LVDS	O	
8	2	LVDS_B1-	LVDS	O	LVDS secondary channel differential pair 1 signal
10	2	LVDS_B1+	LVDS	O	
14	2	LVDS_B2-	LVDS	O	LVDS secondary channel differential pair 2 signal
16	2	LVDS_B2+	LVDS	O	
20	2	LVDS_B3-	LVDS	O	LVDS secondary channel differential pair 3 signal
22	2	LVDS_B3+	LVDS	O	
26	2	LVDS_BCLK-	LVDS	O	LVDS secondary channel clock signal
28	2	LVDS_BCLK+	LVDS	O	
32	2	LVDS_BBL_CTRL	CMOS 3.3V	O	LVDS secondary channel panel backlight control
34	2	LVDS_BEN	CMOS 3.3V	O	LVDS secondary channel panel backlight enable
36	2	LVDS_BVDD_EN	CMOS 3.3V	O	LVDS secondary channel panel power enable

Note : Signals with gray background are shared with the embedded Display Port signals.

3.1.2. LVDS Connector and Cabling

When implementing LVDS signal pairs on a single-ended carrier board connector, the signals of a pair should be arranged so that the positive and negative signals are side by side. The trace lengths of the LVDS signal pairs between the EDM module and the connector on the carrier board should be as close as possible. Additionally, one or more ground traces/pins must be placed between the LVDS pairs.

Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode noise, which is rejected by the receiver.

Twisted pair cables provide a low-cost solution with good balance and flexibility. They are capable of medium to long runs depending upon the application skew budget. A variety of shielding options are available.

Ribbon cables are a cost effective and easy solution. Even though they are not well suited for high-speed differential signaling they do work fine for very short runs. Most cables will work effectively for cable distances of <0.5m.

The cables and connectors that are to be utilized should have a differential impedance of 100Ω ±15%. They should not introduce major impedance discontinuities that cause signal reflections.

For more information about this subject, refer to the 'LVDS Owners Manual Section 6' available from National Semiconductor (http://www.national.com).

One suggested LVDS connector to be used on the carrier board is a Hirose DF13-40DP-1.25V. Matching LVDS cables should use a Hirose DF13-40SA-1.25C matching connector or equivalent.

Figure 16 - LVDS Connector

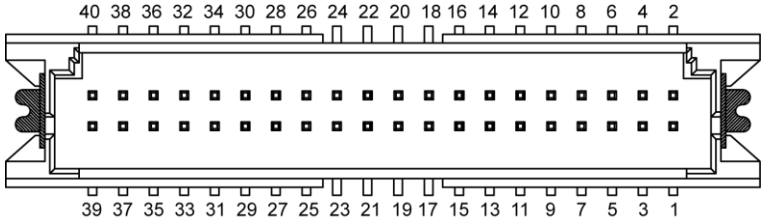


Table 5 - LVDS Connector Suggested Pin-out

Pin #	Signal	Description	Pin #	Signal	Description
1	12V	12V power to data driver circuit	2	5V	5V power to data driver circuit
3	12V		4	5V	
5	LCD_ENB	LCD on/off @ 5V	6	PWM_5V	Backlight PWM @ 5V
7	LCD_ENBK	LCD on/off @ 3.3V	8	PWM_3.3V	Backlight PWM @ 3.3V
9	GND	Ground	10	GND	Ground
11	SEL68	LVDS 18/24 bit selection pin	12	3.3V	3.3V power to data driver circuit
13	LVDS_D0-	LVDS primary channel differential pair 0 signal	14	3.3V	
15	LVDS_D0+		16	LVDS REV	LVDS Reverse Scan signal
17	GND	Ground	18	LVDS R/L	Horizontal Reverse Scan Control
19	LVDS_D1-	LVDS primary channel differential pair 1 signal	20	LVDS U/D	Vertical Reverse Scan Control
21	LVDS_D1+		22	SCL	Display ID DDC clock line used for LVDS flat panel detection
23	GND	Ground	24	SDA	Display ID DDC data line used for LVDS flat panel detection.
25	LVDS_D2-	LVDS primary channel differential pair 2 signal	26	LED enable	Backlight on/off
27	LVDS_D2+		28	LED+	Backlight LED signals (5V)
29	GND	Ground	30	LED+	
31	LVDS_CLK-	LVDS primary channel differential pair clock signal	32	LED+	
33	LVDS_CLK+		34	LVDS enable	LCD signal (driver IC) on/off
35	GND	Ground	36	LED-	Ground return signals for LED backlight signals
37	LVDS_D3-	LVDS primary channel differential pair 3 signal	38	LED-	
39	LVDS_D3+		40	LED-	

3.1.3. Display Timing Configuration

The graphic controller needs to be configured to match the timing parameters of the attached flat panel display. To properly configure the controller, there needs to be some method to determine the display parameters. Different module vendors provide differing ways to access display timing parameters. Some vendors store the data in non-volatile memory with the BIOS setup screen as the method for entering the data, other vendors might use a module or carrier based EEPROM. Some vendors might hard code the information into the BIOS or bootloader, and other vendors might support panel located timing via I^2C. Regardless of the method used to store the panel timing parameters, the video BIOS or bootloader will need to have the ability to access and decode the parameters. Given the number of variables it is recommended that carrier board designers contact their EDM module vendor to determine the recommend method to store and retrieve the display timing parameters.

The Video Electronics Standards Association (VESA) released DisplayID, a second generation display identification standard that replaces EDID and other proprietary methods for storing flat panel timing data. DisplayID defines a data structure which contains information such as display model, identification information, colorimetry, feature support, and supported timings and formats. The DisplayID data allows the video controller to be configured for optimal support for the attached display without user intervention. The basic data structure is a variable length block up to 256 bytes with additional 256 byte extensions as required. The DisplayID data is typically stored in a serial EPROM connected to the LVDS_I2C bus. The EPROM can reside on the display or Carrier. DisplayID is not backwards compatible with EDID. Contact VESA (www.vesa.org) for more information.

3.1.4. Backlight Dimming Control

Backlight inverters are either voltage, PWM or resistor controlled. The EDM specification provides two methods for controlling the brightness. One method is to use the backlight control and enable signals from the module. LVDS_xBL_EN and LVDS_xBL_CTRL. LVDS_xBL_CTRL is a Pulse Width Modulated (PWM) output that can be connected to display inverters that accept a PWM input.

The second method it to use the LVDS I^2C bus to control an I2C DAC. The output of the DAC can be used to support voltage controlled inverters. The DAC can be used driving the backlight voltage control input pin of the inverter or LED backlight (LVDS_xBL_CTRL).

3.1.5. Color Mapping and Terms

FPD-Link and Open LDI Color Mapping

An LVDS stream consists of frames that pack seven data bits per LVDS frame. Details can be found in "Table 6 - LVDS Display Terms and Definitions" below. The LVDS clock is one seventh of the source-data clock. The order in which panel data bits are packed into the LVDS stream is referred to as the LVDS color-mapping. There are two LVDS color-mappings in common use: FPD-Link and Open LDI. Open LDI is the newer standard.

The FPD-Link and Open LDI standards are the same for panels with color depths of 18 bits (6 Red, 6 Green, 6 Blue) or less. The 18 bits of color data and 3 bits of control data, or 21 bits total, are packed into 3 LVDS data streams. The LVDS clock is carried on a separate channel for a total of 4 LVDS pairs – 3 data pairs and a clock pair.

For 24-bit color depths, a 4th LVDS data pair is required (for a total of 5 LVDS pairs – 4 data and 1 clock). FPD-Link and Open LDI differ in this case. FPD-Link keeps the least significant color bits on the original 3 LVDS data pairs and adds the most significant color bits (the dominant or "most important" bits) to the 4th channel. Six bits are added: 2 Red, 2 Green, and 2 Blue (the seventh available bit slot in the 4th LVDS stream is not used).

A 24-bit, Open LDI implementation shifts the color bits on the original 3 LVDS data pairs up by two, such that the most significant color bits for both 18- and 24-bit panels occupy the same LVDS slots. For example, the most significant Red color bit is R5 for 18-bit panels and R7 for 24- bit panels. The 18-bit R5 and the 24-bit R7 occupy the same LVDS bit slot in Open LDI. The 4th LVDS data stream in Open LDI carries the least significant bits of a 24-bit panel – R0, R1, G0, G1, B0, and B1.

The advantage of Open LDI is that it provides an easier upgrade and downgrade path than FPD- Link does. An 18-bit panel can be used with an Open LDI 24-bit data stream by simply connecting the 1st three LVDS data pairs to the panel, and leaving the 4th LVDS data pair unused. This does not work with FPD-Link because the mapping for the 24-bit case is not compatible with the 18-bit case – the most significant data bits are on the 4th LVDS data stream.

If you design LVDS deserializers, work around the module color-mapping by picking off the deserializer outputs in the order needed. If you use a flat panel with an integrated LVDS receiver, it is important that the displays color-mapping matches the module's color-mapping.

Table 6 - LVDS Display Terms and Definitions

Term	Definition
Color-Mapping	Color-mapping refers to the order in which display color bits and control bits are placed into the serial LVDS stream. Each LVDS data frame can accept seven bits. The way in which the bits are serialized into the stream is arbitrary, as long as they are de-serialized in a corresponding way. Two main color-mapping schemes are FPD-Link and Open LDI. They are the same for 18-bit panels but differ for 24-bit panels.
DE	Display Enable – a control signal that asserts during an active display line.
Dual Channel	In a dual-channel bit stream, two complete RGB pixels are transmitted with each shift clock. The shift clock is one half the pixel frequency in this case. Dual channel LVDS streams are either 8 differential pairs (6 data pairs, 2 clock pairs, for dual 18 bit streams) or 10 differential pairs (8 data pairs, 2 clock pairs, for dual 24-bit streams).
Even Pixel	A pixel from an even column number, counting from 1. For example, on an 800x600 display, the even pixels along a row are in columns 2,4 … 800. The odd pixels are in columns 1,3,5 … 799.
FPD-Link	Flat Panel Display Link – an LVDS color-mapping scheme popularized by National Semiconductor. FPD Link color-mapping is the same as open LDI color-mapping for 18-bit displays but is different for 24-bit displays. FPD color-mapping puts the most significant bits of a 24-bit display onto the 4th LVDS channel.
HSYNC	Horizontal Sync – a control signal that occurs once per horizontal display line.
LCLK	LVDS clock – the low voltage differential clock that accompanies the serialized LVDS data stream. For a single-channel LVDS stream, the LVDS clock is 1/7th the pixel clock, which means there is one LVDS clock period for every 7 pixel clock periods. For a dual-channel LVDS data stream, the LVDS clock is 1/14th the pixel clock, which means there is one LVDS clock period for every 14-pixel clock periods.
Odd Pixel	A pixel from an odd column number, counting from 1. For example, on an 800x600 display, the odd pixels along a row are in columns 1,3,5, … 799. The even pixels are in columns 2,4 …800.
Open LDI	Open LVDS Display Interface – a formalization by National Semiconductor of de facto LVDS standards. Open LDI color-mapping is the same as FPD-Link color-mapping for 18-bit displays, but is different for 24-bit displays. Open LDI color-mapping puts the least significant bits of a 24-bit display onto the 4th LVDS channel. Doing so means that an 18-bit display can operate on a 24-bit Open LDI link by using the first 3 LVDS data channels.
PCLK	Pixel clock – the clock associated with a single display pixel. For example, on a 640x480 display, there are 640 pixel clocks during the active display line period (and additional pixel clocks during the blanking periods). For a single-channel TFT display, the pixel clock is the same as the shift clock. For a dual-channel TFT display, the pixel clock is twice the frequency of the shift clock.
SCLK	Shift clock – the clock that shifts either a single pixel or a group of pixels into the display, depending on the display type. For a single-channel TFT display, the shift clock is the same as the pixel clock. For a dual-channel TFT display, the shift clock period is twice the pixel clock. For some display types, such as passive STN displays, the shift clock may be four- or eight-pixel clocks.
Single Channel	In a single-channel bit stream, a single RGB pixel is transmitted with each shift clock. The shift clock and the pixel clock are the same in this case. Single-channel LVDS streams are either 4 differential pairs (3 data pairs, 1 clock pair, for a single 18 bit stream) or 5 differential pairs (4 data pairs, 1 clock pair, for a single 24-bit stream).
Transmit Bit Order	The order, in time, in which bits are placed into the seven bit slots per LVDS frame. Bit 1 is earlier in time than bit 2, etc.
Unbalanced	Unbalanced means that the LVDS serializing hardware does not insert or manipulate bits to achieve a DC balance – i.e. an equal number of 0 and 1 bits, when averaged over multiple frames.
VSYNC	Vertical Sync – a control signal that occurs once per display frame.
Xmit Bit Order	See Transmit Bit Order.

3.1.6. Notes on Industry Terms

Some terms in this document that describe LVDS displays may vary from other documents (such as display data sheets from vendors, IC data sheets for graphics controllers and LVDS transmitters and receivers, the Open LDI specification, and EDM module documentation).

Examples of terms that may vary include:

For dual-channel displays, terms are needed to describe the adjacent pixels.
Various documents will reference for the same pair of pixels:
Odd and Even pixels (column count starts at 1)
Even and Odd pixels (column count starts at 0)
R10 and R20 for adjacent least significant Red bits
R00 and R10 for adjacent least significant Red bits

Terms used to describe the clocks vary:

The Open LDI specification uses the term “pixel clock” differently from most other documents. In the Open LDI specification, the “pixel clock” period is seven pixel periods long. Most other documents refer to this concept as the “LVDS clock.”

Transmit Bit Order

In this document, the seven bits in an LVDS frame are numbered 1 – 7, with Bit 1 being placed into the stream before Bit 2.

Display terms used in this document are defined in “Table 6 - LVDS Display Terms and Definitions" above.

3.1.7. LVDS Display Color Mapping Tables

LVDS display color-mappings for single- and dual-channel displays are shown in “Table 7 - LVDS Display: Single Channel, Unbalanced Color-Mapping” and “Table 8 - LVDS Display: Dual Channel, Unbalanced Color-Mapping” below.

For single-channel displays, EDM module LVDS_B pairs are not used and may be left open. For single-channel, 18-bit displays, the LVDS_A3± channel is not used and may be left open.

For 18-bit, single-channel and 36-bit, dual-channel displays, the FPD-Link and Open LDI color-mappings are the same. For 24-bit, single-channel and 48-bit, dual-channel displays, mappings differ and care must be taken that the Module and display LVDS color-mappings agree.

Table 7 - LVDS Display: Single Channel, Unbalanced Color-Mapping

	Xmit Bit Order	LVDS Clock	Open LDI 18 bit Single Channel	Open LDI 24 bit Single Channel	FPD Link 18 bit Single Channel	FPD Link 24 bit Single Channel
LVDS_A0±	1	1	G0	G2	G0	G0
	2	1	R5	R7	R5	R5
	3	0	R4	R6	R4	R4
	4	0	R3	R5	R3	R3
	5	0	R2	R4	R2	R2
	6	1	R1	R3	R1	R1
	7	1	R0	R2	R0	R0
LVDS_A1±	1	1	B1	B3	B1	B1
	2	1	B0	B2	B0	B0
	3	0	G5	G7	G5	G5
	4	0	G4	G6	G4	G4
	5	0	G3	G5	G3	G3
	6	1	G2	G4	G2	G2
	7	1	G1	G3	G1	G1
LVDS_A2±	1	1	DE	DE	DE	DE
	2	1	VSYNC	VSYNC	VSYNC	VSYNC
	3	0	HSYNC	HSYNC	HSYNC	HSYNC
	4	0	B5	B7	B5	B5
	5	0	B4	B6	B4	B4
	6	1	B3	B5	B3	B3
	7	1	B2	B4	B2	B2
LVDS_A3±	1	1				
	2	1		B1		B7
	3	0		B0		B6
	4	0		G1		G7
	5	0		G0		G6
	6	1		R1		R7
	7	1		R0		R6
LVDS_ACLK±			LCLK=PCLK /7 SCLK=PCLK	LCLK=PCLK /7 SCLK=PCLK	LCLK=PCLK /7 SCLK=PCLK	LCLK=PCLK /7 SCLK=PCLK

Table 8 - LVDS Display: Dual Channel, Unbalanced Color-Mapping

	Xmit Bit Order	LVDS Clock	Open LDI 18 bit (36 bit) Dual Channel	Open LDI 24 bit (48 bit) Dual Channel	FPD Link 18 bit (36 bit) Dual Channel	FPD Link 24 bit (48 bit) Dual Channel
LVDS_A0±	1	1	Odd Pixel G0	Odd Pixel G2	Odd Pixel G0	Odd Pixel G0
	2	1	Odd Pixel R5	Odd Pixel R7	Odd Pixel R5	Odd Pixel R5
	3	0	Odd Pixel R4	Odd Pixel R6	Odd Pixel R4	Odd Pixel R4
	4	0	Odd Pixel R3	Odd Pixel R5	Odd Pixel R3	Odd Pixel R3
	5	0	Odd Pixel R2	Odd Pixel R4	Odd Pixel R2	Odd Pixel R2
	6	1	Odd Pixel R1	Odd Pixel R3	Odd Pixel R1	Odd Pixel R1
	7	1	Odd Pixel R0	Odd Pixel R2	Odd Pixel R0	Odd Pixel R0
LVDS_A1±	1	1	Odd Pixel B1	Odd Pixel B3	Odd Pixel B1	Odd Pixel B1
	2	1	Odd Pixel B0	Odd Pixel B2	Odd Pixel B0	Odd Pixel B0
	3	0	Odd Pixel G5	Odd Pixel G7	Odd Pixel G5	Odd Pixel G5
	4	0	Odd Pixel G4	Odd Pixel G6	Odd Pixel G4	Odd Pixel G4
	5	0	Odd Pixel G3	Odd Pixel G5	Odd Pixel G3	Odd Pixel G3
	6	1	Odd Pixel G2	Odd Pixel G4	Odd Pixel G2	Odd Pixel G2
	7	1	Odd Pixel G1	Odd Pixel G3	Odd Pixel G1	Odd Pixel G1
LVDS_A2±	1	1	DE	DE	DE	DE
	2	1	VSYNC	VSYNC	VSYNC	VSYNC
	3	0	HSYNC	HSYNC	HSYNC	HSYNC
	4	0	Odd Pixel B5	Odd Pixel B7	Odd Pixel B5	Odd Pixel B5
	5	0	Odd Pixel B4	Odd Pixel B6	Odd Pixel B4	Odd Pixel B4
	6	1	Odd Pixel B3	Odd Pixel B5	Odd Pixel B3	Odd Pixel B3
	7	1	Odd Pixel B2	Odd Pixel B4	Odd Pixel B2	Odd Pixel B2
LVDS_A3±	1	1				
	2	1		Odd Pixel B1		Odd Pixel B7
	3	0		Odd Pixel B0		Odd Pixel B6
	4	0		Odd Pixel G1		Odd Pixel G7
	5	0		Odd Pixel G0		Odd Pixel G6
	6	1		Odd Pixel R1		Odd Pixel R7
	7	1		Odd Pixel R0		Odd Pixel R6
LVDS_ACLK±			LCLK=PCLK/14 SCLK=PCLK/2	LCLK=PCLK/14 SCLK=PCLK/2	LCLK=PCLK/14 SCLK=PCLK/2	LCLK=PCLK/14 SCLK=PCLK/2
LVDS_B0±	1	1	Even Pixel G0	Even Pixel G2	Even Pixel G0	Even Pixel G0
	2	1	Even Pixel R5	Even Pixel R7	Even Pixel R5	Even Pixel R5
	3	0	Even Pixel R4	Even Pixel R6	Even Pixel R4	Even Pixel R4
	4	0	Even Pixel R3	Even Pixel R5	Even Pixel R3	Even Pixel R3
	5	0	Even Pixel R2	Even Pixel R4	Even Pixel R2	Even Pixel R2
	6	1	Even Pixel R1	Even Pixel R3	Even Pixel R1	Even Pixel R1
	7	1	Even Pixel R0	Even Pixel R2	Even Pixel R0	Even Pixel R0
LVDS_B1±	1	1	Even Pixel B1	Even Pixel B3	Even Pixel B1	Even Pixel B1
	2	1	Even Pixel B0	Even Pixel B2	Even Pixel B0	Even Pixel B0
	3	0	Even Pixel G5	Even Pixel G7	Even Pixel G5	Even Pixel G5
	4	0	Even Pixel G4	Even Pixel G6	Even Pixel G4	Even Pixel G4
	5	0	Even Pixel G3	Even Pixel G5	Even Pixel G3	Even Pixel G3
	6	1	Even Pixel G2	Even Pixel G4	Even Pixel G2	Even Pixel G2
	7	1	Even Pixel G1	Even Pixel G3	Even Pixel G1	Even Pixel G1
LVDS_B2±	1	1				
	2	1				
	3	0				
	4	0	Even Pixel B5	Even Pixel B7	Even Pixel B5	Even Pixel B5
	5	0	Even Pixel B4	Even Pixel B6	Even Pixel B4	Even Pixel B4
	6	1	Even Pixel B3	Even Pixel B5	Even Pixel B3	Even Pixel B3
	7	1	Even Pixel B2	Even Pixel B4	Even Pixel B2	Even Pixel B2
LVDS_B3±	1	1				
	2	1		Even Pixel B1		Even Pixel B7
	3	0		Even Pixel B0		Even Pixel B6
	4	0		Even Pixel G1		Even Pixel G7
	5	0		Even Pixel G0		Even Pixel G6
	6	1		Even Pixel R1		Even Pixel R7
	7	1		Even Pixel R0		Even Pixel R6
LVDS_BCLK±			LCLK=PCLK/14 SCLK=PCLK/2	LCLK=PCLK/14 SCLK=PCLK/2	LCLK=PCLK/14 SCLK=PCLK/2	LCLK=PCLK/14 SCLK=PCLK/2

3.1.8. LVDS PCB Routing Considerations

The EDM standard routing requirements for LVDS and Embedded Display Port interface are identical and all technology requirements are embedded on the EDM module. While using EDM carrier boards one should only have to concern on which interface the EDM module supports and match a compatible LCD panel. No modifications are required on the EDM carrier board while converting from LVDS based panels towards embedded Display Port panels as long as both LCD and EDM module support the same display interface.

Route LVDS signals as differential pairs (excluding the five single-ended support signals), with a 100-Ω differential impedance and a 55-Ω, single-ended impedance. Ideally, a LVDS pair is routed on a single layer adjacent to a ground plane. LVDS pairs should not cross plane splits. Keep layer transitions to a minimum and reference LVDS pairs to a power plane if necessary. The power plane should be well-bypassed.

Length-matching between the two lines that make up an LVDS pair (“intra-pair”) and between different LVDS pairs (“inter-pair”) is required. Intra-pair matching is tighter than the inter-pair matching.

All LVDS pairs should have the same environment, including the same reference plane and the same number of vias.

LVDS routing rules are summarized in “4.5.1. LVDS and eDP Signaling Details and Routing Guideline” on page 114 below.

3.2. Embedded Display Port Interface

Embedded DisplayPort is an open, industry standard digital display interface that is under development within the Video Electronics Standards Association (VESA). The embedded DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its embedded liquid crystal display (LCD).

3.2.1. Embedded Display Port Signal Description

Table 9 - Primary Embedded Display Port Signal Description

Pin #	EDM	Signal	V	I/O	Description
E3_9	1 / 2	eDP0_LANE0-	eDP	O	Embedded Display Port primary channel differential lane 0 signal
E3_10	1 / 2	eDP0_LANE0+	eDP	O	
3	1 / 2	eDP0_LANE1-	eDP	O	Embedded Display Port primary channel differential lane 1 signal
5	1 / 2	eDP0_LANE1+	eDP	O	
9	1 / 2	eDP0_LANE2-	eDP	O	Embedded Display Port primary channel differential lane 2 signal
11	1 / 2	eDP0_LANE2+	eDP	O	
15	1 / 2	eDP0_LANE3-	eDP	O	Embedded Display Port primary channel differential lane 3 signal
17	1 / 2	eDP0_LANE3+	eDP	O	
21	1 / 2	eDP0_AUX-	eDP	O	Embedded Display Port primary differential pair Auxiliary signal
23	1 / 2	eDP0_AUX+	eDP	O	
33	1 / 2	eDP0_SELFTEST	CMOS 3.3V	I	Embedded Display Port Detection pin
35	1 / 2	eDP0_HPD	CMOS 3.3V	I	Embedded Display Port Hot Plug Detection pin

Note : Signals with gray background are shared with the LVDS signals.

Table 10 - Secondary Embedded Display Port Signal Description

Pin #	EDM	Signal	V	I/O	Description
2	2	eDP1_LANE0-	eDP	O	Embedded Display Port secondary channel differential lane 0 signal
4	2	eDP1_LANE0+	eDP	O	
8	2	eDP1_LANE1-	eDP	O	Embedded Display Port secondary channel differential lane 1 signal
10	2	eDP1_LANE1+	eDP	O	
14	2	eDP1_LANE2-	eDP	O	Embedded Display Port secondary channel differential lane 2 signal
16	2	eDP1_LANE2+	eDP	O	
20	2	eDP1_LANE3-	eDP	O	Embedded Display Port secondary channel differential lane 3 signal
22	2	eDP1_LANE3+	eDP	O	
26	2	eDP1_AUX-	eDP	O	Embedded Display Port secondary differential pair Auxiliary signal
28	2	eDP1_AUX+	eDP	O	
38	2	eDP1_SELFTEST	CMOS 3.3V	I	Embedded Display Port Detection pin
40	2	eDP1_HPD	CMOS 3.3V	I	Embedded Display Port Hot Plug Detection pin

Note : Signals with gray background are shared with the LVDS signals.

3.2.2. Embedded Display Port PCB Routing Considerations

The EDM standard routing requirements for LVDS and Embedded Display Port interface are identical and all technology requirements are embedded on the EDM module. While using EDM carrier boards one should only have to concern on which interface the EDM module supports and match a compatible LCD panel. No modifications are required on the EDM carrier board while converting from LVDS based panels towards embedded Display Port panels as long as both LCD and EDM module support the same display interface.

Route embedded DisplayPort signals as differential pairs, with a 100-Ω differential impedance and a 55-Ω, single-ended impedance. Ideally, a eDP pair is routed on a single layer adjacent to a ground plane. eDP pairs should not cross plane splits. Keep layer transitions to a minimum and reference eDP pairs to a power plane if necessary. The power plane should be well-bypassed.

Length-matching between the two lines that make up an eDP pair (“intra-pair”) and between different eDP pairs (“inter-pair”) is required. Intra-pair matching is tighter than the inter-pair matching.

All eDP pairs should have the same environment, including the same reference plane and the same number of vias.

eDP routing rules are summarized in “4.5.1. LVDS and eDP Signaling Details and Routing Guideline” on page 114 below.

3.3. HDMI (High Definition Multi-Media Interface)

The EDM module supports up to two HDMI interfaces. This interface is shared with the DisplayPort interface signals and information about configuration is mandatory to be present in the EDM module vendors' documentation.

The High-Definition Multi-media is an industry-supported digital audio/video interface. HDMI provides an interface between any compatible digital audio/video source and a compatible digital audio and/or video monitor.

HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. It is independent of the various DTV standards such as ATSC, DVB(-T,-S,-C), as these are encapsulations of the MPEG data streams, which are passed off to a decoder, and output as uncompressed video data, which can be high-definition. This video data is then encoded into TMDS for transmission digitally over HDMI. HDMI also includes support for 8-channel uncompressed digital audio. Beginning with version 1.2, HDMI supports up to 8 channels of one-bit audio.

3.3.1. HDMI Signal Description

Table 11 - Primary HDMI Signal Description

Pin #	EDM	Signal	V	I/O	Description
43	1 / 2	HDMI1_CLK+	HDMI	O	HDMI differential pair clock signal
45	1 / 2	HDMI1_CLK-	HDMI	O	
49	1 / 2	HDMI1_D0+	HDMI	O	HDMI differential pair 0 signal
51	1 / 2	HDMI1_D0-	HDMI	O	
55	1 / 2	HDMI1_D1+	HDMI	O	HDMI differential pair 1 signal
57	1 / 2	HDMI1_D1-	HDMI	O	
61	1 / 2	HDMI1_D2+	HDMI	O	HDMI differential pair 2 signal
63	1 / 2	HDMI1_D2-	HDMI	O	
67	1 / 2	HDMI1_HPD DP1_HPD	CMOS 3.3V	I	HDMI/DP Hot plug detection signal that serves as an interrupt request
69	1 / 2	HDMI1_CAD	HDMI	I / O	Cable Adaptor Detect
71	1 / 2	HDMI1_CEC	HDMI	I / O	HDMI Consumer Electronics Control
73	1 / 2	I2C_SCL	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus clock line
75	1 / 2	I2C_SDA	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus data line

Note : Signals with gray background are shared with the Display Port signals.

Table 12 - Secondary HDMI Signal Description

Pin #	EDM	Signal	V	I/O	Description
44	2	HDMI2_CLK+	HDMI	O	HDMI differential pair clock signal
46	2	HDMI2_CLK-	HDMI	O	
50	2	HDMI2_D0+	HDMI	O	HDMI differential pair 0 signal
52	2	HDMI2_D0-	HDMI	O	
56	2	HDMI1_D1+	HDMI	O	HDMI differential pair 1 signal
58	2	HDMI2_D1-	HDMI	O	
62	2	HDMI2_D2+	HDMI	O	HDMI differential pair 2 signal
64	2	HDMI2_D2-	HDMI	O	
68	2	HDMI2_HPD	CMOS 3.3V	I	HDMI Hot plug detection signal that serves as an interrupt request
70	2	HDMI2_CAD	HDMI	I / O	Cable Adaptor Detect
72	2	HDMI2_CEC	HDMI	I / O	HDMI Consumer Electronics Control
74	2	I2C_SCL	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus clock line
76	2	I2C_SDA	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus data line

Note : Signals with gray background are shared with the Display Port signals.

3.3.2. HDMI Connector

The standard Type A HDMI connector has 19 pins and widely being used on televisions and other multimedia equipment.

Figure 17 - HDMI Connector Pin-out

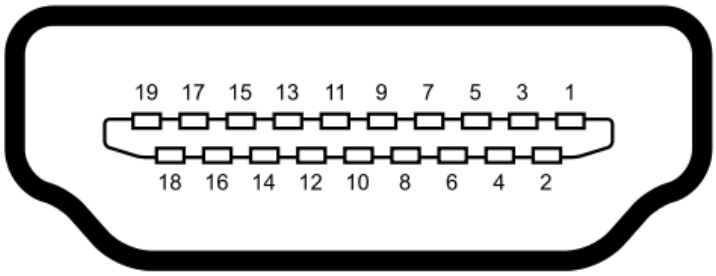


Table 13 - HDMI Connector Pin-out

Pin #	Signal	Description	Pin #	Signal	Description
1	HDMI_D2+	HDMI differential pair 2 signal	2	Shield_D2	Shield of data pair 2
3	HDMI_D2-		4	HDMI_D1+	HDMI differential pair 1 signal
5	Shield_D1	Shield of data pair 1	6	HDMI_D1-	
7	HDMI_D0+	HDMI differential pair 2 signal	8	Shield_D0	Shield of data pair 0
9	HDMI_D0-		10	HDMI_CLK+	HDMI differential clock signal
11	Shield_CLK	Shield of Clock pair	12	HDMI_CLK-	
13	CEC	Consumer Electronics Control Interface	14	RSVD	Reserved
15	DDC Clock	DDC based control clock signal	16	DDC Data	DDC based control data signal
17	GND	Ground	18	+5V	5V Power
19	HPD	Hot plug detect			

3.3.3. HDMI PCB Routing Considerations

Route the HDMI display signals as differential pairs, with a 100-Ω differential impedance and a 55-Ω, single ended impedance. The length of the differential signals must be kept as close to the same as possible. The maximum length difference must not exceed 100mils for any of the pairs relative to each other. Spacing between the differential pair traces should be more than 2x the trace width to reduce trace-to-trace couplings.

For example, having wider gaps between differential pair HDMI traces will minimize noise coupling. It is also strongly advised that ground not be placed adjacent to the HDMI traces on the same layer. There should be a minimum distance of 30mils between the HDMI trace and any ground on the same layer.

HDMI routing rules are summarized in “4.5.2. HDMI and DP Signaling Details and Routing Guideline” on page 115 below

3.3.4. EMI / ESD Protection

To protect the HDMI interface of the Module from over-voltage caused by electrostatic discharge (ESD), EMI noise filtering and electrical fast transients (EFT), a HDMI Transmitter Port Protection and Interface Device can be implemented on the Carrier Board design.

A common way of implementation is by using ' CM2020-00TR HDMI Transmitter Port Protection and Interface Device from ON Semiconductor (http:// www.onsemi.com).

3.4. DisplayPort (DP) Interface

DisplayPort is a digital display interface developed by the Video Electronics Standards Association (VESA). The interface is primarily used to connect a video source to a display device such as a computer monitor, though it can also be used to transmit audio, USB, and other forms of data.

Dual-mode DisplayPort can directly emit single-link HDMI and DVI signals using a simple passive adapter that adjusts for the lower voltages required by DisplayPort. When dual-mode chipset detects that a DVI or HDMI passive adapter is attached, it switches to DVI/HDMI mode which uses the 4-lane main DisplayPort link and the AUX channel link to transmit 3 TMDS signals, a clock signal and Display Data Channel data/clock. Dual-mode ports are marked with the DP++ logo; most current DisplayPort graphics cards and monitors offer this mode.

A notable limitation is that dual-mode can only transmit single-link DVI/HDMI, as the number of pins in the DisplayPort connector is insufficient for dual-link connections; an active converter is needed for Dual-Link DVI (and analog component video such as VGA, since it employs digital to analog conversion). Active conversion can be powered by +3.3 V wire in the DisplayPort connector, but some active adapters require external power.

3.4.1. Display Port Signal Description

Table 14 - Primary Display Port Signal Description

Pin #	EDM	Signal	V	I/O	Description
43	1 / 2	DP1_LANE3+	DP	O	Display Port differential pair lane 3 signal
45	1 / 2	DP1_LANE3-	DP	O	
49	1 / 2	DP1_LANE2+	DP	O	Display Port differential pair lane 2 signal
51	1 / 2	DP1_LANE2-	DP	O	
55	1 / 2	DP1_LANE1+	DP	O	Display Port differential pair lane 1 signal
57	1 / 2	DP1_LANE1-	DP	O	
61	1 / 2	DP1_LANE0+	DP	O	Display Port differential pair lane 0 signal
63	1 / 2	DP1_LANE0-	DP	O	
67	1 / 2	HDMI1_HPD DP1_HPD	CMOS 3.3V	I	HDMI/DP Hot plug detection signal that serves as an interrupt request
69	1 / 2	DP1_CONFIG1	DP	I / O	Display Port Config 1 signal
71	1 / 2	DP1_CONFIG2	DP	I / O	Display Port Config 2 signal
73	1 / 2	DP1_AUX+	DP	O	Display Port differential pair Auxiliary signal
75	1 / 2	DP1_AUX-	DP	O	

Note : Signals with gray background are shared with the HDMI Port signals.

Table 15 - Secondary Display Port Signal Description

Pin #	EDM	Signal	V	I/O	Description
44	2	DP2_LANE3+	DP	O	Display Port differential pair lane 3 signal
46	2	DP2_LANE3-	DP	O	
50	2	DP2_LANE2+	DP	O	Display Port differential pair lane 2 signal
52	2	DP2_LANE2-	DP	O	
56	2	DP2_LANE1+	DP	O	Display Port differential pair lane 1 signal
58	2	DP2_LANE1-	DP	O	
62	2	DP2_LANE0+	DP	O	Display Port differential pair lane 0 signal
64	2	DP2_LANE0-	DP	O	
68	2	HDMI2_HPD DP2_HPD	CMOS 3.3V	I	HDMI/DP Hot plug detection signal that serves as an interrupt request
70	2	DP2_CONFIG1	DP	I / O	Display Port Config 1 signal
72	2	DP2_CONFIG2	DP	I / O	Display Port Config 2 signal
74	2	DP2_AUX+	DP	O	Display Port differential pair Auxiliary signal
76	2	DP2_AUX-	DP	O	

Note : Signals with gray background are shared with the HDMI Port signals.

3.4.2. DisplayPort Connector Pin-out

The standard DisplayPort connector has 20 pins.

Figure 18 - Display Port Connector

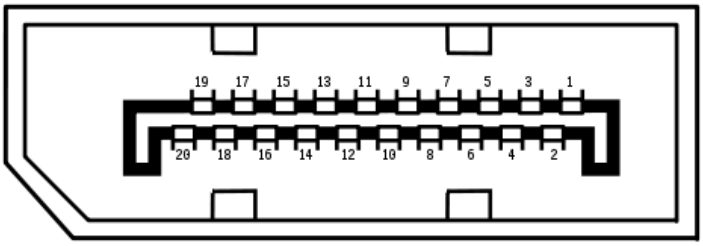


Table 16 - DisplayPort Connector Pin-out

Pin #	Signal	Description	Pin #	Signal	Description
1	DP_LANE0+	DisplayPort Lane 0 differential signal	2	GND	Ground
3	DP_LANE0-		4	DP_LANE1+	DisplayPort Lane 1 differential signal
5	GND	Ground	6	DP_LANE1-	
7	DP_LANE2+	DisplayPort Lane 2 differential signal	8	GND	Ground
9	DP_LANE2-		10	DP_LANE3+	DisplayPort Lane 3 differential signal
11	GND	Ground	12	DP_LANE3-	
13	CONFIG1	Display Port Config 1 signal	14	CONFIG2	Display Port Config 2 signal
15	DP_AUX+	Display Port differential pair Auxiliary signal	16	GND	Ground
17	DP_AUX-		18	DP_HPD#	Hot Plug Detect
19	RETURN	Return for Power	20	DP_PWR	Power For Connector

3.4.3. DisplayPort PCB Routing Considerations

Route the DisplayPort display signals as differential pairs, with a 100-Ω differential impedance and a 55-Ω, single ended impedance. The length of the differential signals must be kept as close to the same as possible. The maximum length difference must not exceed 100mils for any of the pairs relative to each other. Spacing between the differential pair traces should be more than 2x the trace width to reduce trace-to-trace couplings.

For example, having wider gaps between differential pair DisplayPort traces will minimize noise coupling. It is also strongly advised that ground not be placed adjacent to the DisplayPort traces on the same layer. There should be a minimum distance of 30mils between the DisplayPort trace and any ground on the same layer.

DisplayPort routing rules are summarized in “4.5.2. HDMI and DP Signaling Details and Routing Guideline” on page 115 below

3.5. Digital Display Sub-System (DSS) or TTL Interface

Transistor–transistor logic (TTL) is a low level low-cost digital RGB interface that connects directly from the EDM module to small size TFT Liquid Crystal Displays.

The low level interface of TFT display panels use either single ended TTL 3.3V that transmits the pixel clock, horizontal sync, vertical sync, digital red, digital green, digital blue in parallel.

3.5.1. Digital Display Sub-System (DSS) or TTL Interface Signal Description

Table 17 - Digital Display Sub-System (DSS) or TTL Interface Signal Description

Pin #	EDM	Signal	V	I/O	Description
2	1	LCD_D0	TTL	O	LCD Pixel Data bit 0
4	1	LCD_D1	TTL	O	LCD Pixel Data bit 1
8	1	LCD_D2	TTL	O	LCD Pixel Data bit 2
10	1	LCD_D3	TTL	O	LCD Pixel Data bit 3
14	1	LCD_D4	TTL	O	LCD Pixel Data bit 4
16	1	LCD_D5	TTL	O	LCD Pixel Data bit 5
20	1	LCD_D6	TTL	O	LCD Pixel Data bit 6
22	1	LCD_D7	TTL	O	LCD Pixel Data bit 7
26	1	LCD_D8	TTL	O	LCD Pixel Data bit 8
28	1	LCD_D9	TTL	O	LCD Pixel Data bit 9
32	1	LCD_D10	TTL	O	LCD Pixel Data bit 10
34	1	LCD_D11	TTL	O	LCD Pixel Data bit 11
36	1	LCD_D12	TTL	O	LCD Pixel Data bit 12
38	1	LCD_D13	TTL	O	LCD Pixel Data bit 13
40	1	LCD_D14	TTL	O	LCD Pixel Data bit 14
44	1	LCD_D15	TTL	O	LCD Pixel Data bit 15
46	1	LCD_D16	TTL	O	LCD Pixel Data bit 16
50	1	LCD_D17	TTL	O	LCD Pixel Data bit 17
52	1	LCD_D18	TTL	O	LCD Pixel Data bit 18
56	1	LCD_D19	TTL	O	LCD Pixel Data bit 19
58	1	LCD_D20	TTL	O	LCD Pixel Data bit 20
62	1	LCD_D21	TTL	O	LCD Pixel Data bit 21
64	1	LCD_D22	TTL	O	LCD Pixel Data bit 22
68	1	LCD_D23	TTL	O	LCD Pixel Data bit 23
70	1	LCD_CLK	TTL	O	LCD Pixel Clock
72	1	LCD_HSYNC	TTL	O	LCD Horizontal Synchronization
74	1	LCD_VSYNC	TTL	O	LCD Vertical Synchronization
76	1	LCD_CNTRST	TTL	O	LCD backlight control
78	1	LCD_DRD Y	TTL	O	LCD dot enable pin signal
80	1	LCD_VDDEN	TTL	O	LCD Voltage On
82	1	LCD_BKLEN	TTL	O	LCD Backlight Control

3.5.2. TTL Hardware and Software Mapping

To connect the EDM module digital display signals to either an 18 or 24 bit TTL LCD panel the following table is recommended.

Pin #	EDM	Signal	24 bit	18 bit
2	1	LCD_D0	B0	
4	1	LCD_D1	B1	
8	1	LCD_D2	B2	B0
10	1	LCD_D3	B3	B1
14	1	LCD_D4	B4	B2
16	1	LCD_D5	B5	B3
20	1	LCD_D6	B6	B4
22	1	LCD_D7	B7	B5
26	1	LCD_D8	G0	
28	1	LCD_D9	G1	
32	1	LCD_D10	G2	G0
34	1	LCD_D11	G3	G1
36	1	LCD_D12	G4	G2
38	1	LCD_D13	G5	G3
40	1	LCD_D14	G6	G4
44	1	LCD_D15	G7	G5
46	1	LCD_D16	R0	
50	1	LCD_D17	R1	
52	1	LCD_D18	R2	R0
56	1	LCD_D19	R3	R1
58	1	LCD_D20	R4	R2
62	1	LCD_D21	R5	R3
64	1	LCD_D22	R6	R4
68	1	LCD_D23	R7	R5

3.6. Audio Interface

The EDM specifications provide a wide range of audio interfaces and options ranging from HD Audio to I^2S and S/PDIF. It is recommended to evaluate current and future design concepts and prepare the carrier board to incorporate HD Audio and I^2S audio codec's.

3.6.1. I^2S Audio

I^2S, also known as Inter-IC Sound, Integrated Interchip Sound, or IIS, is an electrical serial bus interface standard used for connecting digital audio devices together. It is used to communicate PCM audio data between integrated circuits in an electronic device. The I^2S bus separates clock and serial data signals, resulting in a lower jitter than is typical of communications systems that recover the clock from the data stream.

I²S consists of a bit clock, a word select and data lines. The I²S protocol outlines one specific type of PCM digital audio communication with defined parameters outlined in the Philips specifications.

The bit clock pulses once for each discrete bit of data on the data lines. The bit clock will operate at a frequency which is a multiple of the sample rate. The bit clock frequency multiplier depends on number of bits per channel, times the number of channels. So, for example, CD Audio with a sample frequency of 44.1 kHz, with 32 bits of precision per (2) stereo channels will have a bit clock frequency of 2.8224 MHz (44.1 kHz * 32 * 2). The word select clock lets the device know whether channel 1 or channel 2 is currently being sent, since I²S allows two channels to be sent on the same data line. For stereo material, the I²S specification states that left audio is transmitted on the low-cycle of the word select clock and the right channel is transmitted on the high-cycle. The word select clock is a 50% duty-cycle signal that has the same frequency as the sample frequency.

The first data bit following a word select clock transition is the LSB of the previous word.

In audio equipment the I²S is sometimes used as an external link between the CD transport and a separate box DAC, as opposed to purely internal connection within one box player. This is considered, by some audiophiles, to be a higher quality connection than the commonly used AES/EBU or Toslink or S/PDIF standards. There is no standard interconnecting cable for I²S. Some manufacturers provide simply three BNC connectors, an 8P8C ("RJ45") socket or a DE-9 or DIN connectors.

3.6.2. I²S Audio Signal Description

Table 18 - Primary I^2S Signal Description

Pin #	EDM	Signal	V	I/O	Description
187	1 / 2	I2S1_RXD	CMOS 3.3V	I	Primary Integrated Interchip Sound (I^2S) channel receive data line
189	1 / 2	I2S1_TXFS	CMOS 3.3V	O	Primary Integrated Interchip Sound (I^2S) channel frame synchronization signal
191	1 / 2	I2S1_TXD	CMOS 3.3V	O	Primary Integrated Interchip Sound (I^2S) channel transmit data line
193	1 / 2	I2S1_TXC	CMOS 3.3V	O	Primary Integrated Interchip Sound (I^2S) channel word clock signal
195	1 / 2	I2S1_CLK	CMOS 3.3V	O	Primary Integrated Interchip Sound (I^2S) channel master clock signal

Table 19 - Secondary I^2S Signal Description

Pin #	EDM	Signal	V	I/O	Description
186	1	I2S2_RXD	CMOS 3.3V	I	Secondary Integrated Interchip Sound (I^2S) channel receive data line
188	1	I2S2_TXFS	CMOS 3.3V	O	Secondary Integrated Interchip Sound (I^2S) channel frame synchronization signal
190	1	I2S2_TXD	CMOS 3.3V	O	Secondary Integrated Interchip Sound (I^2S) channel transmit data line
192	1	I2S2_TXC	CMOS 3.3V	O	Secondary Integrated Interchip Sound (I^2S) channel word clock signal
194	1	I2S2_CLK	CMOS 3.3V	O	Secondary Integrated Interchip Sound (I^2S) channel master clock signal

Note: The secondary I^2S Signals are only available on the EDM Type 1 modules and care should be taken if EDM Type 2 modules are used.

3.6.3. S/PDIF Audio

S/PDIF (Sony/Philips Digital Interconnect Format) is a type of digital audio interconnects cable used in consumer audio equipment to output audio over reasonably short distances. The signal is transmitted over either a coaxial cable with RCA connectors or a fibre optic cable with TOSLINK connectors. S/PDIF is based on the professional AES3 interconnect standard. S/PDIF can carry two channels of PCM audio or a multi-channel compressed surround sound format such as Dolby Digital or DTS.

3.6.4. S/PDIF Audio Signal Description

Table 20 - S/PDIF Audio Signal Description

Pin #	EDM	Signal	V	I/O	Description
196	1 / 2	SPDIF_OUT	SPDIF	O	Sony / Philips Digital Interconnect Format Audio output

3.6.5. HD AUDIO

Intel High Definition Audio (also called HD Audio) refers to the specification released by Intel in 2004 for delivering high-definition audio that is capable of playing back more channels at higher quality than previous integrated audio codec's like AC'97.

Hardware based on Intel HD Audio specifications is capable of delivering 192-kHz 32-bit quality for two channels, and 96-kHz 32-bit for up to eight channels.

3.6.6. HD Audio Signal Description

The EDM Type 2 specification allocates five pins to support digital High-Definition (HD) audio interface to audio codec on the carrier board. High-definition (HD) audio uses the same digital-signal interface as AC '97 audio. Codecs for AC '97 and HD Audio are different.

Pin #	EDM	Signal	V	I/O	Description
186	2	HDA_SYNC	CMOS 3.3V	O	HD Audio/AC'97 Serial Bus Synchronization
188	2	HDA_BITCLK	CMOS 3.3V	O	HD Audio/AC'97 24Mhz Serial bit Clock from Codec
190	2	HDA_nRST	CMOS 3.3V	O	HD Audio/AC'97 Codec reset
192	2	HDA_SDI	CMOS 3.3V	I	HD Audio/AC'97 Serial Data Input from Codec
194	2	HDA_SDO	CMOS 3.3V	O	HD Audio/AC'97 Serial Data Output to Codec

Note: The HDA Signals are only available on the EDM Type 2 modules and care should be taken if EDM Type 1 modules are used.

Information about which HD audio interface is supported on the EDM Module can be found in the corresponding EDM Module vendors' documentation.

Some EDM Modules support both the AC'97 and HDA Interface. In these cases the EDM Module's 'BIOS Setup Program' offers a setup entry to choose which interface should be utilized. Only audio codecs that match this setting will work properly. AC'97 and High Definition Audio codecs cannot be mixed on the same link or behind the same controller.

Clocking over the signal 'AC_BITCLK' is derived from a 24.576 MHz crystal or crystal oscillator provided by the primary codec in AC97 implementations. The crystal is not required in HDA implementations. For crystal or crystal oscillator requirements, refer to the datasheet of the codec.

3.6.7. Audio PCB Routing Considerations

The implementation of proper component placement and routing techniques will help to ensure that the maximum performance available from the codec is achieved. Routing techniques that should be observed include properly isolating the codec, associated audio circuitry, analog power supplies and analog ground planes from the rest of the Carrier Board. This includes split planes and the proper routing of signals not associated with the audio section.

The following is a list of basic recommendations:

- Traces must be routed with a target impedance of 55Ω with an allowed tolerance of ±15%. Ground return paths for the analog signals must be given special consideration.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Locate the analog and digital signals as far as possible from each other.
- Partition the Carrier Board with all analog components grouped together in one area and all digital components in another.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Provide separate analog and digital ground planes with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between the planes must be a minimum of 0.05 inch wide.
- Route analog power and signal traces over the analog ground plane. Route digital power and signal traces over the digital ground plane.
- Position the bypassing and decoupling capacitors close to the IC pins with wide traces to reduce impedance.
- Place the crystal or oscillator (depending on the codec used) as close as possible to the codec. (HDA implementations generally do not require a crystal at the codec)
- Do not completely isolate the analog/audio ground plane from the rest of the Carrier Board ground plane. Provide a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between the planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main Carrier Board ground. That is, no signal should cross the split/gap between the ground planes, because this would cause a ground loop, which in turn would greatly increase EMI emissions and degrade the analog and digital signal quality.

3.7. Gigabit Ethernet Interface

EDM Modules provide one LAN port. The 8-wire 10/100/1000BaseT Gigabit Ethernet interface compliant to the IEEE 802.3ab specification is the preferred interface for this port, with the EDM Module PHY responsible for implementing auto-negotiation of 10/100BaseTX or 10/100/1000BaseT operation.

3.7.1. Gigabit Ethernet Signal Description

The LAN interface of the EDM Module consists of 4 pairs of low voltage differential pair signals designated from 'GBE_MDI0' (+ and -) to 'GBE0_MDI3' (+ and -) plus additional control signals for link activity indicators. These signals can be used to connect to a 10/100/1000BaseT RJ45 connector with integrated or external isolation magnetic on the Carrier Board. The corresponding LAN differential pair and control signals can be found on the EDM edge connector, as listed in “Table 21 - Gigabit Ethernet Interface Signal Description” below.

Table 21 - Gigabit Ethernet Interface Signal Description

Pin #	EDM	Signal	V	I/O	Description
E4_2	1 / 2	GBE_MDI0+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 0 signal
E4_3	1 / 2	GBE_MDI0-	LAN	I/O	
E4_5	1 / 2	GBE_MDI1+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 1 signal
E4_6	1 / 2	GBE_MDI1-	LAN	I/O	
E3_2	1 / 2	GBE_MDI2+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 2 signal
E3_3	1 / 2	GBE_MDI2-	LAN	I/O	
E3_5	1 / 2	GBE_MDI3+	LAN	I/O	Gigabit Ethernet Media Dependent Interface (MDI) differential pair 3 signal
E3_6	1 / 2	GBE_MDI3-	LAN	I/O	
E3_7	1 / 2	LED1_ACT	CMOS 3.3V	O	Gigabit Ethernet LED Activity indicator
E4_8	1 / 2	LED1_nLink100	CMOS 3.3V	O	Gigabit Ethernet 100Mbit/sec LED link indicator
E4_9	1 / 2	LED1_nLink1000	CMOS 3.3V	O	Gigabit Ethernet 1000Mbit/sec LED link indicator

3.7.2. Gigabit Ethernet RJ-45 Connector Pin-out

Figure 19 - Gigabit Ethernet RJ-45 Connector

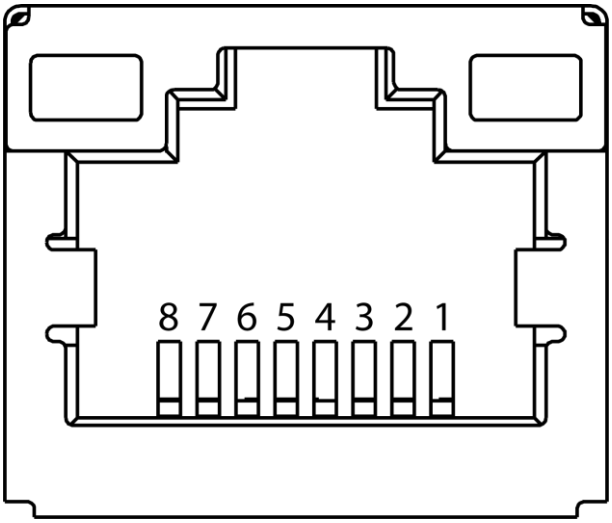


Table 22 - Gigabit Ethernet RJ-45 Connector Pin-out

Pin #	1000 Mbps	100 Mbps	10 Mbps
1	MDI0+	Transmit Data+	Transmit Data+
2	MDI0-	Transmit Data-	Transmit Data-
3	MDI1+	Receive Data+	Receive Data+
4	MDI2+		
5	MDI2-		
6	MDI1-	Receive Data-	Receive Data-
7	MDI3+		
8	MDI3-		

NOTE: The EDM carrier board implementation and circuitry should always be prepared to support 10/100/1000Mbps Ethernet.

3.7.3. Gigabit Ethernet Considerations

The EDM module specification utilizes the IEEE 802.3 PHY / MDI interface circuit resources between the module and carrier board, with the Ethernet PHY located on the EDM module and the coupling magnetics located on the carrier board, preferably physically integrated in the RJ-45 receptacle housing associated with the port.

In order to meet the signal performance requirements for MDI signals as defined in the IEEE 802.3-2005 specification and to ensure maximum interoperability of EDM modules and carrier boards, the PHY / Magnetics circuit should be implemented using the following guidelines.

On the EDM module:

- The termination resistors should be placed on the EDM module, physically as close to the PHY device receive inputs as practical.
- The signals associated with each signaling pair should be independently matched in length to within 6mm (approx. 240 mils)
- The crystal oscillator and its resistors and capacitors must be placed within 12mm (approx. 500mils) of the PHY.
- The power supply decoupling capacitors need to be placed within 7mm (approx. 280mils) of the power supply.
- The 49.9 ohm pull-up resistors on the differential lines, must be placed within 10mm (approx. 400mils) of the PHY device. This ensures the transmit path is identical between the TX and RX
- The strapping resistors need to be located within 20mm (approx. 800mils) of the Ethernet PHY to ensure the voltage into the pin at boot-up is at the correct Vih or Vil level.

On the EDM carrier board:

- The carrier board should provide a full 8-wire (10/100/1000baseT) interface circuit to the EDM module.
- The center tap reference signal should be routed from the EDM module connector to the secondary side center tap of each transformer as defined in the IEEE 802.3-2005 specification, without any series resistance or impedance circuits.
- The signals associated with each signaling pair should be independently matched in length to within 6mm (approx. 240 mils).
- The carrier board design should utilize a coupling transformer capable of interoperating with the largest possible number of PHY devices.
- The carrier board design should have the primary side and secondary side center tap termination components (75 Ω resistors and 100 nF capacitors, respectively) placed physically as close to the coupling transformer as possible.
- The coupling transformer should be placed no further than 100mm (3.9”) from the EDM module connector on the carrier board.

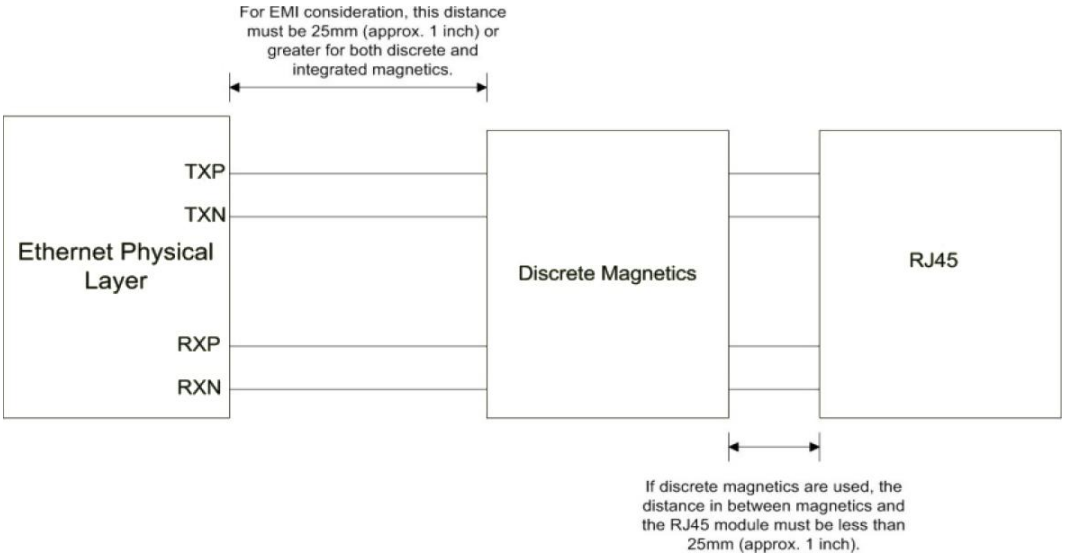
- It is recommended that the carrier board use a RJ-45 connector with an integrated transformer. However, if a discrete coupling transformer is used, the transformer must be placed no further than 25mm (1.0”) from the RJ-45 receptacle.

As there are a large number of Ethernet coupling transformers on the market, it is strongly recommended that the carrier board vendor documents the transformer used in this interface circuit, in order to facilitate interoperability analysis between EDM modules and carrier boards. It is also recommended that the EDM module vendor identify the specific PHY component used on the EDM module.

Table 23 - Recommended LAN Magnetic Modules

Manufacturer	Partnumber	Technology	Description
Pulse Engineering	H5007	10/100/1000BaseT	Discrete magnetics module
Pulse Engineering	JK0-0036	10/100/1000BaseT	RJ45 jack with integrated magnetics and activity LEDs
Bel Fuse	S558-5999–P3	10/100/1000BaseT	Discrete magnetics module
Pulse	JW0A1P01R-E	10/100/1000BaseT	RJ45 jack with integrated magnetics and USB jacks
Foxconn	UB11123-J51	10/100/1000BaseT	RJ45 jack with integrated magnetics and USB jacks

Figure 20 - Gigabit Ethernet Magnetics Considerations



3.7.4. Gigabit Ethernet LAN PCB Routing Considerations

The 8-wire PHY / MDI circuit is required to meet a specific waveform template and associated signal integrity requirements defined in the IEEE 802.3-2005 specification. In order to meet these requirements, the routing rules “4.5.3. Gigabit Ethernet Signaling Details and Routing Guideline” on page 116 should be observed on the carrier board.

The LED status signals driven by the EDM module to the carrier board are low frequency signals that do not have any signal integrity or trace routing requirements beyond generally accepted design practices for such signals.

3.7.5. Reference Ground Isolation and Coupling

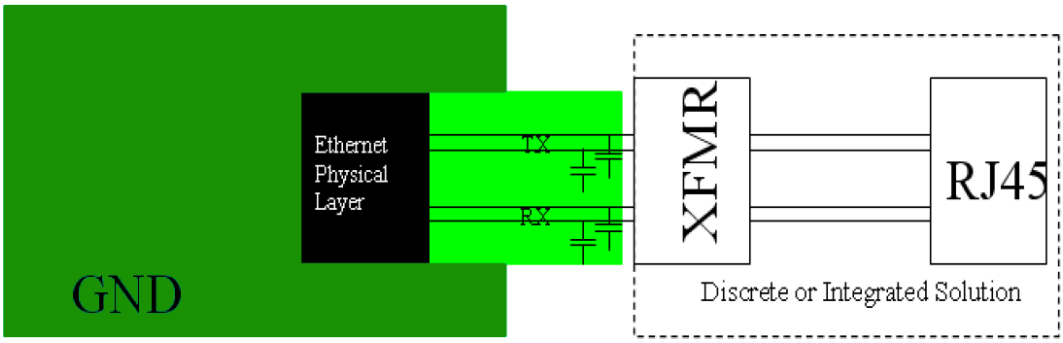
The carrier board should maintain a well-designed analog ground plane around the components on the primary side of the transformer between the transformer and the RJ-45 receptacle. The analog ground plane is bonded to the shield of the external cable through the RJ-45 connector housing.

The analog ground plane should be coupled to the carrier’s digital logic ground plane using a capacitive coupling circuit that meets the ground plane isolation requirements defined in the 802.3-2005 specification. It is recommended that the carrier board PCB design maintain a minimum 30 mil gap between the digital logic ground plane and the analog ground plane.

It's recommended to place an optional GND to SHIELDGND connection near the RJ-45 connector to improve EMI and ESD capabilities.

The plane area underneath the magnetic module should be left empty. This free area is to keep transformer induced noise away from the power and system ground planes. The isolated ground, also called chassis ground, connects directly to the fully shielded RJ45 connector. For better isolation it is also important to maintain a gap between chassis ground and system ground that is wider than 60mils. For ESD protection, a 3kV high voltage capability capacitor is recommended to connect to this chassis ground. Additionally, a ferrite bead can be placed parallel to the capacitor.

Figure 21 - Gigabit Ethernet Reference Ground Isolation and Coupling



3.8. PCI Express

PCI Express is a serial bus which uses two low-voltage differential LVDS pairs, at 2.5Gb/s (Gen2) or 5.0Gb/s (Gen3) in each direction [one transmit, and one receive pair] with a high-bandwidth, low pin count, serial and interconnect technology.

PCI Express architecture provides a high performance I/O infrastructure for Desktop Platforms with transfer rates starting at 2.5 Giga transfers per second over a x1 PCI Express lane for Gigabit Ethernet, TV Tuners, 1394a/b controllers, and general purpose I/O. PCI Express architecture provides a high performance graphics infrastructure for Desktop Platforms.

The broad adoption of PCI Express in the mobile, enterprise and communication segments enables convergence through the re-use of a common interconnect technology.

3.8.1. PCI Express Signal Descriptions

Table 24 - PCI Express Lane A Signal Description

Pin #	EDM	Signal	V	I/O	Description
85	1 / 2	PCIEA_CLK+	PCIE	O	PCI Express channel A clock differential pair signal
87	1 / 2	PCIEA_CLK-	PCIE	O	
91	1 / 2	PCIEA_TX+	PCIE	O	PCI Express channel A Transmit output differential pair signal
93	1 / 2	PCIEA_TX-	PCIE	O	
97	1 / 2	PCIEA_RX+	PCIE	I	PCI Express channel A Receive input differential pair signal
99	1 / 2	PCIEA_RX-	PCIE	I	
107	1 / 2	PCIE_PRST#	PCIE	I	PCI Express interface presence detection pin
113	1 / 2	PCIECLK_OEA	PCIE	O	PCI Express channel A hot plug detection signal
117	1 / 2	PCIE_WAKE#	CMOS 3.3V	I	PCI Express Wake Event: Sideband wake signal asserted by components requesting wake up
119	1 / 2	PCIE_RST#	CMOS 3.3V	O	PCI Express Reset signal for external devices

Table 25 - PCI Express Lane B Signal Description

Pin #	EDM	Signal	V	I/O	Description
79	1 / 2	PCIEB_CLK+	PCIE	O	PCI Express channel B clock differential pair signal
81	1 / 2	PCIEB_CLK-	PCIE	O	
103	1 / 2	PCIEB_TX+	PCIE	O	PCI Express channel B Transmit output differential pair signal
105	1 / 2	PCIEB_TX-	PCIE	O	
107	1 / 2	PCIE_PRST#	PCIE	I	PCI Express interface presence detection pin
109	1 / 2	PCIEB_RX+	PCIE	I	PCI Express channel B Receive input differential pair signal
111	1 / 2	PCIEB_RX-	PCIE	I	
115	1 / 2	PCIECLK_OEB	PCIE	O	PCI Express channel B hot plug detection signal
117	1 / 2	PCIE_WAKE#	CMOS 3.3V	I	PCI Express Wake Event: Sideband wake signal asserted by components requesting wake up
119	1 / 2	PCIE_RST#	CMOS 3.3V	O	PCI Express Reset signal for external devices

Table 26 - PCI Express Lane 0-3 Signal Description

Pin #	EDM	Signal	V	I/O	Description
78	2	PCIECLK_OE0	PCIE	O	PCI Express channel 0 hot plug detection signal
80	2	PCIE0_CLK+	PCIE	O	PCI Express channel 0 clock differential pair signal
82	2	PCIE0_CLK-	PCIE	O	
84	2	PCIE1_CLK+	PCIE	O	PCI Express channel 1 clock differential pair signal
86	2	PCIE1_CLK-	PCIE	O	
90	2	PCIE0_TX+	PCIE	O	PCI Express channel 0 Transmit output differential pair signal
92	2	PCIE0_TX-	PCIE	O	
96	2	PCIE0_RX+	PCIE	I	PCI Express channel 0 Receive input differential pair signal
98	2	PCIE0_RX-	PCIE	I	
102	2	PCIE1_TX+	PCIE	O	PCI Express channel 1 Transmit output differential pair signal
104	2	PCIE1_TX-	PCIE	O	
106	2	PCIECLK_OE1	PCIE	O	PCI Express channel 1 hot plug detection signal
108	2	PCIE1_RX+	PCIE	I	PCI Express channel 1 Receive input differential pair signal
110	2	PCIE1_RX-	PCIE	I	
112	2	PCIE_CPPE#	PCIE	O	PCI Express module detection and power control
114	2	PCIE2_TX+	PCIE	O	PCI Express channel 2 Transmit output differential pair signal
116	2	PCIE2_TX-	PCIE	O	
118	2	PCIECLK_OE2	PCIE	O	PCI Express channel 2 hot plug detection signal
120	2	PCIE2_RX+	PCIE	I	PCI Express channel 2 Receive input differential pair signal
122	2	PCIE2_RX-	PCIE	I	
134	2	PCIE2_CLK+	PCIE	O	PCI Express channel 2 clock differential pair signal
136	2	PCIE2_CLK-	PCIE	O	
138	2	PCIE3_TX+	PCIE	O	PCI Express channel 3 Transmit output differential pair signal
140	2	PCIE3_TX-	PCIE	O	
142	2	PCIECLK_OE3	PCIE	O	PCI Express channel 3 hot plug detection signal
144	2	PCIE3_RX+	PCIE	I	PCI Express channel 3 Receive input differential pair signal
146	2	PCIE3_RX-	PCIE	I	
150	2	PCIE3_CLK+	PCIE	O	PCI Express channel 3 clock differential pair signal
152	2	PCIE3_CLK-	PCIE	O	
107	1 / 2	PCIE_PRST#	PCIE	I	PCI Express interface presence detection pin
117	1 / 2	PCIE_WAKE#	CMOS 3.3V	I	PCI Express Wake Event: Sideband wake signal asserted by components requesting wake up
119	1 / 2	PCIE_RST#	CMOS 3.3V	O	PCI Express Reset signal for external devices

NOTE: PCI Express Lane 0-3 can be configured as a single PCIe x4 lane or as four separate PCIe x1 lanes and this is module and/or BIOS/software dependent and one should check the EDM module vendors' documentation.

3.8.2. PCI Express x1 and x4 Connector Pin-out

Table 27 – PCI Express Connector Pin-out

	Side B		Side A	
Pin #	**Name**	**Description**	**Name**	**Description**
1	+12V	12V Power	PRSNT#*	Hot-Plug presence detected
2	+12V	12V Power	+12V	12V Power
3	+12V	12V Power	+12V	12V Power
4	GND	Ground	GND	Ground
5	SMB_CLK*	SMBus Clock	JTAG2*	TCK - Boundary Scan Test Clock
6	SMB_DAT*	SMBus Data	JTAG3*	TDI - Boundary Scan Test Data Input
7	GND	Ground	JTAG4*	TDO - Boundary Scan Test Data Output
8	+3.3V	3.3V Power	JTAG5*	TMS – Boundary Scan Test Mode Select
9	JTAG1*	TRST# - Boundary Scan Test Reset	+3.3V	3.3V Power
10	+3.3V*	3.3V Power	+3.3V	3.3V Power
11	PCIE_WAKE#*	Link reactivation	PCIE_RST#*	Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	PCIE_CLK_REF+*	Reference Clock differential pair signal
14	PCIE0_TX+	PCI Express channel 0 Transmit output differential pair signal	PCIE_CLK_REF-*	
15	PCIE0_TX-		GND	Ground
16	GND	Ground	PCIE0_RX+	PCI Express channel 0 Receive output differential pair signal
17	PRSNT#*	Hot-Plug presence detected	PCIE0_RX-	
18	GND	Ground	GND	Ground
19	PCIE1_TX+	PCI Express channel 1 Transmit output differential pair signal	RSVD	Reserved
20	PCIE1_TX-		GND	Ground
21	GND	Ground	PCIE1_RX+	PCI Express channel 1 Receive output differential pair signal
22	GND	Ground	PCIE1_RX-	
23	PCIE2_TX+	PCI Express channel 2 Transmit output differential pair signal	GND	Ground
24	PCIE3_TX-		GND	Ground
25	GND	Ground	PCIE2_RX+	PCI Express channel 2 Receive output differential pair signal
26	GND	Ground	PCIE2_RX-	
27	PCIE3_TX+	PCI Express channel 3 Transmit output differential pair signal	GND	Ground
28	PCIE3_TX-		GND	Ground
29	GND	Ground	PCIE3_RX+	PCI Express channel 3 Receive output differential pair signal
30	GND	Ground	PCIE3_RX-	
31	PRSNT#*	Hot-Plug presence detected	GND	Ground
32	GND	Ground	RSVD	Reserved

Note : Signals marked (*) are not required by the PCI Express Architecture and a general recommendation is to not connect these pins.

3.8.3. PCI Express Mini Card Connector Pin-out

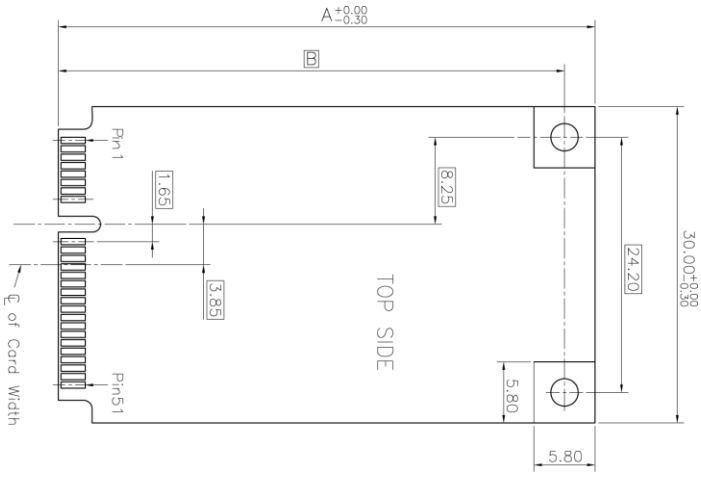
The PCI Express Mini Card is a small form factor add-in card optimized for mobile computing and embedded platforms. It is not hot-swappable.

PCI Express Mini Cards are popular for implementing features such as wireless LAN and communication modules. A small footprint connector can be implemented on the carrier board providing the ability to insert different removable PCI Express Mini Cards. Using this approach gives the flexibility to mount an upgradeable, standardized PCI Express Mini Card device to the carrier board without additional expenditure of a redesign.

A PCI Express Mini Card interface includes a single x1 PCIe link and a single USB 2.0 channel. The mini PCI Express Card host should offer both interfaces. The PCI Express Mini Card installed into the socket may use either interface.

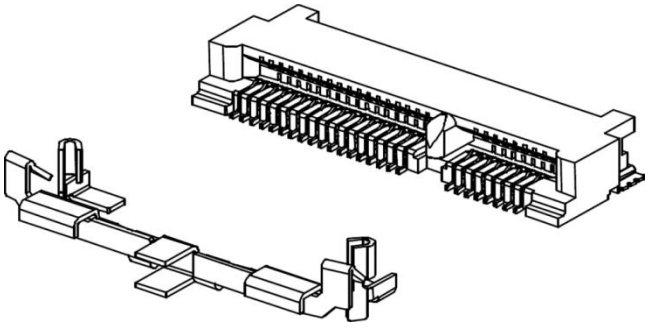
The source specification for mini-PCI Express Cards is the PCI Express Mini Card Electromechanical Specification.

Figure 22 - PCI Express Mni Card Footprint



	DIM A	DIM B
Half - Mini Card	26.80	23.90
Full - Mini Card	50.95	48.05

Figure 23 - PCI Express Mini Card Connector



A typical PCI Express Mini-Card socket is shown in Figure 23 above.

The most common pin-out used on a PCI Express Mini-Card socket is listed below and includes a single PCI Express lane, a USB port and the usage of and UIM (user Identity Module) interface.

Table 28 – PCI Express Mini Card Connector Pin-out

Pin #	Signal	Description	Pin #	Signal	Description
1	WAKE#	Request that host interface return to full operation	2	+3.3V	3.3V Power
3	RSVD	Reserved	4	GND	Ground
5	RSVD	Reserved	6	+1.5V	1.5V Power
7	CLKREQ#	Reference clock request signal	8	UIM_PWR	User Identity Module (UIM) Power
9	GND	Ground	10	UIM_DATA	User Identity Module (UIM) Data
11	REFCLK-	Reference Clock differential pair signal	12	UIM_CLK	User Identity Module (UIM) Clock
13	REFCLK+		14	UIM_RST	User Identity Module (UIM) Reset
15	GND	Ground	16	UIM_VPP	User Identity Module (UIM) variable Power
Mechanical Key					
17	RSVD	Reserved	18	GND	Ground
19	RSVD	Reserved	20	W_DISABLE#	Wireless Disable
21	GND	Ground	22	PERST#	PCI Express Reset
23	PCIEx_RX-	PCI Express Receive output differential pair signal	24	+3.3V	3.3V Power
25	PCIEx_RX+		26	GND	Ground
27	GND	Ground	28	+1.5V	1.5V Power
29	GND	Ground	30	SMB_CLK*	SMBus Clock
31	PCIEx_TX-	PCI Express Transmit output differential pair signal	32	SMB_DATA*	SMBus Data
33	PCIEx_TX+		34	GND	Ground
35	GND	Ground	36	USB_D-	Universal Serial Bus differential pair signal
37	GND	Ground	38	USB_D+	
39	+3.3V	3.3V Power	40	GND	Ground
41	+3.3V	3.3V Power	42	LED_WWAN#	LED status indicator signal
43	GND	Ground	44	LED_WLAN#	LED status indicator signal
45	RSVD	Reserved	46	LED_WPAN#	LED status indicator signal
47	RSVD	Reserved	48	+1.5V	1.5V Power
49	RSVD	Reserved	50	GND	Ground
51	RSVD	Reserved	52	+3.3V	3.3V Power

Note : Signals marked (*) are not required by the PCI Express Architecture and a general recommendation is to not connect these pins.

3.8.4. PCI Express Routing Considerations

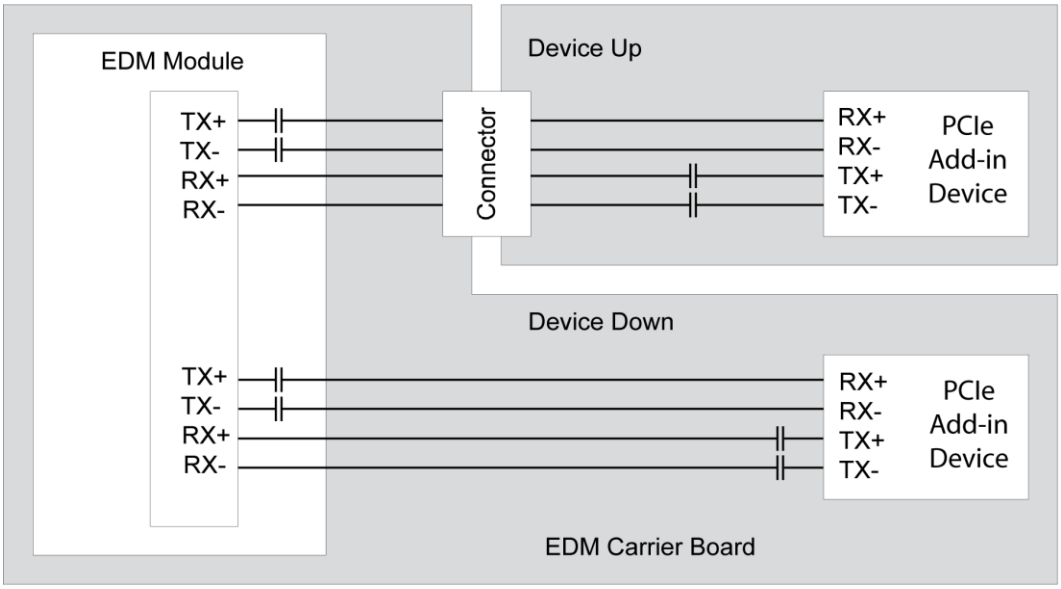
PCI Express (PCIe) signals are high-speed differential pairs with a nominal 100-Ω differential impedance. Route them as differential pairs, preferably referenced to a continuous GND plane with a minimum of via transitions.

PCIe pairs need to be length-matched within a given pair (“intra-pair”), but the different pairs do not need to be closely matched (“inter-pair”).

Coupling capacitors are not needed on carrier board PCI Express RX lines. They are present on the EDM module. Coupling capacitors however should be added on the carrier board PCI Express TX lines.

PCB design rules for these signals are summarized in ”4.5.4. PCI Express Signaling Details and Routing Guideline” on page 117.

Figure 24 - PCI Express Coupling Capacitors



3.8.5. Polarity Inversion

Per the PCI Express Card Electromechanical Specification, all PCIe devices must support polarity inversion on each PCIe lane, independently of the other lanes. This means that, for example, you can route the Module PCIE_TX0+ signal to the corresponding ‘-’ pin on the slot or target device, and the PCIE_TX0- signal to the corresponding ‘+’ pin. If this makes the layout cleaner, with fewer layer transitions and better differential pairs, then take advantage of this PCIe feature.

3.9. Serial ATA Interface

Serial ATA (SATA) is a serial interface for connecting storage devices (mainly hard disks) and was defined to replace the old parallel ATA interface. Serial ATA uses a point-to-point serial connection between the system and the storage device. The first generation of standard Serial ATA provides a maximum effective data transfer rate of 150MB/s per port. With the second generation SATA II, an effective transfer rate of up to 300MB/s per port is possible. With the third generation SATA III, an effective transfer rate of up to 600MB/s per port is possible.

3.9.1. Serial ATA Signal Description

Table 29 – SATA Port 1 Interface Signal Description

Pin #	EDM	Signal	V	I/O	Description
123	1 / 2	SATA1_RXP	SATA	I	Serial ATA channel 1 Receive differential pair signal
125	1 / 2	SATA1_RXN	SATA	I	
133	1 / 2	SATA1_nACT	SATA	I/O	Serial ATA LED. Open collector output pin driven during SATA command activity
135	1 / 2	SATA1_TXP	SATA	O	Serial ATA channel 1 Transmit differential pair signal
137	1 / 2	SATA1_TXN	SATA	O	

The EDM Module provides a LED signal SATA_ACT# that can be used to indicate SATA drive activity.

Table 30 - SATA Port 2 Interface Signal Description

Pin #	EDM	Signal	V	I/O	Description
156	2	SATA2_RXP	SATA	I	Serial ATA channel 2 Receive differential pair signal
158	2	SATA2_RXN	SATA	I	
160	2	SATA2_ODD	SATA	I/O	Serial ATA channel 2 ODD signal
162	2	SATA2_TXN	SATA	O	Serial ATA channel 2 Transmit differential pair signal
164	2	SATA2_TXP	SATA	O	

3.9.2. Serial ATA Connector Pin-out

SATA devices can be internal to the system or external. The eSATA specification defines the connector used for external SATA devices. The eSATA interface must be designed to prevent damage from ESD, comply with EMI limits, and withstand more insertion/removals cycles than standard SATA. A specific eSATA connector was designed to meet these needs. The eSATA connector does not have the “L” shaped key, and because of this, SATA and eSATA cables cannot be interchanged.

Figure 25 - Serial ATA Connector

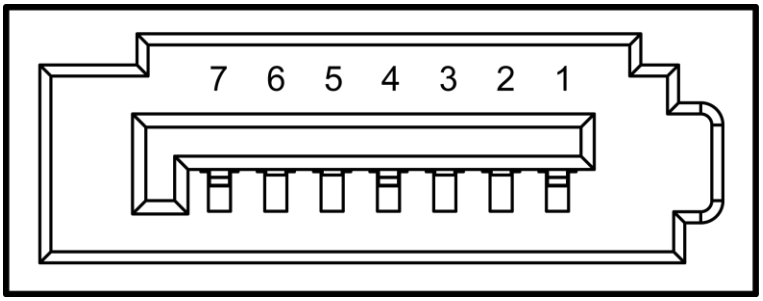


Figure 26 - Serial ATA with Power Connector

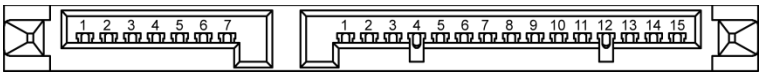


Table 31 - Serial ATA Connector Pin-out

Pin #	Signal	Description
1	GND	Ground
2	TX+	Transmitter differential pair signal
3	TX-	
4	GND	Ground
5	RX-	Receiver differential pair signal
6	RX+	
7	GND	Ground

Table 32 - Serial ATA Power Connector Pin-out

Pin #	Signal	Description
1,2,3	+3.3V	3.3V Power supply
4,5,6	GND	Ground
7,8,9	+5V	5V Power supply
10,11,12	GND	Ground
13,14,15	+12V	12V Power supply

3.9.3. Serial ATA PCB Routing Considerations

Route SATA signals as differential pairs, with a 100 Ω differential impedance and a 55 Ω, single- ended impedance. Ideally, a SATA pair is routed on a single layer adjacent to a ground plane. SATA pairs should not cross plane splits. Keep layer transitions to a minimum. Reference the SATA pairs to a power plane if necessary. The power plane should be quiet and well bypassed.

Coupling capacitors are not needed on carrier board SATA lines. They are present on the EDM module.

PCB design rules for these signals are summarized in “4.5.5. Serial ATA Signaling Details and Routing Guideline” on page 118 below.

3.10. Universal Serial Bus (USB) Interface

All the available USB ports on the EDM module should support at least a USB2.0 Host compliant interface including PHY. The EDM carrier board must current limit the USB power source to minimize disruption of the carrier board in the event that a short or over-current condition exists on one of the USB Ports.

Although USB signals use differential signaling, the USB specification also encodes single ended state information in the differential pair, making EMI filtering somewhat challenging. Ports that are internally on the carrier board connected to devices do not need EMI filters.

A USB Port can be powered from the carrier board main power or from the carrier board suspend power if supported by the power circuit and EDM module.

3.10.1. Universal Serial Bus Signal Description

Table 33 - USB Port 1 Signal Description

Pin #	EDM	Signal	V	I/O	Description
183	1 / 2	USB1_VBUS	5V	I/O	Universal Serial Bus port 1 power
181	1 / 2	USB1_D+	USB	I/O	Universal Serial Bus port 1 differential pair signal
179	1 / 2	USB1_D-	USB	I/O	
175	1 / 2	StdB1_SSTX-	USB	O	Universal Serial Bus Superspeed transmitter differential pair signal
173	1 / 2	StdB1_SSTX+	USB	O	
171	1 / 2	GND1_DRAIN	USB	P	Universal Serial Bus ground for signal return
169	1 / 2	StdB1_SSRX-	USB	I	Universal Serial Bus Superspeed receiver differential pair signal
167	1 / 2	StdB1_SSRX+	USB	I	
165	1 / 2	USB1_OC	CMOS 3.3V	I	Over current detect input pin to monitor USB power over current
139	1 / 2	USB1_HUB_RST	USB	O	Universal Serial Bus carrier board hub reset pin

Table 34 - USB Port 2 Signal Descriptions

Pin #	EDM	Signal	V	I/O	Description
161	1 / 2	USB2_VBUS	5V	I/O	Universal Serial Bus port 2 power
159	1 / 2	USB2_D-	USB	I/O	Universal Serial Bus port 2 differential pair signal
157	1 / 2	USB2_D+	USB	I/O	
155	1 / 2	USB2_OTG_ID	USB	I	Universal Serial Bus On-The-Go detection signal
151	1 / 2	StdB2_SSTX-	USB	O	Universal Serial Bus Superspeed transmitter differential pair signal
149	1 / 2	StdB2_SSTX+	USB	O	
147	1 / 2	GND2_DRAIN	USB	P	Universal Serial Bus ground for signal return
145	1 / 2	StdB2_SSRX-	USB	I	Universal Serial Bus Superspeed receiver differential pair signal
143	1 / 2	StdB2_SSRX+	USB	I	
141	1 / 2	USB2_OC	CMOS 3.3V	I	Over current detect input pin to monitor USB power over current
163	1 / 2	USB2_PWR_EN	USB	O	Universal Serial Bus power enable

3.10.2. USB Connector Pin Out

Figure 27 - USB Host Connector

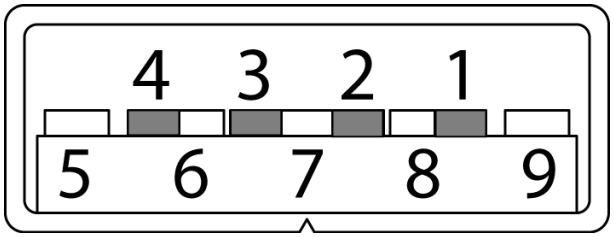


Table 35 - USB connector Pin-out

Pin #	Signal	Description
1	VBUS	5V Uviversal Serial Bus Power
2	USB_D-	Universal Serial Bus port 2 differential pair signal
3	USB_D+	
4	GND	Ground
5	StdA_SSRX-	Universal Serial Bus Superspeed receiver differential pair signal
6	StdA_SSRX+	
7	GND	Ground
8	StdA_SSTX-	Universal Serial Bus Superspeed transmitter differential pair signal
9	StdA_SSTX+	

Figure 28 - USB OTG Connector

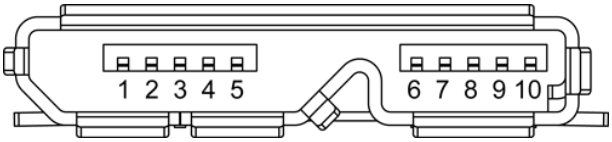


Table 36 - USB OTG connector Pin-out

Pin #	Signal	Description
1	VBUS	Ground
2	USB_D-	Universal Serial Bus port 2 differential pair signal
3	USB_D+	
4	USB_OTG_ID	Universal Serial Bus On-The-Go detection signal
5	GND	Ground
6	StdA_SSTX-	Universal Serial Bus Superspeed transmitter differential pair signal
7	StdA_SSTX+	
8	GND	Ground
9	StdA_SSRX-	Universal Serial Bus Superspeed receiver differential pair signal
10	StdA_SSRX+	

3.10.3. USB Over-Current Protection (USBx_OC#)

The USB Specification describes power distribution over the USB port, which supplies power for USB devices that are directly connected to the carrier board. Therefore, the host must implement over-current protection on the ports for safety reasons. Should the aggregate current drawn by the downstream ports exceed a permitted value, the over-current protection circuit removes power from all affected downstream ports. The over-current limiting mechanism must be resettable without user mechanical intervention. For more detailed information about this subject, refer to the 'Universal Serial Bus Specifications Revision 2.0', which can be found on the website http://www.usb.org.

Over-current protection for USB ports can be implemented by using power distribution switches on the carrier board that monitors the USB port power lines. Power distribution switches usually have a soft-start circuitry that minimizes inrush current in applications where highly capacitive loads are employed. Transient faults are internally filtered.

Additionally, they offer a fault status output that is asserted during over-current and thermal shutdown conditions. These outputs should be connected to the corresponding EDM modules USB over-current sense signals. Fault status signaling is an option at the USB specification. If you don't need the popup message in your OS you may leave the signals unconnected.

Simple resettable PolySwitch devices are capable of fulfilling the requirements of USB over- current protection and therefore can be used as a replacement for power distribution switches.

3.10.4. Powering USB Devices during S5 (x86 based EDM Modules)

The power distribution switches and the ESD protection can be powered from Main Power or Suspend Power (5VSB).

Suspend Power (5VSB) is used for devices that need to be powered when the EDM module is in Sleep-State S5. This would typically be for USB devices that support Wake-on-USB. The amount of current available on 5VSB is limited so it should be used sparingly.

3.10.5. USB PCB Routing Considerations

Route USB signals as differential pairs, with a 90-Ω differential impedance and a 45-Ω, single- ended impedance. Ideally, a USB pair is routed on a single layer adjacent to a ground plane.

USB pairs should not cross plane splits. Keep layer transitions to a minimum. Reference USB pairs to a power plane if necessary. The power plane should be well-bypassed.

USB routing rules are summarized in “4.5.6. Universal Serial Bus (USB) Signaling Details and Routing Guideline” on page 119 below.

3.10.6. EMI / ESD Protection

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins. Common mode chokes can provide required noise attenuation but they also distort the signal quality of full-speed and high-speed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the carrier board design.

To protect the USB host interface of the module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes can be optionally implemented on the carrier board design,

3.11. SDIO/MMC Interface

SDIO (Secure Digital I/O) provides an easy to implement solution for high-speed data I/O combined with low power consumption. SDIO cards are fully compatible with SD memory cards. This includes mechanical, electrical, power, signaling and software compatibility. SDIO hosts are able to drive SD cards and MMC (MultiMediaCards) as well as SDIO cards that provide functions such as Ethernet or WLAN, GPS receivers, Bluetooth, modems etc.

3.11.1. SDIO/MMC Interface Signal Description

Table 37 - SDIO/MMC Interface Signal Description

Pin #	EDM	Signal	V	I/O	Description
212	1 / 2	SDIO_DAT0	CMOS 3.3V	I/O	MMC/SDIO Data bit 0
209	1 / 2	SDIO_DAT1	CMOS 3.3V	I/O	MMC/SDIO Data bit 1
214	1 / 2	SDIO_DAT2	CMOS 3.3V	I/O	MMC/SDIO Data bit 2
211	1 / 2	SDIO_DAT3	CMOS 3.3V	I/O	MMC/SDIO Data bit 3
216	1 / 2	SDIO_DAT4	CMOS 3.3V	I/O	MMC/SDIO Data bit 4
213	1 / 2	SDIO_DAT5	CMOS 3.3V	I/O	MMC/SDIO Data bit 5
218	1 / 2	SDIO_DAT6	CMOS 3.3V	I/O	MMC/SDIO Data bit 6
215	1 / 2	SDIO_DAT7	CMOS 3.3V	I/O	MMC/SDIO Data bit 7
203	1 / 2	SDIO_CD	CMOS 3.3V	I/O	MMC/SDIO Card Detect
205	1 / 2	SDIO_CMD	CMOS 3.3V	I/O	MMC/SDIO Command
206	1 / 2	SDIO_CLK	CMOS 3.3V	O	MMC/SDIO Clock
207	1 / 2	SDIO_WP	CMOS 3.3V	I/O	MMC/SDIO Write Protect
208	1 / 2	SDIO_LED	CMOS 3.3V	O	MMC/SDIO LED
210	1 / 2	SDIO_PWR	CMOS 3.3V	O	MMC/SDIO Power Enable

3.11.2. SDIO/MMC PCB Routing Considerations

SDIO signals are low speed signals. Route the SDIO bus as 55 Ω, single-ended signals. The bus may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

3.11.3. EMI / ESD Protection

To improve the EMI behavior of the SDIO interface, a design should include common mode chokes, which have to be placed as close as possible to the SD card connector signal pins. Common mode chokes can provide required noise attenuation but they also distort the signal quality. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the SDIO signals on the Carrier Board design.

To protect the SDIO interface of the Module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes have to be implemented on the Carrier Board design.

3.12. Low Pin Count Interface (LPC)

The Low Pin Count Interface is a common interface in x86 based systems and was defined by Intel® Corporation to facilitate the industry's transition toward legacy free systems. It allows the integration of low-bandwidth legacy I/O components within the system, which are typically provided by a Super I/O controller. Furthermore, it can be used to interface Firmware Hubs, Trusted Platform Module (TPM) devices, general-purpose inputs and outputs, and Embedded Controller solutions. Data transfer on the LPC bus is implemented over a 4 bit serialized data interface, which uses a 33MHz LPC bus clock. It is straightforward to develop PLDs or FPGAs that interface to the LPC bus.

3.12.1. LPC Signal Description

Table 38 - LPC Signal Description

Pin #	EDM	Signal	V	I/O	Description
168	2	LPC_AD0	CMOS 3.3V	I/O	Low Pin Count Interface multiplex Address and Data line 0
170	2	LPC_AD1	CMOS 3.3V	I/O	Low Pin Count Interface multiplex Address and Data line 1
172	2	LPC_AD2	CMOS 3.3V	I/O	Low Pin Count Interface multiplex Address and Data line 2
174	2	LPC_AD3	CMOS 3.3V	I/O	Low Pin Count Interface multiplex Address and Data line 3
176	2	LPC_CLK	CMOS 3.3V	O	Low Pin Count Interface clock
178	2	LPC_nFRAME	CMOS 3.3V	O	Low Pin Count Interface frame
180	2	LPC_nLDDRQ	CMOS 3.3V	I	Low Pin Count Interface DMA request
182	2	LPC_nSERIRQ	CMOS 3.3V	I/O	Low Pin Count Interface serialized interrupt

3.12.2. Super I/O

Within the EDM modular architecture, super I/O controllers could be placed on carrier boards according to unique application requirements. However, LPC super I/O devices are closely coupled to the BIOS firmware that initializes them and performs setup-based interrupt assignments. The BIOS flash generally resides on the EDM modules in order for the modules to be self-booting. This tight coupling of LPC super I/O to the BIOS presents a multitude of problems in a legacy-free modular environment.

Normally the BIOS vendor supplies to the BIOS developer the choice of different super I/O modules that can be plugged-in at the source level during the BIOS build process. The BIOS super I/O code modules often require considerable adaptation work by the BIOS developer to be able to be “plugged-in”. The supported super I/O device would be determined by the EDM module vendor, and other device support would involve customization of the BIOS for each super I/O device.

3.12.3. LPC Data signal PCB Routing Considerations

LPC signals are low speed signals. Route the LPC bus as 55 Ω, single-ended signals. The bus may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

3.12.4. LPC Clock signal PCB Routing Considerations

Route the LPC clock as a single-ended, 55 Ω trace with generous clearance to other traces and to itself. A continuous ground-plane reference is recommended. Routing the clock on a single ground referenced internal layer is preferred to reduce EMI.

The EDM Specification allows 1.6 ns +/- 0.1ns for the propagation delay of the LPC clock from the EDM Module pin to the LPC device destination pin. Using a typical propagation delay value of 180 ps / inch, this works out to 8.88 inches of Carrier Board trace for a device-down application. For device-up situations, 2.5 inches of clock trace are assumed to be on the LPC slot card. This is deducted from the 8.88 inches, yielding 6.38 inches.

On a Carrier Board with a small form factor, serpentine clock traces may be required to meet the clock-length requirement.

The EDM Specification brings a single LPC clock out of the Module. If there are multiple LPC targets on the Carrier Board design, then a zero delay clock buffer is recommended. This provides a separate copy of the LPC clock to each target. The overall delay from the Module LPC clock pin to the target LPC device clock pin should be 1.6 ns.

3.12.5. Design Recommendation

The EDM consortium recommends using USB peripherals or PCI Express super I/O devices on carrier boards for customers wishing to use additional UART serial ports or other legacy peripherals. Plug-and-play based interrupt assignments are automatic, and drivers initialize devices after the operating system is loaded. A USB keyboard can be used to enter BIOS setup prior to power-on self-test.

The EDM consortium recommends against using LPC super I/O devices on the carrier board as such usage creates BIOS customization requirements and can greatly restrict Module interoperability. PCI Express, and/or USB devices should be used instead.

The EDM consortium suggests that alternate BIOS firmware support on the carrier board as well as port 0x80 implementations are appropriate uses of the LPC interface on the carrier board.

3.13. General Purpose Memory Controller Bus (Local Bus)

Local bus is a common interface in ARM based systems that connect directly, or almost directly, from the CPU to one or more slots on the expansion bus. The significance of direct connection to the CPU is avoiding the bottleneck created by the expansion bus, thus providing fast throughput. There are several local buses built into various types of computers to increase the speed of data transfer. Local buses for expanded memory and video boards are the most common.

The General Purpose Memory Controller (GPMC) can be used to connect to external memory devices such as NOR Flash, NAND Flash, Pseudo SRAM, SRAM or Field programmable Gate Array (FPGA)

3.13.1. GPMC Signal Description

Table 39 - GPMC Signal Description

Pin #	EDM	Signal	V	I/O	Description
182	1	GPMC_D0	CMOS 3.3V	I/O	GPMC data bit 0
180	1	GPMC_D1	CMOS 3.3V	I/O	GPMC data bit 1
178	1	GPMC_D2	CMOS 3.3V	I/O	GPMC data bit 2
176	1	GPMC_D3	CMOS 3.3V	I/O	GPMC data bit 3
174	1	GPMC_D4	CMOS 3.3V	I/O	GPMC data bit 4
172	1	GPMC_D5	CMOS 3.3V	I/O	GPMC data bit 5
170	1	GPMC_D6	CMOS 3.3V	I/O	GPMC data bit 6
168	1	GPMC_D7	CMOS 3.3V	I/O	GPMC data bit 7
164	1	GPMC_D8	CMOS 3.3V	I/O	GPMC data bit 8
162	1	GPMC_D9	CMOS 3.3V	I/O	GPMC data bit 9
160	1	GPMC_D10	CMOS 3.3V	I/O	GPMC data bit 10
158	1	GPMC_D11	CMOS 3.3V	I/O	GPMC data bit 11
156	1	GPMC_D12	CMOS 3.3V	I/O	GPMC data bit 12
152	1	GPMC_D13	CMOS 3.3V	I/O	GPMC data bit 13
150	1	GPMC_D14	CMOS 3.3V	I/O	GPMC data bit 14
146	1	GPMC_D15	CMOS 3.3V	I/O	GPMC data bit 15
144	1	GPMC_A1	CMOS 3.3V	O	GPMC output address bit 1
142	1	GPMC_A2	CMOS 3.3V	O	GPMC output address bit 2

140	1	GPMC_A3	CMOS 3.3V	O	GPMC output address bit 3
138	1	GPMC_A4	CMOS 3.3V	O	GPMC output address bit 4
136	1	GPMC_A5	CMOS 3.3V	O	GPMC output address bit 5
134	1	GPMC_A6	CMOS 3.3V	O	GPMC output address bit 6
122	1	GPMC_A7	CMOS 3.3V	O	GPMC output address bit 7
120	1	GPMC_A8	CMOS 3.3V	O	GPMC output address bit 8
118	1	GPMC_A9	CMOS 3.3V	O	GPMC output address bit 9
116	1	GPMC_A10	CMOS 3.3V	O	GPMC output address bit 10
112	1	GPMC_RE	CMOS 3.3V	O	GPMC Read Enable
110	1	GPMC_WE	CMOS 3.3V	I	GPMC Write Enable
108	1	GPMC_ALE	CMOS 3.3V	O	GPMC Address Valid or Address Latch Enable
106	1	GPMC_CLE	CMOS 3.3V	O	GPMC Lower Byte Enable. Also used for Command Latch Enable
104	1	GPMC_WP	CMOS 3.3V	O	GPMC Write Protect / Enable
102	1	GPMC_WAIT	CMOS 3.3V	I	GPMC External indication of wait
98	1	GPMC_nCSE	CMOS 3.3V	O	GPMC Chip Select bit E
96	1	GPMC_nCSD	CMOS 3.3V	O	GPMC Chip Select bit D
92	1	GPMC_nCSC	CMOS 3.3V	O	GPMC Chip Select bit C
90	1	GPMC_nCSB	CMOS 3.3V	O	GPMC Chip Select bit B
86	1	GPMC_nCSA	CMOS 3.3V	O	GPMC Chip Select bit A

3.13.2. GPMC PCB Routing Considerations

GPMC signals are low speed signals. Route the LPC bus as 55 Ω, single-ended signals. The bus may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

3.13.3. Design Recommendation

The EDM consortium recommends using USB peripherals or PCI Express super I/O devices on carrier boards for customers wishing to use additional UART serial ports or other legacy peripherals. Plug-and-play based interrupt assignments are automatic, and drivers initialize devices after the operating system is loaded.

The EDM consortium recommends against using GPMC based devices on the carrier board as such usage creates software customization requirements and can greatly restrict EDM module interoperability. PCI Express, and/or USB devices should be used instead.

3.14. CAN BUS Interface signals

Controller Area Network (CAN or CAN-bus) is a message based protocol designed specifically for automotive applications but is also often being used in other areas such as industrial automation and medical equipment.

CAN is a multi-master broadcast serial bus standard for connecting electronic control units (ECUs).

Each node is able to send and receive messages, but not simultaneously. A message consists primarily of an ID (identifier), which represents the priority of the message, and up to eight data bytes. It is transmitted serially onto the bus. This signal pattern is encoded in non-return-to-zero (NRZ) and is sensed by all nodes.

The devices that are connected by a CAN network are typically sensors, actuators, and other control devices. These devices are not connected directly to the bus, but through a host processor and a CAN controller.

If the bus is free, any node may begin to transmit. If two or more nodes begin sending messages at the same time, the message with the more dominant ID (which has more dominant bits, i.e., zeroes) will overwrite other nodes' less dominant IDs, so that eventually (after this arbitration on the ID.) only the dominant message remains and is received by all nodes. This mechanism is referred to as priority based bus arbitration. Messages with numerically smaller values of IDs have higher priority and are transmitted first.

3.14.1. CAN BUS Signal Description

Table 40 - Primary CAN BUS Signal Description

Pin #	EDM	Signal	V	I/O	Description
202	1 / 2	CAN1-	CAN	I/O	Primary CAN (controller Area Network) differential pair signal
200	1 / 2	CAN1+	CAN	I/O	

Table 41 - Secondary CAN BUS Signal Description

Pin #	EDM	Signal	V	I/O	Description
199	1 / 2	CAN2-	CAN	I/O	Secondary CAN (controller Area Network) differential pair signal
197	1 / 2	CAN2+	CAN	I/O	

3.14.2. CAN Bus Security

CAN Bus is a low-level protocol, and does not support any security features intrinsically. Applications are expected to deploy their own security mechanisms; e.g., to authenticate each other. Failure to do so may result in various sorts of attacks, if the opponent manages to insert messages on the bus. Password mechanisms exist for data transfer that can modify the control unit software, like software download or ignition key codes, but usually not for standard communication.

3.14.3. CAN Bus PCB Routing Considerations

CAN Bus signals are low speed signals. Route the CAN Bus signals as 55 Ω, single-ended signals. The data signals may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

3.14.4. CAN Bus Isolation

For applications where CAN Bus isolation is required, a SHARP PC400 Compact, Surface Mount Type OPIC Photo coupler can be implemented on the EDM Carrier Board.

3.15. Universal Asynchronous Receiver/Transmitter (UART) Interface

A universal asynchronous receiver/transmitter (UART) is a type of "asynchronous receiver/transmitter", a piece of computer hardware that translates data between parallel and serial forms. UARTs are commonly used in conjunction with communication standards such as EIA RS-232, RS-422 or RS-485

3.15.1. UART Signal Description

Table 42 - Primary UART Signal Description

Pin #	EDM	Signal	V	I/O	Description
241	1 / 2	UART1_CTS	UART	O	Universal Asynchronous Receive Transmit secondary channel clear to send signal
243	1 / 2	UART1_TXD	UART	O	Universal Asynchronous Receive Transmit secondary channel transmit data signal
245	1 / 2	UART1_RXD	UART	I	Universal Asynchronous Receive Transmit secondary channel receive data signal
247	1 / 2	UART1_RTS	UART	O	Universal Asynchronous Receive Transmit secondary channel request to send signal

NOTE: it is recommended to use the UART1 interface as system debug where possible and use the UART2 signals in applications where one serial port is required.

Table 43 - Secondary UART Signal Description

Pin #	EDM	Signal	V	I/O	Description
234	1 / 2	UART2_CTS	UART	O	Universal Asynchronous Receive Transmit secondary channel clear to send signal
236	1 / 2	UART2_TXD	UART	O	Universal Asynchronous Receive Transmit secondary channel transmit data signal
238	1 / 2	UART2_RXD	UART	I	Universal Asynchronous Receive Transmit secondary channel receive data signal
240	1 / 2	UART2_RTS	UART	O	Universal Asynchronous Receive Transmit secondary channel request to send signal
242	1 / 2	UART2_DCD	UART	I	Universal Asynchronous Receive Transmit secondary channel carrier detect signal
244	1 / 2	UART2_DSR	UART	I	Universal Asynchronous Receive Transmit secondary channel data set ready signal
246	1 / 2	UART2_DTR	UART	O	Universal Asynchronous Receive Transmit secondary channel data terminal ready signal
248	1 / 2	UART2_RI	UART	I	Universal Asynchronous Receive Transmit secondary channel ring indication signal

3.15.2. Serial Port Connector Pin-out

Serial port connectors are widely spread and often use a DE-9 type connector. It is recommended to follow the following pin-out in order to easily obtain standard serial communication or NULL-Modem cables.

Figure 29 - DE-9 Serial Port Connector

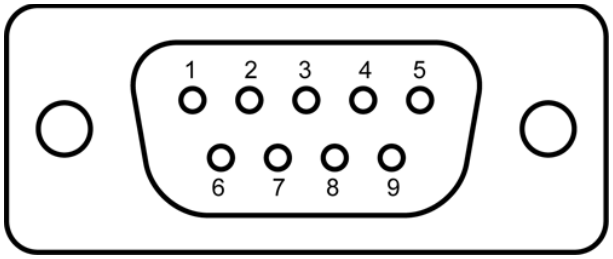


Table 44 - Serial Port Connector Pin-out

Pin #	RS-232	RS-422	RS-485
1	Carrier Detect	TxD- (A)	Data- (A)
2	Receive Data	TxD+ (B)	Data+ (B)
3	Transmit Data	RXD+ (B)	
4	Data Terminal Ready	RxD- (A)	
5	GND	GND	GND
6	Data Set Ready		
7	Request to Send		
8	Clear to Send		
9	Ring Indicator		

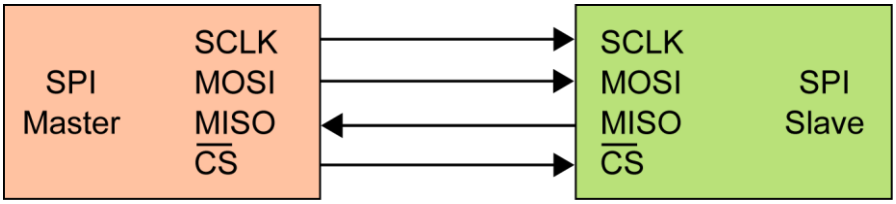
3.15.3. UART PCB Routing Considerations

UART signals are low speed signals. Route the UART signals as 55 Ω, single-ended signals. The data signals may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

3.16. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface Bus or SPI bus is a synchronous serial data link standard, named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines. Sometimes SPI is called a four-wire serial bus, contrasting with three-, two-, and one-wire serial buses. SPI is often referred to as SSI (Synchronous Serial Interface).

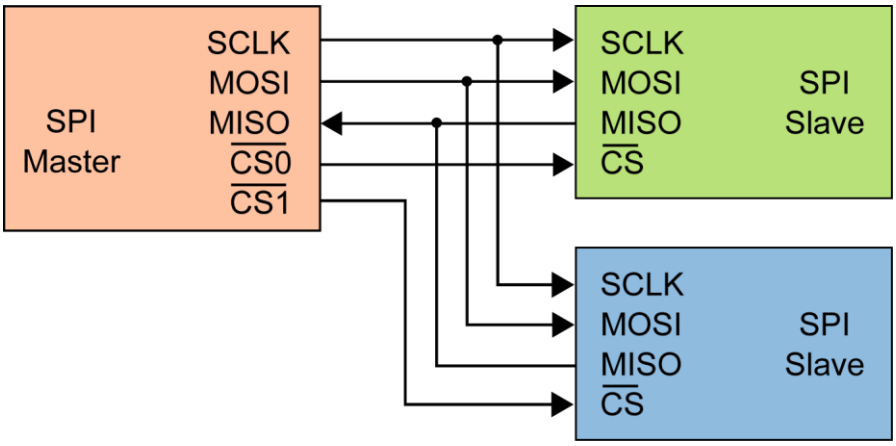
Figure 30 - SPI bus: single master and single slave



3.16.1. Independent slave SPI configuration

Typical SPI bus: master and three independent slaves in the independent slave configuration, there is an independent chip select line for each slave. This is the way SPI is normally used. Since the MISO pins of the slaves are connected together, they are required to be tri-state pins.

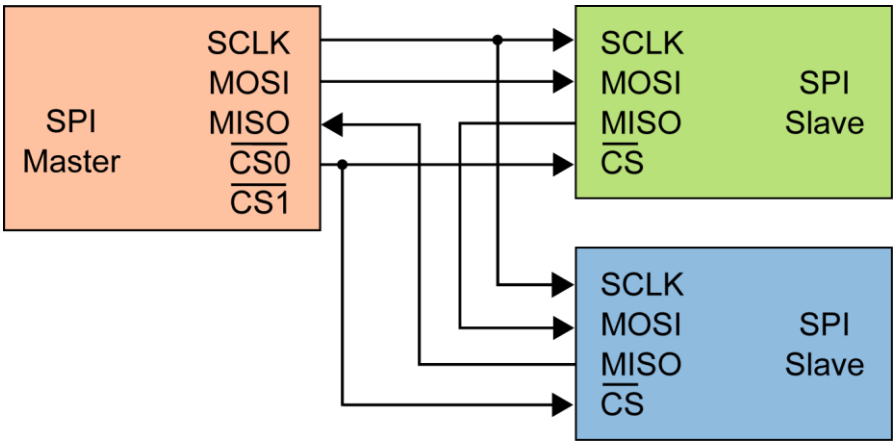
Figure 31 - SPI bus: master and two independent slaves



3.16.2. Daisy chain SPI configuration

Daisy-chained SPI bus: master and cooperative slaves. Products with SPI bus are designed to be capable of being connected in a daisy chain configuration, the first slave output being connected to the second slave input, etc. The SPI port of each slave is designed to send out during the second group of clock pulses an exact copy of what it received during the first group of clock pulses. The whole chain acts as an SPI communication shift register; daisy chaining is often done with shift registers to provide a bank of inputs or outputs through SPI. Such a feature only requires a single CS line from the master, rather than a separate CS line for each slave.

Figure 32 - Daisy-chained SPI bus: master and cooperative slaves



3.16.3. SPI Signal Description

Table 45 - Primary SPI Signal Description

Pin #	EDM	Signal	V	I/O	Description
222	1 / 2	SPI1_MOSI	CMOS 3.3V	O	Serial Peripheral Interface secondary channel master output slave input signal
224	1 / 2	SPI1_MISO	CMOS 3.3V	I	Serial Peripheral Interface secondary channel master input slave output signal
226	1 / 2	SPI1_CLK	CMOS 3.3V	O	Serial Peripheral Interface secondary channel clock signal
228	1 / 2	SPI1_CS0	CMOS 3.3V	O	Serial Peripheral Interface secondary channel Chip Select 0 signal
230	1 / 2	SPI1_CS1	CMOS 3.3V	O	Serial Peripheral Interface secondary channel Chip Select 1 signal. Do not use if only 1 SPI device is used

Table 46 - Secondary SPI Signal Description

Pin #	EDM	Signal	V	I/O	Description
219	1 / 2	SPI2_MOSI	CMOS 3.3V	O	Serial Peripheral Interface primary channel master output slave input signal
221	1 / 2	SPI2_MISO	CMOS 3.3V	I	Serial Peripheral Interface primary channel master input slave output signal
223	1 / 2	SPI2_CLK	CMOS 3.3V	O	Serial Peripheral Interface primary channel clock signal
225	1 / 2	SPI2_CS0	CMOS 3.3V	O	Serial Peripheral Interface primary channel Chip Select 0 signal
227	1 / 2	SPI2_CS1	CMOS 3.3V	O	Serial Peripheral Interface primary channel Chip Select 1 signal. Do not use if only 1 SPI device is used

3.16.4. SPI signal PCB Routing Considerations

SPI signals are low speed signals. Route the SPI bus as 55 Ω, single-ended signals. The SPI bus may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

Do not connect Standby Power to SPI devices unless bus isolation is used to prevent back feeding of voltage from the Suspend supply to the Non-Suspend supply voltages.

3.17. SMBus / I²C Bus System Management Interface

The SMBus is a monitoring system bus primarily used as an interface to manage peripherals such as serial presence detect (SPD), thermal sensors, PCI Express devices, smart battery, display detection, etc.

The devices that can connect to the SMBus can be located on the EDM module and carrier board. Designers need to take note of several implementation issues to ensure reliable SMBus interface operation. The SMBus is similar to I²C.

I²C devices have the potential to lock up the data line while sending information and require a power cycle to clear the fault condition. SMBus devices contain a timeout to monitor for and correct this condition.

EDM modules are required to power SMBus devices from Early Power in order to have control during system states S0-S5. The devices on the carrier board using the SMBus are normally powered by the 3.3V main power. To avoid current leakage between the main power of the carrier board and the Suspend power of the module, the SMBus on the carrier board must be separated by a bus switch from the SMBus of the module. However, if the carrier board also uses Suspend powered SMBus devices that are designed to operate during system states S3-S5, then these devices must be connected to the Suspend powered side of the SMBus, i.e. between the EDM module and the bus switch.

Since the SMBus is used by the EDM module and carrier board, care must be taken to ensure that carrier board based devices do not overlap the address space of EDM module based devices.

Contact your EDM Module vendor for information on the SMBus addresses used.

3.17.1. SMBus Signal Description

Table 47 - SMBus 3.3V Pins

Pin #	EDM	Signal	V	I/O	Description
37	1 / 2	I2C_SDA	CMOS 3.3V	I/O	Display ID DDC data line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I²C bus data line
39	1 / 2	I2C_SCL	CMOS 3.3V	I/O	Display ID DDC data line used for LVDS flat panel detection. If not used this can be assigned to General Purpose I²C bus clock line

NOTE : The above signals are normally connected towards the internal display interface and smart battery. On exception basis these signals can be used to connect to other system management devices.

Table 48 - SMBus 5.0V Pins

Pin #	EDM	Signal	V	I/O	Description
73	1 / 2	I2C_SCL	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus clock line
75	1 / 2	I2C_SDA	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus data line
74	2	I2C_SCL	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus clock line
76	2	I2C_SDA	CMOS 5V	I/O	Display ID DDC data line used for HDMI detection. If not used this can be assigned to General Purpose I^2C bus data line

NOTE : The 5.0V I^2C signals are normally connected towards the external HDMI display interface and should not be connected to other parts of the system on a EDM carrier board.

3.17.2. SMBus Routing Considerations

SMBus/I^2C signals are low speed signals. Route the SMBus as 55 Ω, single-ended signals. The SMBus may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

SMBus should be connected to all or none of the PCI Express devices and slots. A general recommendation is to not connect these devices to the SMBus.

The maximum load of SMBus lines is limited to 3 external devices. Please contact your EDM module vendor if more devices are required.

Do not connect Non-Suspend powered devices to the SMBus unless a bus switch is used to prevent back feeding of voltage from the Suspend rail to other supplies.

Contact your EDM module vendor for a list of SMBus addresses used on the EDM module. Do not use the same address for carrier board devices.

3.18. General Purpose I²C Bus

The I²C (Inter-Integrated Circuit) bus is a two-wire serial bus originally defined by Philips. The bus is used for low-speed (up to 400kbps) communication between system ICs. The bus is often used to access small serial EEPROM memories and to set up IC registers. The EDM Specification defines two general I²C interfaces that are brought to the EDM module connector for use on the carrier board.

The lack of a common software interface for the General Purpose I²C interface might limit vendor interoperability. The EDM module vendors' documentation should be consulted for limitations and available I²C addresses.

3.18.1. General Purpose I²C Bus Implementation

I²C Bus uses only two bidirectional open-drain lines, Serial Data Line (SDA) and Serial Clock (SCL), pulled up with resistors.

The EDM specifications describe two I²C Bus at 3.3V for general purpose usage to connect to sensors, EEPROM, external RTC, touchpanel controllers, etc.

Devices operating on other voltages as the supplied 3.3V are permitted. However implementation of voltage level shifts on the carrier board is required.

Figure 33 - I2C Bus Voltage Level shift with Pull up Resistors

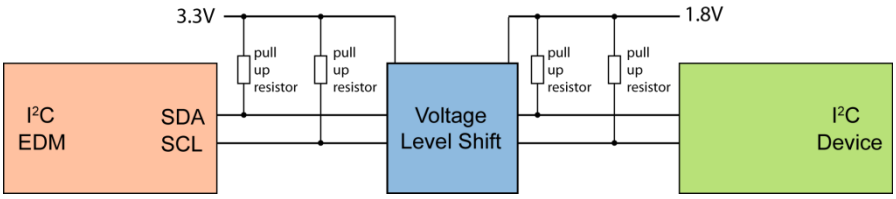
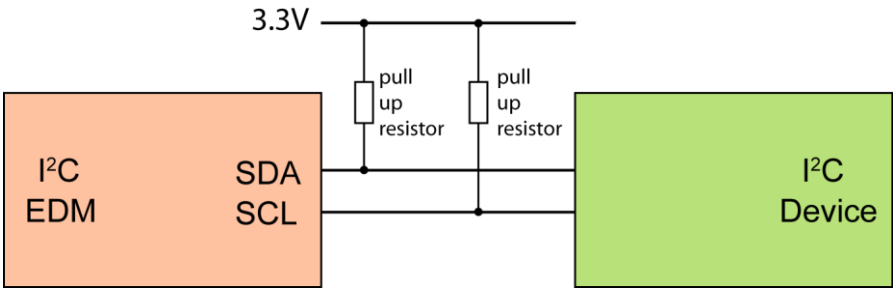


Figure 34 - I2C Bus operating at 3.3V with Pull up Resistors



3.18.2. General Purpose I²C Bus Signal Description

Table 49 - Primary General Purpose I²C Bus Signal Description

Pin #	EDM	Signal	V	I/O	Description
231	1 / 2	I2C2_SCL	CMOS 3.3V	I/O	I²C bus clock line
233	1 / 2	I2C2_SDA	CMOS 3.3V	I/O	I²C bus data line

Table 50 - Secondary General Purpose I²C Bus Signal Description

Pin #	EDM	Signal	V	I/O	Description
235	1 / 2	I2C3_SCL	CMOS 3.3V	I/O	I²C bus clock line
237	1 / 2	I2C3_SDA	CMOS 3.3V	I/O	I²C bus data line

NOTE : It's allowed that the same I²C Bus channel signal is available on different pins. Consult your EDM module vendors' documentation to ensure the I²C Bus signals are independent or duplicated.

3.18.3. General Purpose I²C Bus Routing Considerations

I²C signals are low speed signals. Route the I²C bus as 55 Ω, single-ended signals. The I²C bus may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

The maximum amount of capacitance allowed on the carrier board General Purpose I²C bus lines (I2C_SDA, I2C_SCL) is specified by your EDM module vendor. The carrier board designer is responsible for ensuring that the maximum amount of capacitance is not exceeded and the rise/fall times of the signals meet the I²C bus specification. As a general guideline, an IC input has 12pF of capacitance, and a PWB trace has 3.8pF per inch of trace length.

Do not connect Standby Power to I²C devices unless bus isolation is used to prevent back feeding of voltage from the Suspend supply to the Non-Suspend supply voltages.

3.19. General Purpose Input/Out (GPIO)

Table 51 - GPIO Signals

Pin #	EDM	Signal	V	I/O	Description
255	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
256	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
257	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
258	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
259	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
260	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
261	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
262	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
263	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output
264	1 / 2	GPIO	CMOS 3.3V	I/O	General Purpose Input Output

It is suggested to use the GPIO's connected to pin 263 and 264 for touch controller related functions.

3.19.1. General Purpose Input/Output PCB Routing Considerations

GPIO signals are low speed signals. Route the GPIO signals as 55 Ω, single-ended signals.

3.20. Input Power Requirements

EDM modules are designed to be driven with a single +5V input power rail. Additionally, two optional power rails are specified by EDM to provide a +5V standby voltage on the EDM module as well as a +3V Real Time Clock (RTC) supply voltage, which is provided by a battery cell located on the carrier board or from a dedicated 3V power source.

If the carrier board does not require standby functionality, then the +5V standby power rail can be omitted. The same applies to the +3V RTC battery voltage. If no RTC/CMOS backup functionality is required by the system, then the +3V RTC supply battery voltage can be omitted.

Table 52 - Input Power Signals

Power Rail	Nominal Input	Input Range	Maximum Input Ripple
VCC	5V	+4.75V - +5.25V	±50 mV
5VSB	5VSB	+4.75V - +5.25V	±50 mV
VCC_RTC	3V	+2.5V - +3.3V	±20 mV

3.20.1. Input Power Sequencing for AT based configurations

EDM input power sequencing requirements for AT based configurations are as follows:

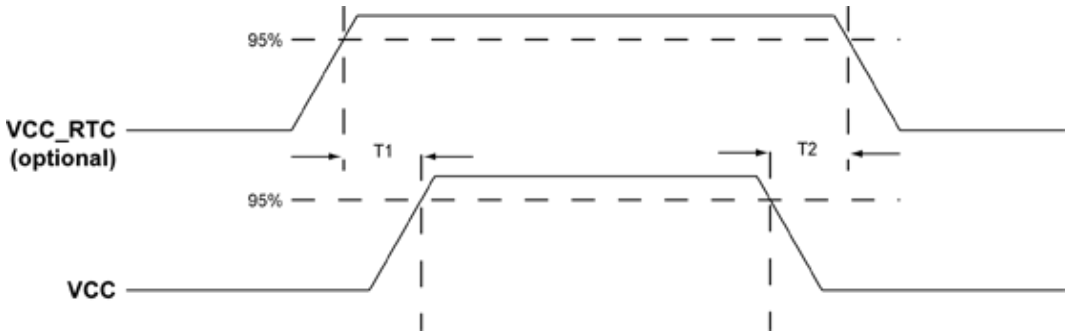
Start Sequence:
VCC_RTC must come up at the same time or before VCC comes up.

Stop Sequence:
VCC must go down at the same time or before VCC_RTC goes down

Table 53 - Input Power Sequencing for AT based configurations

Item	Description	Value
T1	VCC_RTC rise to VCC rise	≥ 0 ms
T2	VCC fall to VCC_RTC fall	≥ 0 ms

Figure 35 - Input Power sequence for AT based configurations



3.20.2. Input Power Sequencing for ATX based configurations

EDM input power sequencing requirements for ATX based configurations are as follows:

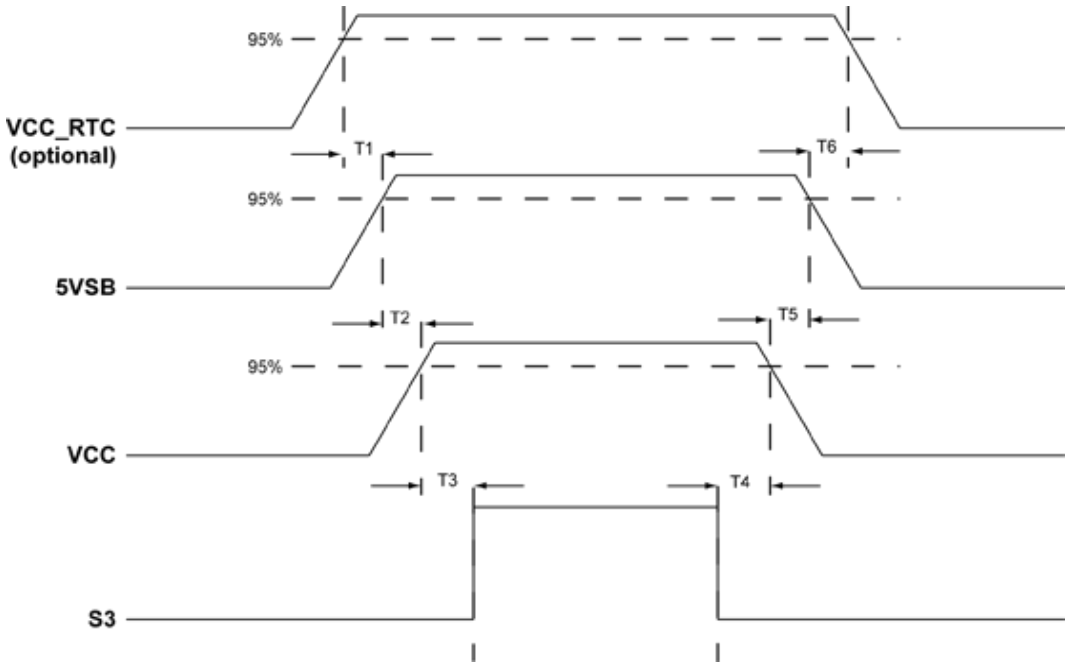
Start Sequence:
VCC_RTC must come up at the same time or before 5VSB comes up.
5VSB must come up at the same time or before VCC comes up.
PWGIN must be active at the same time or after VCC comes up.

Stop Sequence:
PWGIN must be inactive at the same time or before VCC goes down
VCC must go down at the same time or before 5VSB goes down
5VSB must go down at the same time or before VCC_RTC goes down

Table 54 - Input Power Sequencing for ATX based configurations

Item	Description	Value
T1	VCC_RTC rise to 5VSD rise	≥ 0 ms
T2	5VSB rise to VCC rise	≥ 0 ms
T3	VCC rise to PWGIN (S3) rise	≥ 0 ms
T4	PWGIN (S3) fall to VCC fall	≥ 0 ms
T5	VCC fall to 5VSB fall	≥ 0 ms
T6	5VSB fall to VCC_RTC fall	≥ 0 ms

Figure 36 - Input Power sequence for ATX based configurations



3.20.3. Power Management Signals

EDM specifies a set of signals to control the system power states such as the power-on and reset conditions. This enables the system designer to implement a fully ACPI compliant system supporting system states S3 and S5. The minimum hardware requirements for an ACPI compliant system are an EDM module supporting ACPI, ATX conforming power supply and a power button.

Table 55 - Power Management Signals

Pin #	EDM	Signal	V	I/O	Description
251	1 / 2	S3	CMOS 3.3V	O	S3 signal shuts off power to all runtime system components that are not maintained during S3 state
252	1 / 2	ON/OFF	CMOS 3.3V	I	Power ON button input signal
253	1 / 2	S5	CMOS 3.3V	O	S5 signal shuts off power to the system. Restart is only possible with power button or by a system wake up event
254	1 / 2	RESET	CMOS 3.3V	I	Reset button input signal

3.21. Watchdog Timer (WDT)

The WDT event can cause the system to reset by making appropriate carrier board connections. It also may be possible to configure the module to reset on a WDT event; check the EDM module Vendors' documentation.

If the WDT output is used to cause a system reset, the WDT output will be cleared by the system reset event. The Watchdog Timer (WDT) event signal is provided by the EDM module. The WDT output is active-high.

Pin #	EDM	Signal	V	I/O	Description
279	1 / 2	Watchdog	CMOS 3.3V	O	Watchdog event indication signal

3.22. RTC Battery Implementation

The Real Time Clock (RTC) is responsible for maintaining the time and date even when the EDM module is not connected to a main power supply. Usually a +3V lithium battery cell or super cap is used to supply the internal RTC of the Module. The EDM specification defines an optional power pin 'VCC_RTC', which connects the RTC of the EDM module to the external battery. The specified input voltage range of the battery is defined between +2.0V and +3.0V. The signal 'VCC_RTC' can be found on the EDM module's connector pin 281.

To implement a RTC Battery according to the Underwriters Laboratories Inc® (UL) guidelines, battery cells must be protected against a reverse current going to the cell. This can be done by either a series Schottky diode or a series resistor. There are two implementation possibilities and the following examples explain the advantages and disadvantages of each one.

The safest way to implement a RTC battery circuitry is by using a Schottky diode. This method offers protection against a possible explosion hazard as a result of reverse current flowing to the battery. Moreover, this implementation offers more flexibility when choosing battery type and manufacturer. Lithium batteries are the most common form of battery used in this scenario.

A big drawback of this circuitry is that the battery voltage monitoring result displayed by the EDM module will be inaccurate due to current leakage on the EDM module side. When the system is running, this current leakage loads the capacitor of the battery circuitry. This leads to a higher voltage on the signal pin 'VCC_RTC' and therefore produces inaccurate monitoring results.

Pin #	EDM	Signal	V	I/O	Description
281	1 / 2	VCC_RTC	3.3V	I	Input power for RTC clock

3.22.1. RTC Battery Lifetime

The RTC battery lifetime determines the time interval between system battery replacement cycles. Current leakage from the RTC battery circuitry on the carrier board is a serious issue and must be considered during the system design phase. The current leakage will influence the RTC battery lifetime and must be factored in when a specific life expectancy of the system battery is being defined.

In order to accurately measure the value of the RTC current, it should be measured when the complete system is disconnected from AC power.

For information about the power consumption of the RTC circuit, refer to the EDM module vendors' documentation.

4. Carrier Board PCB Layout Routing Guidelines

This section describes PCB Layout Routing guidelines and assumes a thickness for the carrier PCB to be 1.6 mm (0.62 inches) Other PCB mechanics are possible but the described stack-ups need to be adapted.

4.1. Four Layer PCB Stack-up

Figure 37 - Four Layer PCB Stack-up

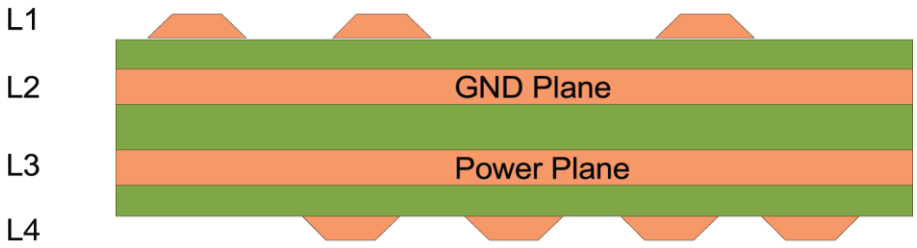


Figure 38 above is an example of a four layer stack-up. Layers L1 and L4 are used for signal routing.

Layers L2 and L3 are used for solid ground and power planes respectively.

Microstrips on layers 1 and 4 reference ground and power planes on layers 2 and 3 respectively.

In some cases, it may be advantageous to swap the GND and PWR planes. This allows Layer 4 to be GND referenced. Layer 4 is clear of parts and may be the preferred primary routing layer.

4.2. Six Layer PCB Stack-up

Figure 38 - Six Layer PCB Stack-up

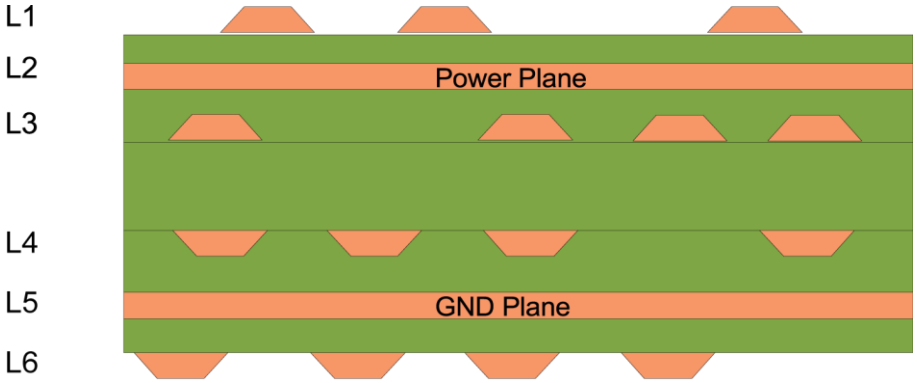


Figure 38 above is an example of a six layer stack-up. Layers L1, L3, L4 and L6 are used for signal-routing. Layers L2 and L5 are power and ground planes respectively.

Microstrips on layers 1 and 6 reference solid ground and power planes on layers 2 and 5 respectively.

Inner layers 3 and 4 are asymmetric striplines that are referenced to planes on layers 2 and 5.

4.3. Eight Layer PCB Stack-up

Figure 39 - Eight Layer PCB Stack-up

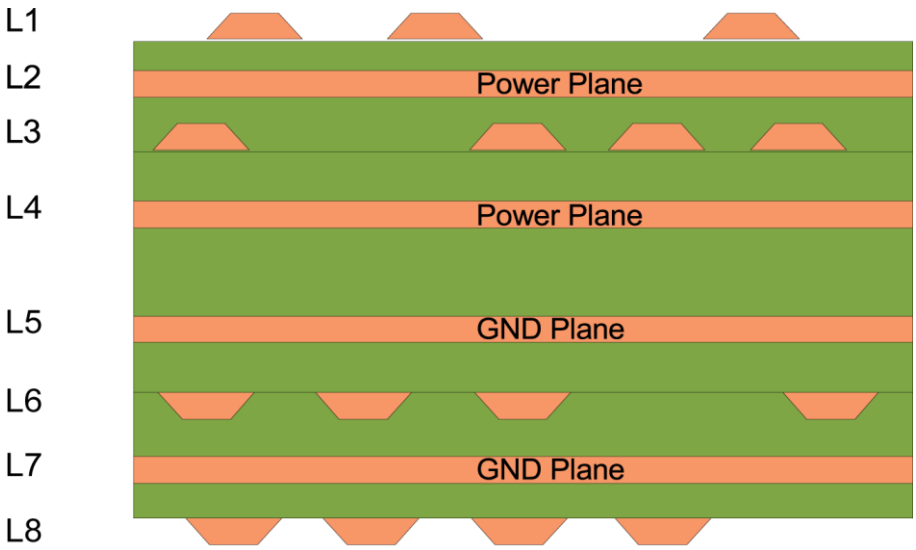


Figure 39 above is an example of an eight layer stack-up. Layers L1, L3, L6 and L8 are used for signal-routing. Layers L2 and L7 are solid ground planes, while L4 and L5 are used for power.

Microstrip layers 1 and 8 reference solid ground planes on layers 2 and 7 respectively.

Inner signal layers 3 and 6 are asymmetric striplines that route differential signals. These signals are referenced to layers 2 and 7 to meet the characteristic impedance target for these traces.

To reduce coupling to layers 4 and 5, specify thicker pre-preg to increase layer separation.

4.4. Trace-Impedance Considerations

Most high-speed interfaces used in an EDM design for a carrier board are differential pairs that need a well-defined and consistent differential and single-ended impedance. The differential pairs should be edge-coupled (i.e. the two lines in the pair are on the same PCB layer, at a consistent spacing to each other). Broadside coupling (in which the two lines in the pair track each other on different layers) is not recommended for mainstream commercial PCB fabrication.

There are two basic structures used for high-speed differential and single-ended signals. The first is known as a “microstrip”, in which a trace or trace pair is referenced to a single ground or power plane.

The outer layers of multi-layer PCBs are microstrips. A diagram of a microstrip cross section is shown in “Figure 40 - Microstrip Cross Section” below.

The second structure is the “stripline”, in which a trace or pair of traces is sandwiched between two reference planes, as shown in “Figure 41 - Strip Line Cross Section” below. If the traces are exactly halfway between the reference planes, then the stripline is said to be symmetric or balanced. Usually the traces are a lot closer to one of the planes than the other (often because there is another orthogonal trace layer, which is not shown in “Figure 41 - Strip Line Cross Section” below). In this case, the striplines are said to be asymmetric or unbalanced. Inner layer traces on multi-layer PCBs are usually asymmetric striplines.

Before proceeding with a carrier board layout, designers should decide on a PCB stack-up and on trace parameters, primarily the trace-width and differential-pair spacing. It is quite a bit harder to change the differential impedance of a trace pair after layout work is done than it is to change the impedance of a single-ended signal. That is because (with reference to “Figure 40 - Microstrip Cross Section”, “Figure 41 - Strip Line Cross Section” and “Table 56 - Trace Parameters” below) the geometric factors that have the biggest impact on the impedance of a single-ended trace are H1 and W1.

Both H1 and W1 can be manipulated slightly by the PCB vendor. The differential impedance of a trace pair depends primarily on H1, W1 and the pair pitch. A PCB vendor can easily manipulate H1 and W1 but changing the pair pitch cannot generally be done at fabrication time. It is more important for the PCB designer and the Project Engineer to determine the routing parameters for differential pairs ahead of time.

Work with a PCB vendor on a suitable board stack-up and use a PCB- impedance calculator. An easy to use and comprehensive calculator is available from Polar Instruments (www.polarinstruments.com). Alternatively, impedance calculators are included in many PCB layout packages, although these are often incomplete when it comes to differential-pair impedances. There are also quite a few free impedance calculators available on the Web. Most are very basic, but still useful.

Figure 40 - Microstrip Cross Section

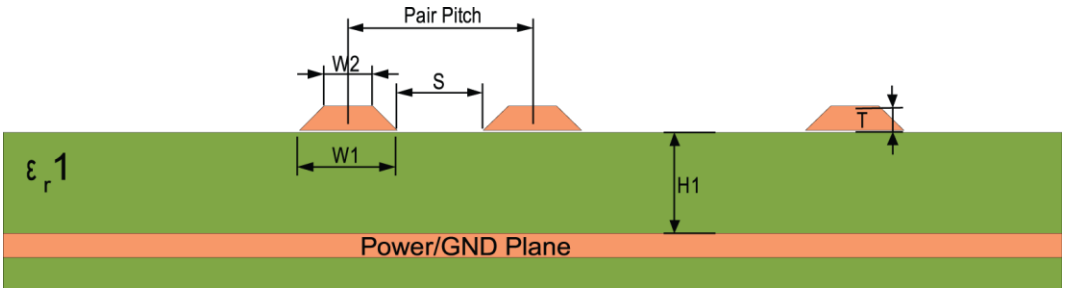


Figure 41 - Strip Line Cross Section

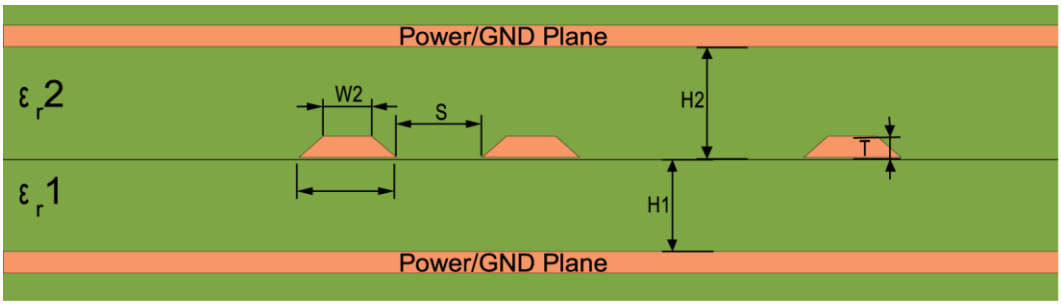


Table 56 - Trace Parameters

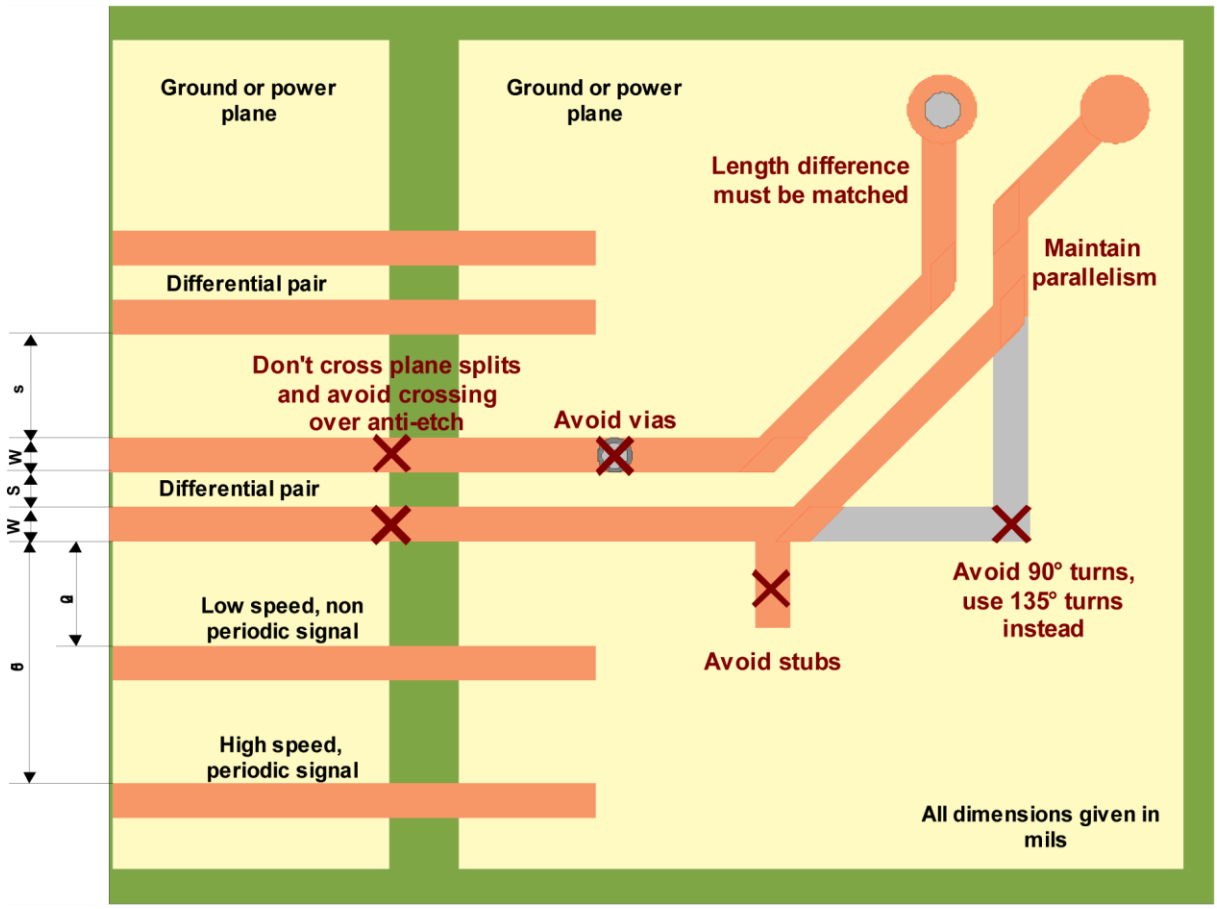
Symbol	Definition
εr1	Dielectric constant of material between the trace and the reference plane. Increasing εr1 results in lower trace impedance.
εr2	Dielectric constant of the material between the 2nd reference plane (stripline case only). Usually εr1 and εr2 are the same. Increasing εr2 results in lower trace impedance.
H1	Distance between the trace lower surface and the closer reference plane. Increasing H1 raises the trace impedance (assuming that H1 is less than H2).
H2	Distance between the trace lower surface and the more distant reference plane (stripline case only). Usually H2 is significantly greater than H1. When this is true, the lower plane shown in the figure is the primary reference plane. Increasing H2 raises the trace impedance.
Pair Pitch	The center-to-center spacing between two traces in a differential pair. Increasing the pair pitch raises the differential trace impedance.
S	The spacing or gap between two traces in a differential pair. The pair pitch is the sum of S and W1. Increasing S raises the differential trace impedance.
T	The thickness of the trace. The thickness of a ½ oz. inner layer trace is about 0.0007 inches. The thickness of a 1 oz. inner layer trace is about 0.0014 inches. Outer layer traces using a given copper weight are thicker, due to plating that is usually done on outer layers. Increasing the trace thickness lowers trace impedance.
W1, W2	W1 is the base thickness of the trace. W2 is the thickness at the top of the trace. The relation between W1 and W2 is called the “etch factor” in the PCB trade. For rough calculations, it can be assumed that W1 = W2. The etch factor is process dependent. W2 is often about 0.001 inches less than W1 for ½ oz inner layer traces; for example, a 5 mil (0.005 inch) nominal trace will be 5-mil wide at the bottom and 4-mil wide at the top. Increasing the trace-width lowers trace impedance.

4.5. Routing Rules for High-Speed Differential Interfaces

The following is a list of suggestions for designing with high-speed differential signals. This should help implement these interfaces while providing maximum EDM carrier board performance.

- Use controlled impedance PCB traces that match the specified differential impedance.
- Keep the trace lengths of the differential signal pairs as short as possible.
- The differential signal pair traces should be trace-length matched and the maximum trace-length mismatch should not exceed the specified values. Match each differential pair per segment.
- Maintain parallelism and symmetry between differential signals with the trace spacing needed to achieve the specified differential impedance.
- Maintain maximum possible separation between the differential pairs and any high-speed clocks/periodic signals (CMOS/TTL) and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).
- Route differential signals on the signal layer nearest to the ground plane using a minimum of vias and corners. This will reduce signal reflections and impedance changes. Use GND stitching vias when changing layers.
- It is best to put CMOS/TTL and differential signals on a different layer(s), which should be isolated by the power and ground planes.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn.
- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use, and/or generate, clocks.
- Stubs on differential signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50mil.
- Use a minimum of 20mil spacing between the differential signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.
- Route all traces over continuous planes (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (split planes) increases inductance and radiation levels by forcing a greater loop area.

Figure 42 - Layout Considerations



In order to determine the necessary trace width, trace height and spacing needed to fulfill the requirements of the interface specification, it's necessary to use an impedance calculator.

4.5.1. LVDS and eDP Signaling Details and Routing Guideline

Table 57 - LVDS and eDP Signaling Details and Routing Guideline

Parameter	Trace Routing
Transfer Rate	5.38 Gbits/sec (LVDS) 17.28 Gbits/sec (eDP)
Maximum signal line length (coupled traces)	6.5 inch
Maximum signal length used on EDM module	3 inch
Signal length allowance on EDM Carrier Board	3.5 inch
Cable length allowance from EDM Carrier Board connector to panel	10 inch
Differential Impedance	100 Ohms +/- 20%
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	4 mils (microstrip routing)
Spacing between differential pair signals (intra-pair)	6 mils (microstrip routing)
Spacing between pair to pairs (inter-pair)	Min. 20 mils
Spacing between differential pairs and high-speed periodic signals	Min. 20 mils
Length matching between differential pairs (intra-pair)	+/- 20 mils
Length matching between clock and data pairs (inter-pair)	+/- 20 mils
Length matching between data pairs (inter-pair)	+/- 40 mils
Spacing from edge of plane	+/- 40 mils
Reference plane	GND referenced preferred
Via Usage	Max. of 4 vias per line

4.5.2. HDMI and DP Signaling Details and Routing Guideline

Table 58 - HDMI and DP Signaling Details and Routing Guideline

Pin #	Description
Transfer Rate	10.2 Gbits/sec (HDMI) 17.28 Gbits/sec (DP)
Maximum signal length allowance on EDM Carrier Board	4 inch
Differential Impedance	100 Ohms +/- 15%
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	5 mils (microstrip routing)
Spacing between differential pair signals (intra-pair)	7 mils (microstrip routing)
Spacing between differential pairs (inter-pair)	Min. 20 mils
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils
Length matching between differential pairs (intra-pair)	Max. 5 mils
Length matching between differential pairs (inter-pair)	Max. 30 mils
Spacing from edge of plane	+/- 40 mils
Via Usage	Try to avoid vias

4.5.3. Gigabit Ethernet Signaling Details and Routing Guideline

Table 59 - Gigabit Ethernet Signaling Details and Routing Guideline

Pin #	Description
Transfer Rate	1.0 Gbits/sec
Maximum signal length allowance on EDM Carrier Board	4 inch to the magnetic module
Maximum signal length between isolation magnetics module and RJ45 connector on the EDM Carrier Board	1 inch
Differential Impedance	100 Ohms +/- 15%
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	4 mils (microstrip routing)
Spacing between differntial pair signals (intra-pair)	6 mils (microstrip routing)
Spacing between RX and TX pairs (inter-pair)	Min. 50 mils
Spacing between differential pairs and high-speed periodic signals	Min. 100 mils
Spacing between differential pairs and low-speed non periodic signals	Min. 50 mils
Length matching between differential pairs (intra-pair)	Max. 5 mils
Length matching between RX and TX pairs (inter-pair)	Max. 30 mils
Spacing between digital ground and analog ground plane (between the magnatics module and RJ45 connector)	Min. 100 mils
Spacing from edge of plane	+/- 40 mils
Via Usage	Try to avoid vias

4.5.4. PCI Express Signaling Details and Routing Guideline

Table 60 - PCI Express Signaling Details and Routing Guideline

Pin #	Description
Transfer Rate	PCIe 2.0 : 2.5 Gbits/sec PCIe 3.0 : 5.0 Gbits/sec
Maximum signal length allowance on EDM Carrier Board	5 inch to the PCIe slot 12 inch to PCIe device
Differential Impedance	100 Ohms +/- 15%
Single-ended Impedance	60 Ohms +/-15%
Trace width (W)	4 mils (microstrip routing)
Spacing between differential pair signals (intra-pair)	6 mils (microstrip routing)
Spacing between RX and TX pairs (inter-pair)	Min. 20 mils
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils
Length matching between differential pairs (intra-pair)	Max. 5 mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements.
Length matching between reference clock differential pairs (intra-pair)	Max. 5 mils
Length matching between reference clock pairs (inter-pair)	No electrical requirements.
Reference plane	GND referenced preferred
Spacing from edge of plane	+/- 40 mils
Via Usage	Max. 2 vias per trace
AC coupling capacitors	Implement type X7R, 100nF +/- 10% 16V on all datalines

4.5.5. Serial ATA Signaling Details and Routing Guideline

Table 61 - Serial ATA Signaling Details and Routing Guideline

Pin #	Description
Transfer Rate	SATA II : 3.0 Gbits/sec SATA III : 6.0 Gbits/sec
Maximum signal line length (coupled traces)	7 inch
Maximum signal length used on EDM module	3 inch
Signal length allowance on EDM Carrier Board	4 inch
Cable length allowance from EDM Carrier Board connector to SATA device	30 inch
Differential Impedance	100 Ohms +/- 20%
Single-ended Impedance	60 Ohms +/-15%
Trace width (W)	4 mils (microstrip routing)
Spacing between differential pair signals (intra-pair)	6 mils (microstrip routing)
Spacing between RX and TX pairs (inter-pair)	Min. 20 mils
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils
Length matching between differential pairs (intra-pair)	Max. 5 mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements.
Spacing from edge of plane	+/- 40 mils
Via Usage	Try to avoid vias
AC Coupling capacitors	The AC coupling capacitors for the TX and RX lines should be implemented on the EDM Carrier Board accordingly.

4.5.6. Universal Serial Bus (USB) Signaling Details and Routing Guideline

Table 62 - Universal Serial Bus (USB) Signaling Details and Routing Guideline

Pin #	Description
Transfer Rate	USB 2.0 : 480Mbits/sec USB 3.0 : 5.0 Gbits/sec
Maximum signal length allowance on EDM Carrier Board	14 inch
Differential Impedance	90 Ohms +/- 15%
Single-ended Impedance	45 Ohms +/-10%
Trace width (W)	5 mils (microstrip routing)
Spacing between differential pair signals (intra-pair)	6 mils (microstrip routing)
Spacing between pairs-to-pairs (inter-pair)	Min. 20 mils
Spacing between differntial pairs and high-speed periodic signals	Min. 50 mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils
Length matching between differential pairs (intra-pair)	Max. 150 mils
Reference plane	GND referenced preferred
Spacing from edge of plane	Min. 40 mils
Via Usage	Try to avoid vias

4.6. Routing Rules for Single Ended Interfaces

The following is a list of suggestions for designing with single ended signals. This should help implement these interfaces while providing maximum EDM carrier board performance.

- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use or generate clocks.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn.
- Stubs on signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50mil.
- Route all traces over continuous planes with no interruptions (ground reference preferred). Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (split planes) increases inductance and radiation levels by forcing a greater loop area.
- Route digital power and signal traces over the digital ground plane.
- Position the bypassing and decoupling capacitors close to the IC pins with wide traces to reduce impedance.

4.6.1. General Trace Routing Guideline

Table 63 - General Signaling Details and Routing Guideline

Pin #	Description
Transfer Rate @ 33Mhz	16Mbits/sec
Maximum signal length allowance on EDM Carrier Board for data signals	15 inch
Maximum signal length allowance on EDM Carrier Board for clock signals	8. inch
Single-ended Impedance	55 Ohms +/-15%
Trace width (W)	5 mils (microstrip routing)
Spacing between signals (inter-signal)	7 mils (microstrip routing)
Length matching between single ended signals	Max. 200 mils
Length matching between clock signals	Max. 200 mils
Reference plane	GND referenced preferred
Spacing from edge of plane	Min. 40 mils
Via Usage	Try to avoid vias

5. External Industry Standard Documents and References

The following documents and resources contain provisions which through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. However users of this standard are advised to ensure they have the latest versions of the referenced standards and documents.

References Electric Interfaces:

MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVidia Corporation (www.mxm-sig.org)

MXM Version 3.0 Connector Interoperability Design Guide, Revision 1.1 (www.mxm-sig.org)

CAN (“Controller Area Network”) Bus Standards – ISO 11898, ISO 11992, SAE J2411

CSI-2 (Camera Serial Interface version 2) The CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)

D-PHY CSI-2 physical layer standard – owned and maintained by the MIPI Alliance (www.mipi.org).

eMMC (“Embedded Multi-Media Card”) The eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org)

GBE MDI (“Gigabit Ethernet Medium Dependent Interface”) This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)

HDMI Specification, Version 1.3a, November 10, 2006 © Hitachi and other companies (www.hdmi.org)

The I^2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com)

I^2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)

JEDEC MO-300 (mSATA) defines the physical form factor of the mSATA format (www.jedec.org). The electrical connections are defined in the Serial ATA document.

JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org).

Low Pin Count Interface Specification, Revision 1.1 (LPC) (www.intel.com/design/chipsets/industry/lpc.htm)

Open LVDS Display Interface (Open LDI) Specification, v0.95, May 13, 1999, Copyright © National Semiconductor (www.national.com)

LVDS owner’s manual (www.national.com)

PCI Express Specifications (www.pci-sig.org)

PCI Express Mini Card Electromechanical Specification Revision 2.0, April 21, 2012, © PCI-SIG (www.pci-sig.org)

RS-232 (EIA “Recommended Standard 232”) This standard for asynchronous serial port data exchange dates from 1962. The original standard is hard to find. Many good descriptions of the standard can be found on-line, e.g. at Wikpedia, and in text books.

Serial ATA Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (www.sata-io.org)

SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (“Secure Digital”) (www.sdcard.org)

SMBus Specification, Revision 2.0 (www.smbus.org)

SPDIF (aka S/PDIF) (“Sony Philips Digital Interface)- IEC 60958-3

SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)

USB Specifications (www.usb.org)

VESA DisplayPort Standard, Version 1.2a (www.vesa.org)

VESA Embedded DisplayPort (eDP), Version 1.3 (www.vesa.org)

References mechanical and vibration:

ASME Y14.5M - Dimensioning and Tolerancing Standard (www.asme.org)

EIA-364-9 - Durability Test Procedure for Electrical Connectors and Contacts (www.eciaonline.org)

EIA-364-28D - Vibration Test Procedure for Electrical Connectors and Sockets (www.eciaonline.org)

EIA-364-27B - Mechanical Shock (Specified Pulse) Test Procedure for Electrical Connectors (www.eciaonline.org)

EIA-364-23B - Low Level Contact Resistance Test Procedure for Electrical Connectors and Sockets (www.eciaonline.org)

EIA-364-13C - Mating and Unmating Forces Test Procedure for Electrical Connectors (www.eciaonline.org)

EIA-364-21C - Insulation Resistance Test Procedure for Electrical Connectors, Sockets and Coaxial Contacts (www.eciaonline.org)

EIA-364-20C - Withstanding Voltage Test Procedure for Electrical Connectors, Sockets and Coaxial Contacts (www.eciaonline.org)

EIA-364-108 - Impedance, Reflection Coefficient, Return Loss and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Cable Assemblies or Interconnection Systems (www.eciaonline.org)

EIA-364-101 - Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems (www.eciaonline.org)

EIA-364-90 - Crosstalk Ratio Test Procedures for Electrical Connectors, Sockets, Cable Assemblies or Interconnect Systems (www.eciaonline.org)

EIA-364-1000.1 - Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications (www.eciaonline.org)

IPC-A-600F - Acceptability of Printed Circuit Boards (www.ipc.org)

IPC-A-610D - Acceptability of Electronic Assemblies (www.ipc.org)