

User's Manual Version 1.1



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Revision History

Version	Release Time	Description
1.0	November 2012	Initial release
1.1	Jan 2014	 Jumper JP14 is newly featured to enable/disable LVDS. See JP14 at 2.3.2. Jumpers. Jumpers JP8, JP9, JP10, JP11 are newly provided to configure LVDS features. See JP8, JP9, JP10. JP11 at 2.3.2. Jumpers. BIOS Setup utility is updated to v2.00. Newly featured settings are: 3.2.14. Intel(R) 82579LM Gigabit Network Connection on page 61 and 3.2.15. Intel(R) 82583V Gigabit Network Connection on page 62.

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Declaration of Conformity CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class B

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential

installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- -- Reorient or relocate the receiving antenna.
- -- Increase the separation between the equipment and receiver.
- -- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- -- Consult the dealer or an experienced radio/TV technician for help.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals)

regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

- 1. Disconnect your Single Board Computer from the power source when you want to work on the inside.
- 2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.
- 3. Use a grounded wrist strap when handling computer components.
- 4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

Replacing Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor.com.tw

E-mail:info@arbor.com.tw

Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

Chapter 1 Introduction

1.1. Product Highlights

- Intel[®] LGA1155 3rd / 2nd Gen. Core[™] Processors supported
- Dual Gigabit Ethernet Ports
- Dual Independent Displays
- DVI-I, DVI-D and Dual Channels 24-bit LVDS (for Windows 7 only)
- RS-485 Auto-flow Control supported
- Intel[®] AMT8.0 supported
- RAID 0, 1, 5, 10 supported
- USB 3.0 supported

1.2. About This Manual

This user's manual provides general information and installation instructions about the product. This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet, please consult your vendor before further handling.

1.3. Packing List

Before starting to install the single board, make sure the following items are shipped. If any of the following items is damaged or missing, contact your vendor immediately.



1.4. Ordering Information

MB-i77Q0	Intel [®] LGA1155 socket Core™ i7/i5/i3 embedded Micro-ATX motherboard
CPF-67Q0-C1	CPU Cooling Fan for LGA1155/1156 CPU
CBK-11-77Q0-00	Cable kit 6 x SATA cables 1 x two-port COM cable 2 x COM flat cables 2 x USB cables

1.5. Recommended CPU List

Intel® 3rd Generation

i7-3770 3.4GHz Core™ Processor
i5-3550S 3.0GHz Core™ Processor
i3-3220_3.3GHz Core™ Processor

Intel® 2nd Generation

i7-2600 3.4GHz Core™ Processor

i5-2400 3.1GHz Core™ Processor

i3-2120 3.3GHz Core™ Processor

G850 2.9GHz Pentium® Dual Core Processor

G540 2.5GHz Celeron[®] Dual Core Processor

1.6. Specification

Form Factor	Micro-ATX Industrial Motherboard				
CPU	3rd generation Intel [®] Core™ i7/i5/i3 processors in LGA1155 socket				
Chipset	Intel [®] PCH Q77				
System Memory	4 x 240-pin DDR3 DIMM sockets, supporting 1333/1600MHz SDRAM up to 32GB				
	Integrated Intel® HD Graphics 4000 and HD Graphics 2500				
Display	1 x DVI-I connector, supporting either analog RGB or DVI, resolution up to 2048 x 1536 for analog RGB and 1920 x 1200 for TMDS				
	1 x DVI-D connector, supporting resolution up to 1920 x 1200				
	Dual Channel 24-bit LVDS up to 1600 x 1200 resolution supported				
Ethornot	1 x Intel [®] 82583V Gigabit Ethernet controller				
Lulemet	1 x Intel [®] 82579LM Gigabit Ethernet PHY w/ iAMT				
I/O Chip	Fintek F71869ED + Fintek F81216AD				
BIOS	AMI BIOS				
Watchdog Timer	1~255 levels reset				
	4 x Serial ATA 300MB/s HDD transfer rate				
Sorial ATA	2 x Serial ATA 600MB/s HDD transfer rate				
	Intel® Rapid Storage Technology supported				
	RAID 0, 1, 5, 10 supported				
Serial Port	4 x COM ports: COM1~3 RS-232, COM4 RS-232/422/485 selectable w/ auto-flow control				
Universal Serial Rue	4 x USB 3.0/2.0 compatible ports				
Universal Serial Dus	10 x USB 2.0 ports				
KBMS	1 x 6-pin wafer connector for PS/2 keyboard and mouse				
	1 x PCle x16 slot				
Expansion Bus	1 x PCle x1 slot				
Expansion bus	1 x PCle x4 interface in x8 slot				
	1 x PCI slot				
Digital I/O	1 x 16-bit digital I/O, 8 in/8 out				
Audio	Realtek ALC886 HD Audio Codec, Mic-in/Line-in/Line-out				
Power Consumption	6.5A@+12V, 3.8A@+5V, 1.8A@+3.3V with Intel [®] CoreTM i7-3770 3.4GHz processor (Typical)				
Power Connector	24-pin + 4-pin ATX connector				
Certification	CE/FCC Class B				
Operating Temp.	0°C ~ 60°C (32°F ~ 140°F)				
Storage Temp.	-20°C ~ 80°C (-4°F ~ 176°F)				
Humidity	0% ~ 95% non-condensing				
Dimension (L x W)	244 x 244 mm (9.6" x 9.6")				

Chapter 2 Getting Started

2.1. Board Dimensions



2.2. Block Diagram



2.3. Jumpers & Connectors

The board comes with some connectors to join some devices and also some jumpers to alter the hardware configuration. The following in this section will explicate each of these components one-by-one.

2.3.1. Board Layout

An overview of this board's top side:



2.3.2. Jumpers

Jumper Settings

The jumper is "short" (closed) when the jumper cap is placed on pins; otherwise the jumper is "open."

JBIOS1

Function:	BIOS	S update p	oort	
Jumper Type:	2.54	mm pitch	2x4-pir	header
Setting:	Pin	Desc.	Pin	Desc.
	1	3.3V	2	GND
	3	CS0#	4	CLK
	5	SO	6	SI
	7	N/C	8	N/C



JP12

Function:	Configures Intel [®] ME mode			
Jumper Type:	2.54mm pitch 1x3-pin header			
Setting:	Pin Description			
	1-2 Disable ME	3 2 〇 —		
	2-3 Enable ME (Default)	3 2		



JP2

Function:	CMOS setup			
Jumper Type:	2.00mm pitch 1x3-pin header			
Setting:	Pin Description			
	1-2 Normal (default)			
	2-3 Clears CMOS			

Board Top



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JRS2

Function: Configures COM4 RS-232/422/485

Jumper Type:

2.00mm pitch 2x3-pin header

Setting:

Mode	RS-232 (default)	RS-422	RS-485
Pin 1-2	Short	Open	Open
Pin 3-4	Open	Short	Open
Pin 5-6	Open	Open	Short
	1 2 0 0 5 0 6	1 2 2 5 0 6	1 2 0 0 5 6



JKBMS1

Function:	Configures KB/MS power source			
Jumper Type:	2.54mm pitch 1x3-pin header			
Setting:	Pin Voltage			
	1-2 5V (Default)	3 2		
	2-3 5VSB	3 2		

Board Top



JLVDS1

Function:	Configures LCD voltage				
Jumper Type:	2.54mm pitch 1x3-pin header				
Setting:	Pin	Pin Voltage			
	1-2	3.3V	3 2 1 0		
	2-3	5V (Default)	3 2 1		



JP14

Function:	Enables/disables LVDS					
Jumper Type:	2.00mm pitch 1x3-pin header					
Setting:	Pin Description					
	1-2	Enable				
	2-3	Disable (default)				



Setting:

JP8, JP9, JP10. JP11

Function: Configures LVDS features

Jumper Type: 2.00mm pitch 1x3-pin header

Pin	Description						
1-2	On						
2-3	Off						

JP8	JP9	JP10	JP11	EDID Resolution	Color Depth	Channel
Off	Off	Off	Off	640 x 480 @ 60Hz	18-bit	Single
On	Off	Off	Off	800 x 600 @ 60Hz	18-bit	Single
Off	On	Off	Off	1024 x 768 @ 60Hz	18-bit	Single
On	On	Off	Off	1024 x 768 @ 60Hz	24-bit	Single
Off	Off	On	Off	1280 x 720 @ 60Hz	18-bit	Single
On	Off	On	Off	1280 x 800 @ 60Hz	18-bit	Single
Off	On	On	Off	1366 x 768 @ 60Hz	18-bit	Single
On	On	On	Off	1440 x 900 @ 60Hz	18-bit	Single
Off	Off	Off	On	1366 x 768 @ 60Hz	24-bit	Single
On	Off	Off	On	1440 x 900 @ 60Hz	24-bit	Single
Off	On	Off	On	1280 x 1024 @ 60Hz	24-bit	Dual
On	On	Off	On	1440 x 1050 @ 60Hz	24-bit	Dual
Off	Off	On	On	1600 x 900 @ 60Hz	24-bit	Dual
On	Off	On	On	1680 x 1050 @ 60Hz	24-bit	Dual
Off	On	On	On	1600 x 1200 @ 60Hz	24-bit	Dual
On	On	On	On	1920 x 1080 @ 60Hz	24-bit	Dual



2.3.3. Connectors

ATX12V1

Description:	ATX opera	+12V coi tion	nnecto	r to supply +12V for CPU	
Connector Type:	4-pin	ATX 12V	connec	ctor	4∥⊖∥⊖∬3
Pin Definition:	Pin	Desc.	Pin	Desc.	
	1	GND	2	GND	
	3	+12\/	4	+12\/	



FAN1, 2, 3

Description:	Fan power connectors					
Connector Type:	2.54mm pitch 1x4 wafer one wall connector					
Pin Definition:	Pin Description					
	1 GND					
	2 +12V					
	3 FAN_IN					
	4	FAN_CTL				





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2 3

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SATA1~6

Descri	ption:	Se
Descri	puon.	00

erial ATA connectors

Connector Type: Lockable SATA connectors with housing

- SATA1~2 support 600MB/s HDD transfer rate. •
 - SATA3~6support 300MB/s HDD transfer rate.

Pin Definition:

Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND





AUDIO1

Description:	Audio interface port			
Connector Type:	3 x 3.5mm phone jack stacked			
Pin Definition:	Audio Jack Description			
	Blue Line-in			
	Green Line-out			
	Pink Mic-in			





ATX1

Description:	ATX power connector

Connector Type: 24-pin ATX power supply connector

Pin Definition:

Pin	Desc.	Pin	Desc.
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PS-ON
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PW-OK	20	-5V
9	+5VSB	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	GND





JFRT1

- **Description:** Provides status LED lights for computer and switches to change the computer's activities
- Connector Type: 2.54mm pitch 2x8 pin header

Pin Definition: Pin Description Pin Description 1 2 1 LED-2 LED+ Power LED ΟC Power Button 3 **PWRBTN-**4 **PWRBTN+** System Reset 5 RESET-6 RESET+ HDD LED 0 6 Speaker+ 7 HDD LED+ 8 GND r SMBus Speaker-9 HDD LED-10 SPEAKER+ 11 SMB_CLK 12 SPEAKER+ 1516 13 SMB DATA 14 SPEAKER-15 GND 16 SPEAKER-



10 9 00

2 1

COM1, 2, 3

Description:	Seria	port con	nectors					
Connector Type:	2.54n	2.54mm pitch 2x5-pin box header.						
Pin Definition:	Pin	Pin Desc. Pin Desc.						
	10	10 N/C 9 RI1						
	8	8 CTS1 7 RTS1						
	6	DSR1	5	GND				
	4	4 DTR1 3 TXD1						
	•		4					



COM4

Description:	RS-232/422/485 connector						13.14
Connector Type:	2.54mm pitch	2х7-р	in header			I	
Pin Definition:		Pin	Desc.	Pin	Desc.		00
	RS-485/422	14	422RX-	13	422RX+	0	00
		12	422TX-485-	11	422TX+485+		
		10	N/C	9	RI		
		8	CTS	7	RTS		00
	RS-232	6	DSR	5	GND		
		4	DTR	3	TXD		
		2	RXD	1	DCD		7 l



AUDIO3

Description:	AUX audio connector						
Connector Type:	2.54mm pitch 2x5-pin box header						
Pin Definition:	Pin	Description	Pin	Description			
	1	MIC2_L	2	GND			
	3	MIC2_R	4	PRESENCE	-		
	5	LINE2_R	6	MIC2_JD			
	7	SENSE	8	N/C			
	9	LINE2_L	10	LINE2_JD			

2000010 100009



Getting Started

USB1,2

Description:	USB connectors					
Connector Type:	2.54mm pitch 2x5 pin header					



Pin Definition:	Pin	Desc.	Pin	Desc.	Pin	Desc.	Pin	Desc.	Pin	Desc.
	1	+5V	3	USBD1-	5	USBD1+	7	GND	9	N/C
	2	+5V	4	USBD2-	6	USBD2+	8	GND	10	N/C


LAN1,2

Description: Ethernet ports and double-stacked USB ports

Connector Type: RJ-45 connectors with LED and doublestacked USB type A connectors



Pin Definition:	LAN (RJ-45)				USB (USB type A connector)			
	Pin	Desc.	Pin	Desc.	B1	+5V	B5	+5V
	A1	TCT VCC	A2	M0+	B2	USBD1-	B6	USBD2-
	A3	M0-	A4	M1+	B3	USBD1+	B7	USBD2+
	A5	M1-	A6	M2+	B4	GND	B8	GND
	A7	M2-	A8	M3+	H1	GND	H5	GND
	A9	M3-	A10	RCT GND	H2	GND	H6	GND
	A11	LED1 Y-	A12	LED1 Y+	H3	GND	H7	GND
	A13	LED2 G-O+	A14	LED2 G+O-	H4	GND	H8	GND



Description:

Four USB ports

USB3

•		•						
Connector Type:	4-stack USB 3.0/2.0 type A connectors							
Pin Definition:	Pin	Desc.	Pin	Desc.	Pin	Desc.	Pin	Desc.
	11	5V	33	USBD3+	21	5V	43	USBD4+
	12	USBD1-	34	GND5	22	USBD2-	44	GND7
	13	USBD1+	35	SSRX3-	23	USBD2+	45	SSRX4-
	14	GND1	36	SSRX3+	24	GND3	46	SSRX4+
	15	SSRX1-	37	GND6	25	SSRX2-	47	GND8
	16	SSRX1+	38	SSTX3-	26	SSRX2+	48	SSTX4-
	17	GND2	39	SSTX3+	27	GND4	49	SSTX4+
	18	SSTX1-	H1	GND	28	SSTX2-	H4	GND
	19	SSTX1+	H2	GND	29	SSTX2+	H5	GND
	31	5V	H3	GND	41	5V	H6	GND
	32	USBD3-	-		42	USBD4-	-	
	52	00000-			74	00004-		





DVI2

Description:	DVI-I port and DVI-D port	DVH
Connector Type:	Female DVI-D connector and female DVI-I connector	DVI-D



LVDS1

Description:

LCD connector

Connector Type: 34-pin female LDVS connector



Pin	Desc.	Pin	Desc.
33	N.C.	34	N.C.
31	N.C.	32	N.C.
29	TX1D3-	30	TX2D3-
27	TX1D3+	28	TX2D3+
25	GND	26	GND
23	TX1D2-	24	TX2D2-
21	TX1D2+	22	TX2D2+
19	GND	20	GND
17	TX1D1-	18	TX2D1-
15	TX1D1+	16	TX2D1+
13	GND	14	GND
11	TX1D0-	12	TX2D0-
9	TX1D0+	10	TX2D0+
7	GND	8	GND
5	TX1CLK-	6	TX2CLK-
3	TX1CLK+	4	TX2CLK+
1	VDD1	2	VDD2



LVDSBL1

Description:	LCD inverter connector					
Connector Type:	2.00mm pitch 1x5-pin box wafer connector					
Pin Definition:	Pin Description					
	1 +12V/+5V					
	2 GND					
	3 Backlight on/off					
	4 Brightness control					

5 GND





JDIO1

Description:	Digital I/O connector that supports 16-bit programmable digital input/output			
Connector Type:	2.00mm pitch 2x10-pin header			

Pin	Desc.	Pin	Desc.
20	GND	19	VCC
18	GND	17	VCC
16	DIO15	15	DIO14
14	DIO13	13	DIO12
12	DIO11	11	DIO10
10	DIO9	9	DIO8
8	DIO7	7	DIO6
6	DIO5	5	DIO4
4	DIO3	3	DIO2
2	DIO1	1	DIO0

20	19



KBMUSB1

Description:	PS/2 keyboard and double-stacked USB connectors				
Connector Type:	6-pin Mini-DIN connector and double- stacked type A USB connectors				





J80P1

Description:	I/O po	I/O port 80 connector				
Connector Type:	2.00n	2.00mm pitch 2x5-pin female connector				
Pin Definition:	Pin	Description	Pin	Description	ŌČ	
	10	L_AD1	9	VCC3		
	8	L_AD2	7	L_AD3		
	6	N/C	5	P_PCIRST_N		
	4	L_AD0	3	L_FRAME_N	21	
	2	GND	1	CK P33M		



2.4. Driver Installation Notes

The board supports Windows 7. Find the necessary drivers on the CD that comes with your purchase.

Find the drivers on CD by the following paths:

Windows 7	
Driver	Path
Chipset	\MB-i77Q0\CHIPSET\Win7
AMT	\MB-i77Q0\ME\MEI_allOS_8.0.4.1441_PV_5M
Graphics	\MB-i77Q0\GRAPHICS\Win7\Win32 \MB-i77Q0\GRAPHICS\Win7\Win64
LAN	\MB-i77Q0\ETHERNET\WIN_allos_Ver16.3
Audio	\MB-i77Q0\AUDIO\Vista_Win7_R261-32_64 bit
USB3.0	\MB-i77Q0\USB3.0

Windows 7

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3.1. Install CPU

The LGA1155 processor socket comes with a lever to secure the processor. Please refer to the pictures step by step as below and note that the cover of the LGA1155 socket must always be installed during transportation to avoid damage to the socket.



Make sure that heat sink putting on the CPU's top surface is in complete contact to avoid overheating problem.

If not, it would cause your system or CPU hanged, unstable or damaged.

3.2. Install/uninstall Memory

To install the memory module:

1. Find the memory DIMM socket on the board.

The DIMM socket has a slot connector with a off-center break and a spring-loaded latch on each side to fix the DDR3 memory module in place.

 Position the memory module's pin side at the SO-DIMM socket, with the memory module's key notch aligning at the SO-DIMM socket's slot connector break.



- 3. Insert the memory module to the slot connector at an slanted angle. Note to "fully" insert the memory module to avoid improper insertion.
- 4. Press down the memory module until it auto-clicks in place.

To uninstall the memory module:

- 1. Pull back the latches from both sides of the SO-DIMM socket.
- 2.

The memory module will be auto-released from the socket.

3. Remove the memory module.

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3.1. Main

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS RAM of the system stores the Setup utility and configurations. When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILITY, press "**Delete**" once the power is turned on. When the computer is shut down, the battery on the motherboard supplies the power for BIOS RAM.

The Main Setup screen lists the following information:

Aptio Setup Utility	- Copyright (C) 2012 Americ	can Megatrends, Inc.
Main Advanced Chipset	BOOT SECURITY SAVE & EX	
BIOS Information BIOS Vendor Core Version BIOS version Build Date and Time	American Megatrends 4.6.5.3 MB-i77Q0 2.00 01/23/2014 15:49:18	Set the Date. Use Tab to switch between Date elements.
System Date System Time Access Level	[Tue 01/28/2014] [09:31:42] Administrator	<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>

Setting	Description
BIOS Information	
BIOS Vendor	displays vendor name
Core Version	displays current core version information
BIOS Version	displays current BIOS version information
Build Date and Time	the date that the BIOS version was made/updated
System Language	Choose the system default language

System Date	 Set the system date. Note that the 'Day' automatically changes when you set the date. The date format is: Day: Sun to Sat Month: 1 to 12 Date: 1 to 31 Year: 1998 to 2099 	
System Time	Set the system time.The time format is:	Hour: 00 to 23 Minute: 00 to 59 Second: 00 to 59

Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

Keystroke	Function
<►	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
▼ ▲	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select "OK" or "Cancel" for exiting and discarding changes. Use "←" and "→" to select and press "Enter" to confirm) On the Sub Menu – Exit current page and return to main menu
Page Up / +	Increase the numeric value on a selected setup item / make change
Page Down -	Decrease the numeric value on a selected setup item / make change
F1	Activate "General Help" screen
F10	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select "OK" or "Cancel" for exiting and saving changes. Use " \leftarrow " and " \rightarrow " to select and press "Enter" to confirm)

3.2. Advanced

The "Advanced" setting page provides you the options to configure the details of your hardware, such as PCI, ACPI, CPU, SATA, AMT, USB and Second Super IO.

Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc. Main <mark>Advanced</mark> Chipset Boot Security Save & Exit		
 PCI Subsystem Settings ACPI Settings CPU Configuration SATA Configuration Intel(R) Rapid Start Technology Intel(R) Anti-Theft Technology Configuration AMT Configuration USB Configuration SMART Settings H/W Monitor Second Super IO Configuration Intel(R) Smart Connect Technology CPU PPM Configuration Intel(R) 82579LM Gigabit Network Connecti - 88:88:88:88 Intel(R) 82583V Gigabit Network Connecti - 00:05:B7:DF 	<pre>PCI, PCI-X and PCI Express Settings.</pre>	

Setting	Description
PCI Subsystem Settings	See Section 3.2.1
ACPI Settings	See Section 3.2.2
CPU Configuration	See Section 3.2.3
SATA Configuration	See Section 3.2.4
Intel(R) Rapid Start Technology	See Section 3.2.5
Intel(R) Anti-Theft Technology Configuration	See Section 3.2.6
AMT Configuration	See Section 3.2.7
USB Configuration	See Section 3.2.8

SMART Settings	See Section 3.2.9
H/W Monitor	See Section 3.2.10
Second Super IO Configuration	See Section 3.2.11
Intel(R) Smart Connect Technology	See Section 3.2.12
CPU PPM Configuration	See Section 3.2.13
Intel(R) 82579LM Gigabit Network Connection	See Section 3.2.14
Intel(R) 82583V Gigabit Network Connection	See Section 3.2.15

3.2.1. PCI Subsystem Settings

Aptio Setup Utility - Copy Advanced	right (C) 2012 Americ	an Megatrends, Inc.
PCI Bus Driver Version	V 2.05.02	Enables or Disables 64bit capable Devices to be Decoded in Above
PCI 64bit Resources Handling Above 4G Decoding	[Disabled]	4G Address Space (Only if System Supports 64 bit PCI Decoding).
PCI Common Settings PCI Latency Timer VGA Palette Snoop PERR# Generation SERR# Generation	[32 PCI Bus Clocks] [Disabled] [Disabled] [Disabled]	
		<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults E10: Save and Exit</pre>
		ESC: Exit

Setting	Description
PCI 64bit Resources Handling	
Above 4G Decoding	Enable or Disable (default) 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).
PCI Common Settings	
PCI Latency Timer	 Value to be programmed into PCI Latency Timer Register. > Options: 32 (default)/64/96/128/160/192/224/248 PCI Bus Clocks.
VGA Palette Snoop	Enable or Disable (default) VGA Palette Registers Snooping.
PERR# Generation	Enable or Disable (default) PCI Device to Generate PERR#.
SERR# Generation	Enable or Disable (default) PCI Device to Generate SERR#.

3.2.2. ACPI Settings

Aptio Setup Utility - Advanced	Copyright (C) 2012 Americ	an Megatrends, Inc.
ACPI Settings		Enables or Disables System ability to Hibernate (OS/S4 Sleen
Enable Hibernation ACPI Sleep State	[Enabled] [Both S1 and S3 ava]	State). This option may be not effective with some OS.
		<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>

Setting	Description	
Enable Hibernation	Enable (default) or Disable system ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.	
ACPI Sleep State	 Select ACPI sleep state the system will enter when the SUSPEND button is pressed. Options: Suspend Disabled, S1 only(CPU Stop Clock), S3 only(Suspend to RAM), Both S1 and S3 available for OS to choose from (default). 	

3.2.3. CPU Configuration

Aptio Setup Utility - Copyright (Advanced	C) 2012 Americ	an Megatrends, Inc.
CPU Configuration		To turn on/off
Genuine Intel(R) CPU @ 2.20GHz CPU Signature Microcode Patch Max CPU Speed Min CPU Speed CPU Speed Processor Cores Intel HT Technology Intel VT-x Technology	306a4 7 2200 MHz 1600 MHz 2200 MHz 4 Supported Supported	adjacent cache lines.
Intel SMX Technology 64-bit	Supported Supported	<pre>→←: Select Screen ↓↑: Select Item Enter: Select </pre>
L1 Data Cache L1 Code Cache L2 Cache L3 Cache	32 КВ X 4 32 КВ X 4 256 КВ X 4 8192 КВ	F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit FSC: Exit
Hyper-threading Active Processor Cores Limit CPUID Maximum Execute Disable Bit Intel Virtualization Technology Hardware Prefetcher Adjacent Cache Line Prefetch	[Enabled] [All] [Disabled] [Enabled] [Disabled] [Enabled] [Enabled]	

Setting	Description
Hyper-threading	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled (default) for other OS (OS not optimized for Hyper-threading Technology). When Disabled only one thread per enabled core is enabled.

Active Processor Cores	Number of cores to enable in each processor package. ► Options: All (default), 1, 2, 3.
Limit CPUID Maximum	 Disabled for Windows XP Options: Enabled and Disabled (default).
Execute Disable Bit	XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 update 3.) ► Options: Enabled (default) and Disabled .
Intel Virtualization Technology	 When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. Options: Enabled and Disabled (default).
Hardware Prefetcher	To turn on/off the Mid Level Cache (L2) streamer prefetcher. ► Options: Enabled (default) and Disabled .
Adjacent Cache Line Prefetch	 To turn on/off prefetching of adjacent cache lines. ▶ Options: Enabled (default) and Disabled.

3.2.4. SATA Configuration

Aptio Setup Utility Advanced	- Copyright (C) 201	2 American Megatrends, Inc.
SATA Controller(s) SATA Mode Selection	[Enabled] [AHCI]	Enable or Disable SATA Device.
Serial ATA Port 0 Software Preserve Serial ATA Port 1 Software Preserve Serial ATA Port 2 Software Preserve Serial ATA Port 3 Software Preserve Serial ATA Port 4 Software Preserve Serial ATA Port 5 Software Preserve	Empty Unknown Empty Unknown Empty Unknown Empty Unknown Empty Unknown	<pre>→+: Select Screen ↓1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>
Name	Convertable (c) 2012	Ameniana Manatanadan Tan

Setting	Description
SATA Controller(s)	Enable (default) or Disable SATA Device.
SATA Mode Selection	 Determine how SATA controller(s) operate. Options: IDE, AHCI (default) and RAID.

3.2.5. Intel(R) Rapid Start Technology

Aptio Se Advanc	etup Utility ed	′ - Copyrigh	t (C) 2012 Americ	an Megatrends, Inc.
Intel(R) Ra	oid Start T	-echnology	[Disabled]	<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>
Versio	n 2.15.1236	. Copyright	(c) 2012 American	Megatrendes, Inc.

3.2.6. Intel(R) Anti-Theft Technology Configuration

Disabling Intel(R) AT Allow User to login to platform. This is strictly for testing only. This does not disable Intel(R) AT Services in ME.

Aptio Setup Utility - Copyright (Advanced	C) 2012 Americ	an Megatrends, Inc.
Intel(R) Anti-Theft Technology Conf	iguration	Enable/Disable Intel (R) AT in BIOS for
<pre>Intel(R) Anti-Theft Technology Intel(R) Anti-Theft Technology Rec Enter Intel(R) AT Suspend Mode</pre>	[Enabled] 3 [Disabled]	testing only.
		<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>
Varsion 2 15 1236 Convright (c)	2012 Amorican	Magatrondos Inc

Setting	Description
Intel(R) Anti-Theft Technology	Enable or Disable (default) Intel(R) AT in BIOS for testing only.
Intel(R) Anti-Theft Technology Rec	Set the number of times Recovery attempted will be allowed.

3.2.7. AMT Configuration

Aptio Setup Utility - Copyright (Advanced	C) 2012 Americ	can Megatrends, Inc.
Intel AMT ASF Activate Remote Assistance Process AMT CIRA Timeout	[Enabled] [Enabled] [Disabled] 0	Enable/Disable Intel (R) Active Management Technology BIOS Extension. Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution.If enabled, this requires additional firmware in the SPI device →+: Select Screen ↓1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit

Setting	Description
Intel AMT	Enable (default) or Disable Intel (R) Active Management Technology BIOS Extension. Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device
ASF	Enable (default) or Disable Alert Specification Format.
Activate Remote Assistance Process	Trigger CIRA boot.▶ Options: Enabled and Disabled (default).

3.2.8. USB Configuration

Aptio Setup Utility - Copy Advanced	right (C) 2012 Americ	can Megatrends, Inc.
USB Configuration		Enables Legacy USB
USB Devices: 1 Keyboard, 1 Mouse, 2	Hubs	disables legacy support if no USB devices are connected. DISABLE option will
Legacy USB Support USB3.0 Support USB Beep Switch Port 60/64 Emulation	[Enabled] [Enabled] [Enabled] [Enabled]	keep USB devices available only for EFI applications.
		<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>

Setting	Description	
Legacy USB Support	Enables (default) Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.	
USB3.0 Support	Enable (default) or Disable USB3.0 (XHCI) Controller support.	
USB Beep Switch	Enable (default) or Disable USB Beep sound.	
Port 60/64 Emulation	Enable (default) I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.	

3.2.9. SMART Settings

Aptio Setup Utility Advanced	/ - Copyright (C) 2012 A	umerican Megatrends, Inc.
SMART Settings		Run SMART Self Test on all HDDs during POST.
SMART Self Test	[Disabled]	
		<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>
Version 2.15.1236	. Copyright (c) 2012 Ame	rican Megatrendes, Inc.

Setting	Description
SMART Self Test	 Run SMART Self Test on all HDDs during POST. Options: Enabled and Disabled (default).

3.2.10. H/W Monitor

Aptio Setup Utility - Copyright Advanced	(C) 2012 American	n Megatrends, Inc.
FAN1 Mode setting[Auto FaCPU Temperature Limit of HighesCPU Temperature Limit of LowestSYSF1 Highest SettingSYSF1 Second SettingSYSF1 Lowest SettingFAN2 Mode settingFAN2 Mode settingSYS Temperature Limit of HighesSYS Temperature Limit of LowestSYSF2 Highest SettingSYSF2 Lowest SettingSYSF2 Lowest SettingSYSF2 Lowest SettingSYS Temperature Limit of HighesSYS Temperature Limit of HighesSYS Temperature Limit of HighesSYS Temperature Limit of LowestSYSF3 Highest SettingSYSF3 Highest SettingSYSF3 Lowest SettingPC Health Status	h by PWM Duty] F 55 45 100 70 50 55 45 100 70 55 45 100 70 50 50 55 45 100 70 55 45 45 45 45 100 70 55 55 55 55 55 55 55 55 55 55 55 55 55	AN Control Mode setting +-: Select Screen 1: Select Item inter: Select -/-: Change Opt. 1: General Help 2: Previous Values 9: Optimized Defaults 10: Save and Exit CC: Exit
CPU Temperature System temperature2 System temperature FAN1 Speed FAN2 Speed FAN3 Speed Vcore +3.3V +1.05V VDIMM +5V +12V	: +26°C : +25°C : +27°C : N/A : N/A : 2400 RPM : +0.904 V : +3.408 V : +1.032 V : +1.493 V : +5.003 V : +12.056 V	

Setting	Description
FAN1/2/3 Mode setting	 Fan Control Mode Setting Options: Manual Duty Mode and Auto Fan by PWM Duty (default).

CPU/SYS Temperature Limit of Highest	Highest Temperature Setting. Min=0 Max=127 Please input Dec number:
CPU/SYS Temperature Limit of Lowest	Lowest Temperature Setting. Min=0 Max=127 Please input Dec number:
SYSF1/2/3 Highest	Highest Speed Value
Setting	Min=0 Max=100 Please input Dec number:
SYSF1/2/3 Second	Second Speed Value
Setting	Min=0 Max=100 Please input Dec number:
SYSF1/2/3 Lowest	Lowest Speed Value
Setting	Min=0 Max=100 Please input Dec number:

3.2.11. Second Super IO Configuration

Aptio Setup Utility - Copyright Advanced	(C) 2012 Americ	an Megatrends, Inc.
Second Super IO Configuration Super IO Chip > Serial Port 1 Configuration > Serial Port 2 Configuration > Serial Port 3 Configuration > Serial Port 4 Configuration	Fintek F81216	Set Parameters of Serial Port 1 (COMA)
		<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>
Version 2 15 1236 Convright (r) 2012 American	Megatrendes Inc

Aptio Setup Utility Advanced	/ - Copyright (C) 2012 Americ	can Megatrends, Inc.
Serial Port 4 Configur	ration	Enable or Disable
Serial Port	[Enabled]	Serial Port (COM)
I/O Settings IRQ Settings	[IO=2E8h] [IRQ3]	
COM4 RS485 AutoFlow	[Disable]	
		→←: Select Screen ↓↑: Select Item
		Enter: Select
		F1: General Help
		F2: Previous Values F9: Optimized Defaults
		F10: Save and Exit ESC: Exit

Setting	Description
Serial Port	Enable (default) or Disable Serial Port (COM)
I/O Settings	Select an optimal setting for Super IO device. ► Options: IO=3F8h/2F8h/3E8h/2E8h/2F0h/2E0h
IRQ Settings	Select an optimal setting for Super IO device. ► Options: IRQ3/4/5/6/7/10/11/12
COM4 RS485 AutoFlow (only for Serial Port 4)	COM4 RS485 Autoflow ► Options: Enabled and Disabled (default).

Aptio Setup Utility Advanced	y - Copyright (C)	2012 American Megatrends, Inc.
ISCT Configuration	[Disabled]	Enable/Disable ISCT Configuration. →+: Select Screen ↓1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit
Version 2.15.1236	. Copyright (c) 20	012 American Megatrendes, Inc.
Setting	Description	

3.2.12. Intel(R) Smart Connect Technology

Setting	Description
ISCT Configuration	Enable or Disable (default) ISCT Configuration

3.2.13. CPU PPM Configuration

Aptio Setup Utility - Advanced	- Copyright (C) 2012 Am	erican Megatrends, Inc.
CPU PPM Configuration EIST Turbo Mode CPU C3 Report CPU C6 Report CPU C7 Report	[Enabled] [Enabled] [Enabled] [Enabled] [Enabled]	Enable/Disable Intel SpeedStep.
		<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>

Setting	Description
EIST	Enable (default) or Disable Intel SpeedStep
Turbo Mode	Enable (default) or Disable Turbo Mode
CPU C3 Report	Enable (default) or Disable CPU C3(ACPI C2) report to OS
CPU C6 Report	Enable (default) or Disable CPU C6(ACPI C3) report to OS
CPU C7 Report	Enable (default) or Disable CPU C7(ACPI C3) report to OS

PORT CONFIGURATION MENU Enable/Disable Intel >NIC Configuration SpeedStep. Blink LEDS (range 0-15 seconds) 0 PORT CONFIGURATION INFORMATION Intel(R) PRO/1000 4.8.01 Adapter PBA: FFFFFF-OFF Chip Type: Intel PCH2 PCI Device ID 1502 PCI Bus:Device:Function 00:25:00 Link Status [Disconnected]] Factory MAC Address 88:88:88:87:88	Aptio Setup Utility - Co Advanced	pyright (C) 2012 America	an Megatrends, Inc.
Blink LEDS (range 0-15 seconds) 0 PORT CONFIGURATION INFORMATION UEFI Driver: Intel(R) PRO/1000 4.8.01 Adapter PBA: FFFFFF-0FF Chip Type: Intel PCH2 PCI Device ID 1502 PCI Bus:Device:Function 00:25:00 Link Status [Disconnected] Factory MAC Address 88:88:88:87:88	PORT CONFIGURATION MENU ▶NIC Configuration		Enable/Disable Intel SpeedStep.
F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit	Blink LEDS (range 0-15 seconds) PORT CONFIGURATION INFORMATION UEFI Driver: Adapter PBA: Chip Type: PCI Device ID PCI Bus:Device:Function Link Status Factory MAC Address	0 Intel(R) PRO/1000 4.8.01 FFFFF-OFF Intel PCH2 1502 00:25:00 [Disconnected] 88:88:88:88:87:88	<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>

3.2.14. Intel(R) 82579LM Gigabit Network Connection

Submenu / Setting	Description		
	Configures the network device port by the following settings:		
	Setting	Description	
NIC Configuration	Link Speed	 Changes the link speed and the duplex for the current port. Options: AutoNeg, 10 Mbps Half, 10 Mbps Full, 100 Mbps Half and 100 Mbps Full. 	
	Wake on LAN	Enables/disables waking the system with a network message.	
Blink LEDs (range 0-15)	Specifies the duration for Blink LEDs. (Configurable are 0 to 15 seconds.)		
Link Status	Shows the link status.		

3.2.15. Intel(R) 82583V Gigabit Network Connection

Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc. Advanced			
PORT CONFIGURATION MENU ▶NIC Configuration		Enable/Disable Intel SpeedStep.	
Blink LEDS (range 0-15 seconds) PORT CONFIGURATION INFORMATION UEFI Driver: Adapter PBA: Chip Type: PCI Device ID PCI Bus:Device:Function Link Status Factory MAC Address	0 Intel(R) PRO/1000 4.8.01 FFFFF-OFF Intel 82583V 1502 02:00:00 [Disconnected] 00:05:B7:DF:3B:6F	→+: Select Screen ↓1: Select Item Enter: Select +/-: Change Opt. F1: General Help	
		F9: Optimized Defaults F10: Save and Exit ESC: Exit	

Submenu / Setting	Description		
	Configures the network device port by the following settings:		
NIC Configuration	Setting	Description	
	Link Speed	 Changes the link speed and the duplex for the current port. Options: AutoNeg, 10 Mbps Half, 10 Mbps Full, 100 Mbps Half and 100 Mbps Full. 	
	Wake on LAN	Enables/disables waking the system with a network message.	
Blink LEDs (range 0-15)	Specifies the duration for Blink LEDs. (Configurable are 0 to 15 seconds.)		
Link Status	Shows the link status.		
3.3. Chipset

Aptio Setup Utility - Copyright (C Main Advanced <mark>Chipset</mark> Boot Securi) 2012 American Megatrends, Inc. ty Save & Exit
 PCH-IO Configuration System Agent (SA) Configuration 	PCH Parameters →←: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults
	F10: Save and Exit ESC: Exit
Version 2.15.1236. Copyright (c)	2012 American Megatrendes, Inc.
Setting	Description

Setting	Description
PCH-IO Configuration	See Section 3.3.1
System Agent (SA) Configuration	See Section 3.3.2

3.3.1. PCH-IO Configuration

Aptio Setup Utility - Copyr Chipset	ight (C) 2012 Amer	ican Megatrends, Inc.
Intel PCH RC Version Intel PCH SKU Name Intel PCH Rev ID > PCH Express Configuration > USB Configuration	1.2.0.1 QM77 04/C1	PCI Express Configuration settings
PCH LAN Controller Wake on LAN	[Enabled] [Enabled]	
High Precision Event Timer Co High Precision Timer Restore AC Power LOSS	nfiguration [Enabled] [Power Off]	<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt.</pre>
		F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit

Setting	Description
PCH Express Configuration	See PCH Express Configuration tab
USB Configuration	See USB Configuration tab
PCH LAN Controller	Enable (default) or Disable onboard NIC.
Wake on LAN	Enable (default) or Disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)
High Precision Event Timer Configuration	
High Precision Timer	Enable (default) or Disable the High Precision Event Timer.
Restore AC Power LOSS	 Select AC power state when power is reapplied after a power failure. Options: Power Off (default), Power On and Last State.

PCH Express Configuration

Aptio Setup Utility - Copyright (C) 2012 A Chipset	umerican Megatrends, Inc.
PCI Express Configuration	PCI Express GLAN2 82583V Settings.
PCIE Port 2 is assigned to GLAN1 ► PCI Express GLAN2 82583V ► PCI Express x1 slot ► PCI Express x4 slot	
	<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>
Version 2.15.1236. Copyright (c) 2012 Ame	rican Megatrendes, Inc.

PCI Express Root Port 3 [Enabled] ASPM Support [Auto] PME SCI [Enabled] Hot Plug [Disabled] PCIe Speed [Auto] →+: Select Screen ↓1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit F10: Save and Exit F10: Save and Exit	Aptio Setup Utility - Chipset	Copyright (C) 2012 Americ	can Megatrends, Inc.
	PCI Express Root Port 3 ASPM Support PME SCI Hot Plug PCIe Speed	[Enabled] [Auto] [Enabled] [Disabled] [Auto]	Control the PCI Express Root Port. →+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Evit

Setting	Description
PCI Express Root Port 3/4/x4	 Control the PCI Express Root Port. Options: Enabled (default) and Disabled.
ASPM Support	 Set the ASPM Level: Force L0 - Force all links to L0 State; AUTO - BIOS auto configure; DISABLE - Disable ASPM Options: Disabled, L0s, L1, L0sL1, Auto (default)
PME SCI	Enable (default) or Disable PCI Express PME SCI.
Hot Plug	Enable or Disable (default) PCI Express Hot Plug.
PCIe Speed	 Select PCI Express port speed. Options: Auto (default), Gen1, Gen2

USB Configuration

Aptio Setup Utility - Copyright (C Chipset	C) 2012 America	an Megatrends, Inc.
USB Configuration		Enable or disable XHCI Pre-Boot Driver
XHCI Pre-Boot Driver XHCI Mode HS Port #1 Switchable HS Port #2 Switchable HS Port #3 Switchable HS Port #4 Switchable XHCI Streams	[Enabled] [Smart Auto] [Enabled] [Enabled] [Enabled] [Enabled] [Enabled]	support.
EHCI1	[Enabled]	wit Soloct Scroon
EHCI2	[Enabled]	<pre>↓↑: Select Item Enter: Select</pre>
USB Ports Per-Port Disable Control	[Disabled]	+/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit

Setting	Description
XHCI Pre-Boot Driver	Enable (default) or Disable XHCI Pre-Boot Driver support.
xHCI Mode	 Mode of operation of xHCI controller. Options: Smart Auto (default), Auto, Enabled, Disabled
HS Port #1/2/3/4 Switchable	 Always for HS port switching between xHCI and EHCI. If disabled, port is routed to EHCI. If HS port is routed to xHCI, the corresponding SS port is enabled. ▶ Options: Enabled (default) and Disabled.
xHCI Streams	Enable (default) or Disable xHCI Maximum Primary Stream Array Size.

EHCI1/2	 Control the USB EHCI (USB 2.0) functions. One EHCI controller must always be enabled. Options: Enabled (default) and Disabled.
USB Ports Per-Port Disable Control	 Control each of the USB ports (0~13) disabling. Options: Enabled and Disabled (default).

3.3.2. System Agent (SA) Configuration

Aptio Setup Utility - C Chipset	opyright (C) 2012 Ameri	ican Megatrends, Inc.
System Agent Bridge Name System Agent RC version VT-d Capability	IvyBridge 1.2.0.0 Supported	Check to enable VT-d function on MCH.
VT-d	[Enabled]	
 LCD Control Graphics Configuration NB PCIe Configuration Memory Configuration 		
		<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>

Setting	Description
VT-d	 Check to enable VT-d function on MCH. Options: Enabled (default) and Disabled.
LCD Control	See LCD Control tab
Graphics Configuration	See Graphics Configuration tab
NB PCIe Configuration	See NB PCIe Configuration tab
Memory Configuration	See Memory Configuration tab

LCD Control

Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc. Chipset		
LCD Control Primary IGFX Boot Display Panel Scaling Panel Color Depth	[VBIOS Default] [Auto] [18 Bit]	Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display →+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit

Setting	Description
Primary IGFX Boot Display	 Select the Video Device that will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display. Options: VBIOS Default (default), CRT, LFP, DVI-I, DVI-D
Panel Scaling	Select the LCD panel scaling option used by the Internal Graphics Device. ► Options: Auto (default), Force Scaling
Panel Color Depth	Select the LFP Panel Color Depth Options: 18 Bit (default), 24 Bit

Graphics Configuration

Aptio Setup Utility - Chipset	· Copyright (C) 2012 Americ	can Megatrends, Inc.
Graphics Configuration IGFX VBIOS Version IGfx Frequency Primary Display Internal Graphics GTT Size Aperture Size DVMT Pre-Allocated DVMT Total Gfx Mem	2132 400 MHz [Auto] [Auto] [2MB] [256MB] [64M] [256M]	Select which of IGFX/ PEG/PCI Graphics device should be Primary Display Or Select SG for switchable Gfx.
		<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>

Setting	Description
Primary Display	Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx. ► Options: Auto (default), Disabled, Enabled
Internal Graphics	 Keep IGD enabled based on the setup options. Options: Auto (default), Disabled, Enabled
GTT Size	Select the GTT Size ► Options: 1MB , 2MB (default)
Aperture Size	Select the Aperture Size ► Options: 128MB, 256MB (default), 512MB
DVMT Pre-Allocated	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device ▶ Options: 32/64 (default) /96/128/160/192/224/ 256/288/320/352/384/416/448/480/512/1024M

	Select DVMT5.0 Total Graphic Memory size used
DVMT Total Gfx Mem	by the Internal Graphics Device
	Options: 128M, 256M (default), MAX

NB PCIe Configuration

Aptio Setup Utility - Copy Chipset	right (C) 2012 Ame	erican Megatrends, Inc.
NB PCIe Configuration PEGO PEGO - Gen X PEGO ASPM	Not Present [Auto] [Auto]	Configure PEGO B0:D1:F0 Gen1-Gen3
Enable PEG Detect Non-Compliance Device De-emphasis Control	[Auto] [Disabled] [-3.5 dB]	
		<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>

Setting	Description
PEG0 - Gen X	Configure PEG0 B0:D1:F0 Gen1-Gen3 ▶ Options: Auto (default), Gen1, Gen2, Gen3
PEG0 ASPM	 Control ASPM support for the PEG: Device 1 Function 0. This has no effect if PEG is not the currently active device. Options: Disabled, Auto (default), ASPM L0s, ASPM L1, ASPM L0sL1

Enable PEG	To enable or disable the PEG. ► Options: Disabled , Enabled , Auto (default)
Detect Non- Compliance Device	Detect Non-Compliance PCI Express Device in PEG ► Options: Enabled and Disabled (default).
De-emphasis Control	Configure the De-emphasis control on PEG ► Options: -6 dB , -3.5 dB (default)

Memory Configuration

Aptio Setup Utility - Copyright Chipset	(C) 2012 America	an Megatrends, Inc.
Memory Information Memory RC Version Memory Frequency Total Memory DIMM#0 DIMM#1 DIMM#2 DIMM#3 CAS Latency (tCL) Minimum delay time CAS to RAS (tRCDmin) Row Precharge (tRPmin) Active to Precharge (tRASmin)	1.2.0.0 1333 MHz 4096 MB (DDR3) 4096 MB (DDR3) Not Present Not Present 9 9 9 24	<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>
Version 2.15.1236. Copyright (d	c) 2012 American	Megatrendes, Inc.

3.4. Boot

Aptio Setup Utility - Main Advanced Chipset B	Copyright (C) 2012 Americ oot Security Save & E>	can Megatrends, Inc. Mit
Boot Configuration Setup Prompt Timeout Bootup NumLock State	1 [On]	Select the Keyboard NumLock state
Quiet Boot Fast Boot	[Disabled] [Disabled]	
CSM16 Module Version	07.69	
Option ROM Messages INT19 Trap Response	[Force BIOS] [Immediate]	
Boot Option Priorities		→←: Select Screen ↓↑: Select Item Enter: Select
► CSM parameters		+/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit

Setting	Description
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	Select the keyboard NumLock stateOptions: On (default), Off
Quiet Boot	Enable or Disable (default) Quiet Boot option.
Fast Boot	Enable or Disable (default) boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.
Option ROM Messages	Set display mode for Option ROM. Options: Force BIOS (default) and Keep Current .
INT19 Trap Response	 BIOS reaction on INT19 trapping by Option ROM: IMMEDIATE - execute the trap right away; POSTPONED - execute the trap during legacy boot. ▶ Options: Immediate (default) and Postponed.

CSM parameters	See Section 3.4.1
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3.4.1. CSM parameters

Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc.		
Launch CSM Launch PXE OpROM policy Launch Storage OpROM policy Launch Video OpROM policy	[Always] [Do not launch] [Legacy only] [Legacy only]	This option controls if CSM will be launched →+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit

Setting	Description
Launch CSM	 This option controls if CSM will be launched. ▶ Options: Always (default), Never.
Launch PXE OpROM policy	 Controls the execution of UEFI and Legacy PXE OpROM. Options: Do not launch (default), Legacy only.
Launch Storage OpROM policy	 Controls the execution of UEFI and Legacy Storage OpROM. Options: Do not launch, Legacy only (default).

Launch Video OpROM	Controls the execution of UEFI and Legacy Video OpROM.	
policy	 Options: Do not launch, Legacy only (default). 	

3.5. Security

The **Security** menu sets up the administrator or user password. Once an administrator password is set up, this BIOS SETUP utility is limited to access and will ask for the password each time any access is attempted.

Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc. Main Advanced Chipset Boot <mark>Security</mark> Save & Exit		
Password Description		Set Administrator Password
If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup. If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights. The password length must be in the following		
range: Minimum length Maximum length	3 20	<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. 51: Compred Welp</pre>
Administrator Password User Password		F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit

Setting	Description
Administrator/User	 To set up an administrator password: Select Administrator Password.
Password	The screen then pops up an Create New Password dialog. Enter your desired password that is no less than 3 characters and no more than 20 characters. Hit [Enter] key to submit.

3.6. Save & Exit Options

Aptio Setup Utility - Copyright (C) 2012 American Megatrends, Inc. Main Advanced Chipset Boot Security <mark>Save & Exit</mark>		
Save Changes and Exit Discard Changes and Exit Restore Defaults	Exit system setup after saving the changes.	
Boot Override		
	<pre>→+: Select Screen ↓↑: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F9: Optimized Defaults F10: Save and Exit ESC: Exit</pre>	

Setting	Description
Save Changes and Exit	 Saves the changes and resets the system. Enter the item and then a dialog box pops up: Save configuration and exit?
Discard Changes and Exit	 Exit system setup without saving any changes. Enter the item and then a dialog box pops up: Quit without saving?
Restore Defaults	 Restore/Load Default values for all the setup options. ► Enter the item and then a dialog box pops up: Load Optimized Defaults?
Boot Override	Boot Override presents a list of boot devices on screen. Select the device to boot up the system regardless of the currently configured boot priority.



Appendix A. AMI BIOS Checkpoints

A.1. Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

A.2. Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)

0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress	Codes
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Code	es
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error

0xEC-0xEF	Reserved for future AMI error codes
Recovery Progres	ss Codes
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error C	odes
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description		
0x60	DXE Core is started		
0x61	NVRAM initialization		
0x62	Installation of the South Bridge Runtime Services		
0x63	CPU DXE initialization is started		
0x64	CPU DXE initialization (CPU module specific)		
0x65	CPU DXE initialization (CPU module specific)		
0x66	CPU DXE initialization (CPU module specific)		
0x67	CPU DXE initialization (CPU module specific)		
0x68	PCI host bridge initialization		
0x69	North Bridge DXE initialization is started		
0x6A	North Bridge DXE SMM initialization is started		
0x6B	North Bridge DXE initialization (North Bridge module specific)		
0x6C	North Bridge DXE initialization (North Bridge module specific)		
0x6D	North Bridge DXE initialization (North Bridge module specific)		
0x6E	North Bridge DXE initialization (North Bridge module specific)		
0x6F	North Bridge DXE initialization (North Bridge module specific)		
0x70	South Bridge DXE initialization is started		
0x71	South Bridge DXE SMM initialization is started		
0x72	South Bridge devices initialization		
0x73	South Bridge DXE Initialization (South Bridge module specific)		
0x74	South Bridge DXE Initialization (South Bridge module specific)		
0x75	South Bridge DXE Initialization (South Bridge module specific)		
0x76	South Bridge DXE Initialization (South Bridge module specific)		
0x77	South Bridge DXE Initialization (South Bridge module specific)		
0x78	ACPI module initialization		
0x79	CSM initialization		
0x7A-0x7F	Reserved for future AMI DXE codes		
0x80 – 0x8F	OEM DXE initialization codes		
0x90	Boot Device Selection (BDS) phase is started		
0x91	Driver connecting is started		
0x92	PCI Bus initialization is started		

0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug

0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0-0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

Appendix B: I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.

The following table lists the I/O port addresses used.

Address	Device Description		
0x0000020-0x00000021	Programmable interrupt controller		
0x00000024-0x00000025	Programmable interrupt controller		
0x0000028-0x00000029	Programmable interrupt controller		
0x0000002C-0x0000002D	Programmable interrupt controller		
0x0000030-0x00000031	Programmable interrupt controller		
0x00000034-0x00000035	Programmable interrupt controller		
0x0000038-0x00000039	Programmable interrupt controller		
0x000003C-0x000003D	Programmable interrupt controller		
0x000000A0-0x000000A1	Programmable interrupt controller		
0x000000A4-0x000000A5	Programmable interrupt controller		
0x000000A8-0x000000A9	Programmable interrupt controller		
0x000000AC-0x000000AD	Programmable interrupt controller		
0x000000B0-0x000000B1	Programmable interrupt controller		
0x000000B4-0x000000B5	Programmable interrupt controller		
0x000000B8-0x000000B9	Programmable interrupt controller		
0x000000BC-0x000000BD	Programmable interrupt controller		
0x000004D0-0x000004D1	Programmable interrupt controller		
0x000004D0-0x000004D1	Motherboard resources		
0x00000040-0x00000043	System timer		
0x00000050-0x00000053	System timer		
0x0000F0D0-0x0000F0D7	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E02		
0x0000F0C0-0x0000F0C3	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E02		
0x0000F0B0-0x0000F0B7	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E02		
0x0000F0A0-0x0000F0A3	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E02		
0x0000F060-0x0000F07F	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E02		
0x0000000-0x0000001F	Direct memory access controller		

0x0000000-0x0000001F	PCI bus
0x0000081-0x0000091	Direct memory access controller
0x00000093-0x0000009F	Direct memory access controller
0x00000C0-0x00000DF	Direct memory access controller
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x000003E8-0x000003EF	Communications Port (COM3)
0x000002E8-0x000002EF	Communications Port (COM4)
0x00000D00-0x0000FFFF	PCI bus
0x0000E000-0x0000EFFF	Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 3 - 1E14
0x00000070-0x00000077	System CMOS/real time clock
0x0000070-0x00000077	Motherboard resources
0x0000F0E0-0x0000F0E7	Intel(R) Active Management Technology - SOL (COM5)
0x0000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000044-0x0000005F	Motherboard resources
0x0000062-0x0000063	Motherboard resources
0x00000065-0x0000006F	Motherboard resources
0x00000065-0x0000006F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x0000080-0x0000080	Motherboard resources
0x0000080-0x0000080	Motherboard resources
0x0000084-0x0000086	Motherboard resources
0x0000088-0x0000088	Motherboard resources
0x000008C-0x000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources
0x00000290-0x0000029F	Motherboard resources
0x0000F000-0x0000F03F	Intel(R) HD Graphics 4000
0x000003B0-0x000003BB	Intel(R) HD Graphics 4000
0x000003C0-0x000003DF	Intel(R) HD Graphics 4000
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources

0x0000061-0x0000061	Motherboard resources
0x0000063-0x0000063	Motherboard resources
0x0000067-0x0000067	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x00000200-0x0000020F	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x00000400-0x00000453	Motherboard resources
0x00000458-0x0000047F	Motherboard resources
0x00000500-0x0000057F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x000000F0-0x000000FF	Numeric data processor
0x0000F040-0x0000F05F	Intel(R) 7 Series/C216 Chipset Family SMBus Host Controller - 1E22
0x00000454-0x00000457	Motherboard resources

Appendix C: Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System timer
IRQ 4	Communications Port (COM1)
IRQ 4	Communications Port (COM3)
IRQ 3	Communications Port (COM2)
IRQ 3	Communications Port (COM4)
IRQ 8	System CMOS/real time clock
IRQ 13	Numeric data processor
IRQ 11	Intel(R) 7 Series/C216 Chipset Family SMBus Host Controller - 1E22

Appendix D: BIOS Memory Mapping

Address	Device Description	
0xF7D40000-0xF7D5FFFF	Intel(R) 82583V Gigabit Network Connection	
0xF7C00000-0xF7CFFFFF	Intel(R) 82583V Gigabit Network Connection	
0xF7C00000-0xF7CFFFF	Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 3 - 1E14	
0xF7D60000-0xF7D63FFF	Intel(R) 82583V Gigabit Network Connection	
0xF7E37000-0xF7E373FF	Intel(R) 7 Series/C216 Chipset Family USB Enhanced Host Controller - 1E26	
0xF7E36000-0xF7E367FF	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E02	
0xFED00000-0xFED003FF	High Precision Event Timer, HPET	
0xF7E38000-0xF7E383FF	Intel(R) 7 Series/C216 Chipset Family USB Enhanced Host Controller - 1E2D	
0xF7E20000-0xF7E2FFFF	Intel (R) USB 3.0 Extensible Host Controller	
0xA0000-0xBFFFF	PCI bus	
0xA0000-0xBFFFF	Intel(R) HD Graphics 4000	
0xD0000-0xD3FFF	PCI bus	
0xD4000-0xD7FFF	PCI bus	
0xD8000-0xDBFFF	PCI bus	
0xDC000-0xDFFFF	PCI bus	

0xE0000-0xE3FFF	PCI bus
0xE4000-0xE7FFF	PCI bus
0xDFA00000-0xFEAFFFFF	PCI bus
0xDFA00000-0xFEAFFFFF	Motherboard resources
0xF7E3C000-0xF7E3C00F	Intel(R) Management Engine Interface
0xFED40000-0xFED44FFF	System board
0x2000000-0x201FFFFF	System board
0x40004000-0x40004FFF	System board
0xF7E3A000-0xF7E3AFFF	Intel(R) Active Management Technology - SOL (COM5)
0xFED1C000-0xFED1FFFF	Motherboard resources
0xFED10000-0xFED17FFF	Motherboard resources
0xFED18000-0xFED18FFF	Motherboard resources
0xFED19000-0xFED19FFF	Motherboard resources
0xF8000000-0xFBFFFFFF	Motherboard resources
0xFED20000-0xFED3FFFF	Motherboard resources
0xFED90000-0xFED93FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFF000000-0xFFFFFFF	Motherboard resources
0xFF000000-0xFFFFFFF	Intel(R) 82802 Firmware Hub Device
0xFEE00000-0xFEEFFFF	Motherboard resources
0xF7800000-0xF7BFFFFF	Intel(R) HD Graphics 4000
0xE0000000-0xEFFFFFF	Intel(R) HD Graphics 4000
0xF7E30000-0xF7E33FFF	High Definition Audio Controller
0xF7E00000-0xF7E1FFFF	Intel(R) 82579LM Gigabit Network Connection
0xF7E39000-0xF7E39FFF	Intel(R) 82579LM Gigabit Network Connection
0xF7E35000-0xF7E350FF	Intel(R) 7 Series/C216 Chipset Family SMBus Host Controller - 1E22

Appendix E: Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitoring the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. The WDT will not be reload by an abnormal system, then WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming I/O ports.

Below is an assembly program example for disable and load of WDT.

```
/*---- Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"
/*---- routing, sub-routing -----*/
void main()
{
/*-----*/
                                                     /* initial IO port */
         outportb(0x4e, 0x87);
         outportb(0x4e, 0x87);
                                                   /* twice, */
                                                 /* point to logical device */
/* select logical device 7 */
         outportb(0x4e, 0x07);
outportb(0x4e+1, 0x07);
outportb(0x4e, 0xf5);
                                               /* select logical device / */
/* select offset f5h */
/* select offset f0h */
/* select offset f0h */
/* select offset f6h */
/* select offset f6h */
/* select offset f6h */
         outportb(0x4e+1, 0x40);
outportb(0x4e, 0xf0);
outportb(0x4e+1, 0x81);
outportb(0x4e, 0xf6);
         outportb(0x4e+1, 0x05);
                                                   /* update offset f6h to Oah :10sec
*/
         outportb(0x4e, 0xf5);
                                                   /* select offset f5h */
        outportb(0x4e+1, 0x20);
                                                   /* set bit5 = 1 enable watch dog
time */
         outportb(0x4e, 0xAA);
                                                   /* stop program F71869E, Exit */
/*-----*/
         outportb(0x2e, 0x87);
                                                      /* initial IO port */
                                                   /* twice, */
          outportb(0x2e, 0x87);
                                                 /* point to logical device */
/* select logical device 7 */
/* select offset f5h */
/* set bits
         outportb(0x2e, 0x07);
         outportb(0x2e+1, 0x07);
outportb(0x2e, 0xf5);
                                                   /* set bit5 = 1 to clear bit5 */
         outportb(0x2e+1, 0x40);
                                                   /* select offset f0h */
         outportb(0x2e+1, 0x81);
outportb(0x2e. 0xfe);
                                                  /* set bit7 =1 to enable WDTRST# */
                                                   /* select offset f6h */
```

```
outportb(0x2e+1, 0x05); /* update offset f6h to 0ah :10sec
*/
outportb(0x2e, 0xf5); /* select offset f5h */
outportb(0x2e+1, 0x20); /* set bit5 = 1 enable watch dog
time */
outportb(0x2e, 0xAA); /* stop program F71869E, Exit */
}
```

Appendix F: Digital I/O Setting

Below are the source codes written in C, please take them for Digital I/O application examples. The default I/O address is 6Eh.

```
C Language Code
//-----
            -----
#include "DigitalIO.h"
#define DELAY_TIME
                    10
/* Variable
               * /
int SMB PORT AD = 0 \times 0400;
                          // SM bus Add = 0400h
int SMB DIO ADD = 0x6e;
                   // Fintek F75111 Add = 6eh
bool bWinIoInitOK;
//-----
/* Function
               */
unsigned char SMB Byte READ(int SMPORT, int DeviceID, int iREG INDEX);
void SMB Byte WRITE(int SMPORT, int DeviceID, int oREG INDEX, int oREG DATA);
void GPIO Control(void);
//-----
            _____
#pragma argsused
```

```
BOOL WINAPI DllMain(HINSTANCE hinstDLL, DWORD fwdreason, LPVOID lpvReserved)
ł
      bWinIoInitOK = InitializeWinIo();
     return 1;
//-----
void export stdcall DIO Open()
{
     GPIO Control();
//-----
void export stdcall DIO Close()
{
      if(bWinIoInitOK)
      {
            ShutdownWinIo();
      }
//-----
unsigned char SMB Byte READ(int SMPORT, int DeviceID, int iREG INDEX)
{
      DWORD iData;
      SetPortVal(SMPORT+02,0x00,1);
      SetPortVal(SMPORT+00,0xff,1);
      Sleep(DELAY TIME);
      SetPortVal(SMPORT+04, DeviceID+1, 1);
      SetPortVal(SMPORT+03, iREG INDEX, 1);
      SetPortVal(SMPORT+02,0x48,1);
      Sleep(DELAY TIME);
      GetPortVal(SMPORT+05,&iData,1);
      return iData;
//-----
void SMB Byte WRITE(int SMPORT, int DeviceID, int oREG INDEX, int oREG DATA)
{
      SetPortVal(SMPORT+02,0x00,1);
      SetPortVal(SMPORT+00,0xff,1);
      Sleep(DELAY TIME);
      SetPortVal(SMPORT+04, DeviceID, 1);
      SetPortVal(SMPORT+03, oREG INDEX, 1);
      SetPortVal(SMPORT+05, oREG DATA, 1);
      SetPortVal(SMPORT+02,0x48,1);
      Sleep(DELAY TIME);
//-----
void GPIO Control(void)
{
```

```
/* GPIO10~17 Output pin control */
       SMB Byte WRITE(SMB PORT AD, SMB DIO ADD, 0x10, 0xff);
       Sleep(DELAY TIME);
       /* GPIO20~27 Input pin control */
       SMB Byte WRITE(SMB PORT AD, SMB DIO ADD, 0x20, 0x00);
       Sleep(DELAY TIME);
       /* GPI030~33 Output pin control */
       SMB Byte WRITE(SMB PORT AD, SMB DI0 ADD, 0x40, 0xff);
       Sleep(DELAY TIME);
//-----
void export stdcall DIO Out(int iData)
{
      int iTemp;
      // GPIP1X Output
       SMB Byte WRITE (SMB PORT AD, SMB DIO ADD, 0x11, iData);
       // GPIP3X Output
      iTemp = ( iData & 0x04 ) >> 2;
       SMB Byte WRITE(SMB PORT AD, SMB DI0 ADD, 0x41, iTemp);
//-----
int __export __stdcall DIO_In()
{
      DWORD iData;
      // GPIP2X Input
       iData = SMB Byte READ(SMB PORT AD, SMB DI0 ADD, 0x22);
       iData = SMB Byte READ(SMB PORT AD, SMB DIO ADD, 0x22);
       iData = SMB_Byte_READ(SMB_PORT_AD, SMB_DI0_ADD, 0x22);
      return iData;
               _____
//----
```

Pin	Description	Chipset Pin#	Chipset Pin Description
1	DIO0	10	GPIO10
2	DIO1	11	GPIO11
3	DIO2	12	GPIO12
4	DIO3	3	GPIO13
5	DIO4	9	GPIO14
6	DIO5	19	GPIO15
7	DIO6	4	GPIO16
8	DIO7	5	GPIO17
9	DIO8	6	GPIO20
10	DIO9	7	GPIO21
11	DIO10	8	GPIO22
12	DIO11	24	GPIO23
13	DIO12	23	GPIO24
14	DIO13	22	GPIO25
15	DIO14	21	GPIO26
16	DIO15	20	GPIO27

Digital IO Usage Table (Super IO Chipset F75111)