ITX-i77M0

Mini-ITX Industrial Motherboard

User's Manual

Version 1.0

2014.05

Revision History

Version	Date	Description
1.0	2013/05/17	initial release
1.1	2014/05/07	Revise P.15 LVDS1 Pin definition.

Table of Contents

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Chapter 1

Introduction

1.1 Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

1.2 Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

Warning
This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain

unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

1.3 About This User's Manual

This user's manual provides general information and installation instructions about the product. This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. please consult your vendor before further handling.

1.4 Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.

2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.

3. Use a grounded wrist strap when handling computer components.

4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

1.5 Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

1.6 Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor.com.tw

E-mail: info@arbor.com.tw

1.7 Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

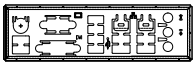
Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

1.8 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

1 x ITX-i77M0 Mini-ITX industrial motherboard

1 x Driver CD
1 x Quick Installation Guide



1 x I/O Bracket

If any of the above items is damaged or missing, contact your vendor immediately.

1.9 Ordering Information

ITX-i77M0	Intel® Ivy Bridge rPGA988 socket Core™ i7/i5/i3, Celeron® embedded Mini-ITX motherboard
CPF-67M0-C1	CPU Cooler Fan for rPGA988 CPU
CBK-11-67M0-00	Cable kit 2 x Two ports COM cables 1 x COM Flat cable 1 x USB cable 2 x SATA cables 1 x SATA Power cable

1.10 Recommended CPU List

Intel® 3rd Generation
i7-3610QE 2.3GHz Core™ Processor
i5-3610ME 2.7GHz Core™ Processor
i3-3120ME 2.4GHz Core™ Processor
Intel® 2nd Generation
i7-2710QE 2.1GHz Core™ Processor
i5-2510E 2.5GHz Core™ Processor
i3-2330E 2.2GHz Core™ Processor
B810 1.6GHz Celeron® Processor

1.11 Specifications

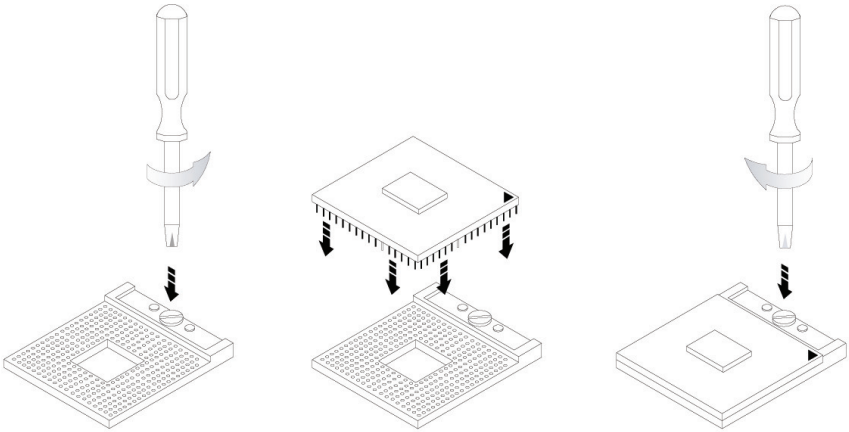
System	
CPU	Support 3rd Generation Intel® Core™ i7/i5/i3 processors in rPGA988 (Socket G2)
Memory	2 x 204-pin DDR3 DIMM Sockets, supporting 1333/1600MHz SDRAM up to 16GB
Chipset	Intel® QM77
BIOS	AMI BIOS
Watchdog Timer	1~255 levels reset
I/O	
I/O Chip	Fintek F71869ED + Fintek F81216AD
Serial Port	5 x RS-232 ports
	1 x RS-232/422/485 selectable port w/ auto-flow control
USB Port	4 x USB 3.0/2.0 compatible ports
	8 x USB 2.0 ports
KB/MS	1 x 6-pin wafer connector for PS/2 keyboard and mouse
Digital I/O	1 x 16-bit programmable Digital Input/Output
Expansion Bus	1 x PCIe x16 slot
	1 x Mini-card slot
Storage	2 x Serial ATA ports with 600MB/s HDD transfer rate
	4 x Serial ATA ports with 300MB/s HDD transfer rate
Ethernet Chipset	1 x Intel® 82579LM PCIe GbE PHY w/ iAMT
	1 x Intel® 82583V PCIe GbE controller
Audio Interface	Realtek ALC886 HD Audio Codec, Mic-in/Line-in/ Line-out
Display	
Graphics Chipset	Integrated Intel HD Graphics 2500 or HD Graphics 4000

Graphics Interface	1 x DVI-I connector, supporting either Analog RGB or DVI, resolution up to 2048 x 1536 for Analog RGB and 1920 x 1200 for TMDS
	Support Dual Channel 24-bit LVDS up to 1600 x 1200 resolution
Mechanical & Environmental	
Power Requirement	DC12V input only
Power Consumption	4.3A@+12V with i7-3610QE (Typical)
Operating Temp.	-20 ~ 70°C (-4 ~ 158°F)
Operating Humidity	0 ~ 95% (non-condensing)
Dimensions (L x W)	170 x 170 mm (6.7" x 6.7")

1.12 Installing the CPU

The processor socket comes with a screw to secure the CPU. As shown in the picture bellow, loose the screw first before inserting the CPU.

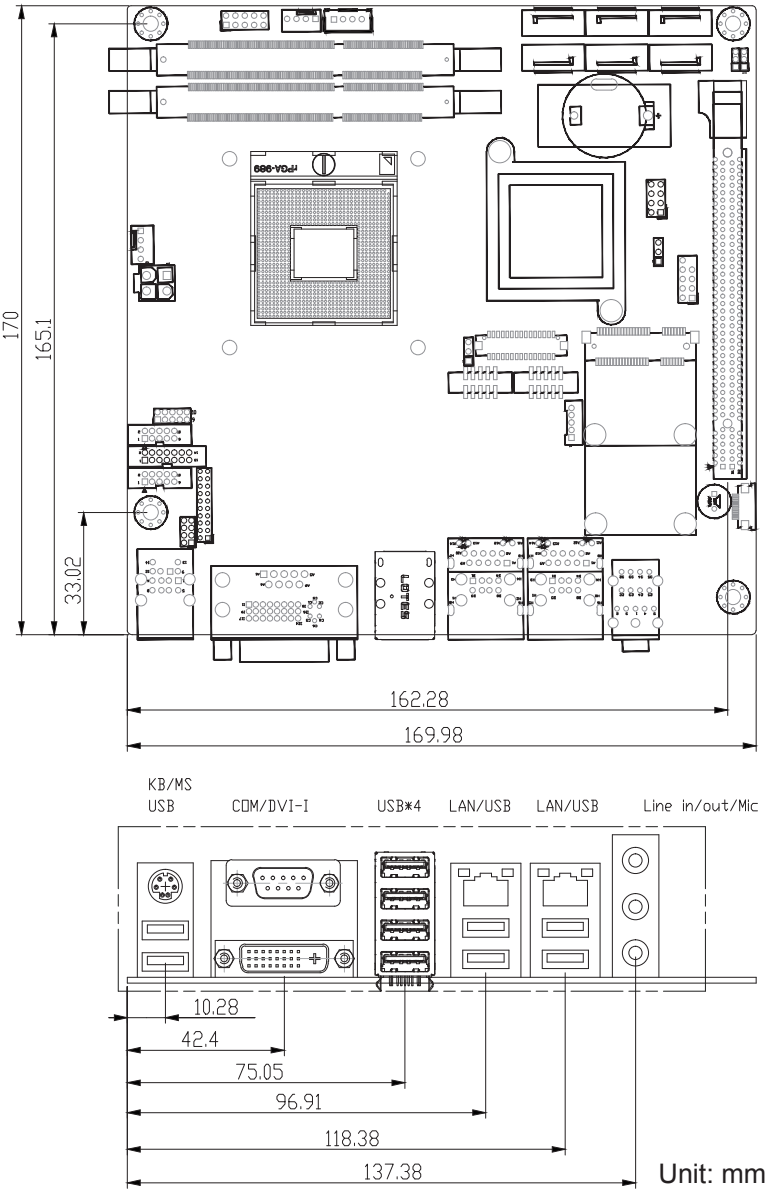
Place the CPU into the socket by making sure the notch on the corner of the CPU correspond to the notch on the inside of the socket. Once the CPU slides into the socket, lock the screw.



Make sure that heatsink is in complete contact with top surface of the CPU to avoid the CPU's overheating problem.

If not, it would cause your system or CPU to be hanged, unstable, damaged.

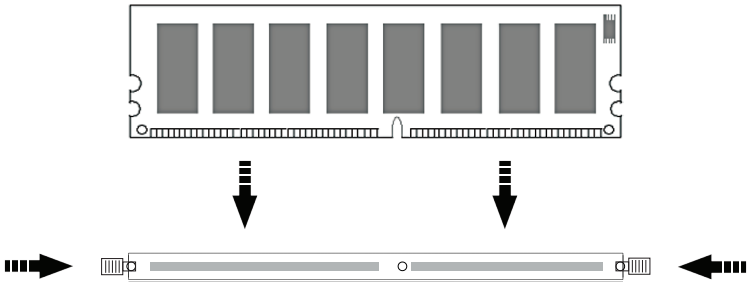
1.13 Board Dimensions



1.14 Installing the Memory

To install the memory module:

1. Find the memory DIMM socket on the board.
   The DIMM socket has a slot connector with a off-center break and two spring-loaded latches on both sides to fix the DDR3 memory module in place.
2. Position the memory module's pin side at the SO-DIMM socket, with the memory module's key notch aligning at the SO-DIMM socket's slot connector break.



3. Insert the memory module to the slot connector at an slanted angle. Note to "fully" insert the memory module to avoid improper insertion.
4. Press down the memory module until it auto-clicks in place.

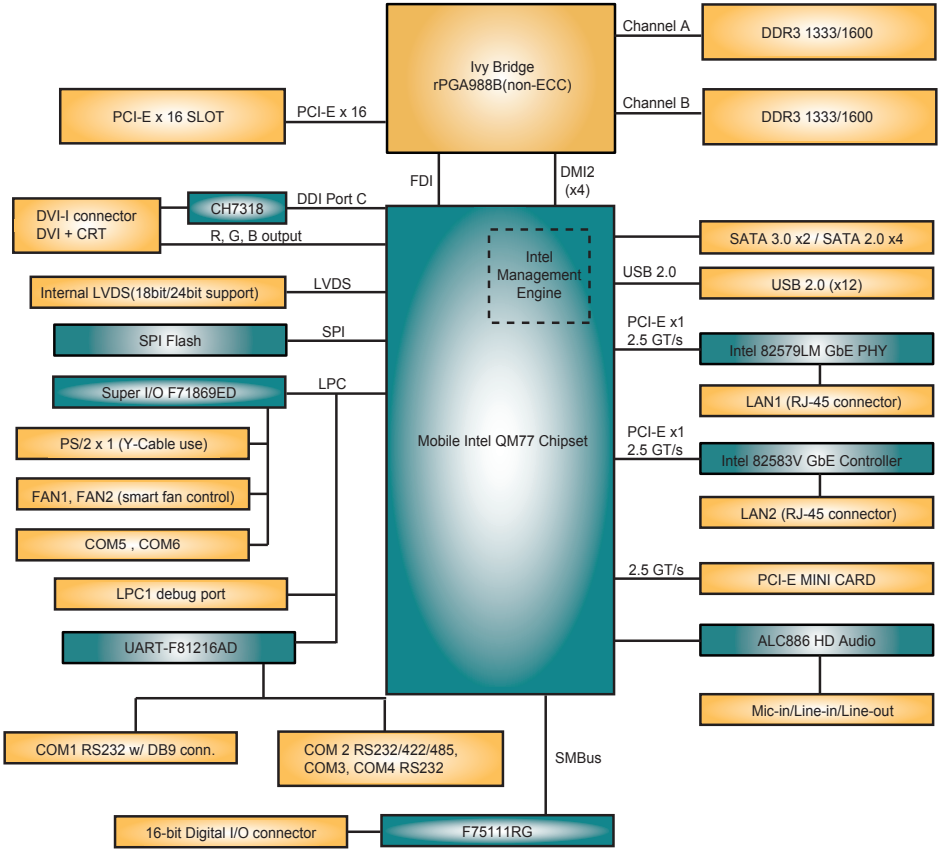
To uninstall the memory module:

1. Pull back the latches from both sides of the SO-DIMM socket.
   The memory module will be auto-released from the socket.
2. Remove the memory module.

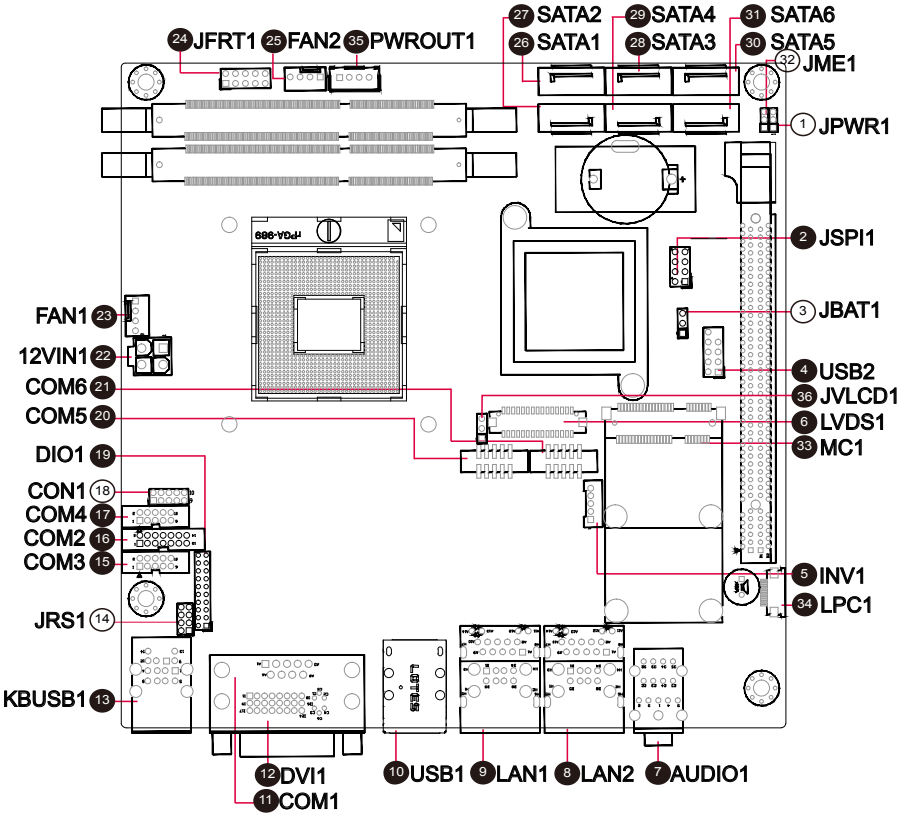
Chapter 2

Installation

2.1 Block Diagram



2.2 Jumpers and Connectors



Jumpers

Jumper Settings

The jumper is “short” (closed) when the jumper cap is placed on pins. If not, that means the jumper is “open.”


Pin open

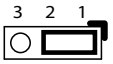
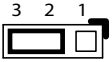

Pin short (closed)

Pin 2-3 short (closed)

Pin 1-2 short (closed)

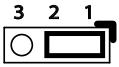
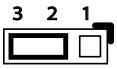
JPWR1: AT/ATX Power Mode Selection (1)

Connector type: 2.00mm pitch 1x3-pin header.

Pin	Power Mode Selection	
1-2	ATX Mode (Default)	
2-3	AT Mode	

JBAT1: Clear CMOS Setting (3)

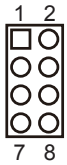
Connector type: 2.00mm pitch 1x3-pin header.

Pin	Mode	
1-2	Keep CMOS data (Default)	
2-3	Clear CMOS data	

JRS1: COM2 RS-232 / 422 / 485 Selection (14)

Connector type: 2.00mm pitch 2x4-pin header.

	Assignment		
Pin	RS-232 (Default)	RS-422	RS-485
1-2	Short	Open	Open
3-4	Open	Short	Open
5-6	Open	Open	Short
7-8 **	Short	Short	Open/Short



** 485 Auto-Flow selection, Open: Enable, Short: Disable.

CON1: COM3/4 Power Source Select on Pin 9 (18)

Connector type: 2.00mm pitch 2x5-pin header.
Default setting: Standard

Pin 9 Power Source Special Support	COM3 CON1	COM4 CON1
Standard (RI) (Default)	7-9	8-10
POS: 12V/1A on Pin 9	1-3	2-4
POS: 5V/1A on Pin 9	3-5	4-6

JME1: ME Function Select (32)

Connector type: 2.00mm pitch 1x3-pin header.

Pin	Power Mode Selection	
1-2	ME Enable/ME Flash disable (Default)	
2-3	ME Disable/ME Flash enable	

JVLCD1: LVDS1 Power Voltage Setting (36)

Connector type: 2.54mm pitch 1x3-pin header

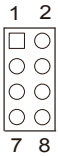
Pin	Power Mode Selection	
1-2	+5V	
2-3	+3.3V (default)	

Connectors

JSPI1: SPI Flash for External SPI Programming Tools (2)

Connector type: 2.54mm pitch 2x4-pin header.

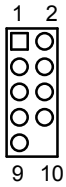
Pin	Desc.	Pin	Desc.
1	V_3P3_SPI	2	GND
3	SPI_CS0_R	4	SPI_CLK_R
5	SPI_SO_R	6	SPI_SI_R
7	NC	8	NC



USB2: USB Port Connector (4)

Connector type: 2.54mm pitch 2x5-pin header.

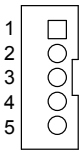
Pin	Description	Pin	Description
1	+5V	2	+5V
3	USBD2-	4	USBD3-
5	USBD2+	6	USBD3+
7	GND	8	GND
9	GND	10	N/C (Key)



INV1: LCD Inverter Connector (5)

Connector type: 2.00mm pitch 1x5 box wafer connector.

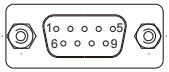
Pin	Description
1	+12V
2	GND
3	Backlight on/off
4	Brightness control
5	GND



COM1: RS-232 Connector (11)

Connector type: D-sub 9-pin male connector.

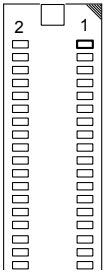
Pin	Desc.	Pin	Desc.
1	DCD	6	DSR
2	RX	7	RTS
3	TX	8	CTS
4	DTR	9	RI
5	GND	10	NC



LVDS1: LVDS Connector (6)

Connector type: DF-13-34DP-1.25V connector.

Pin	Description	Pin	Description
2	VDD	1	VDD
4	TX2CLK+	3	TX1CLK+
6	TX2CLK-	5	TX1CLK-
8	GND	7	GND
10	TX2D0+	9	TX1D0+
12	TX2D0-	11	TX1D0-
14	GND	13	GND
16	TX2D1+	15	TX1D1+
18	TX2D1-	17	TX1D1-
20	GND	19	GND
22	TX2D2+	21	TX1D2+
24	TX2D2-	23	TX1D2-
26	GND	25	GND
28	TX2D3+	27	TX1D3+
30	TX2D3-	29	TX1D3-



AUDIO1: Audio Interface Port (7)

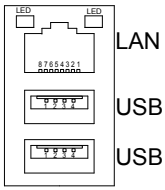
Connector type: triple stacked audio jacks (Stereo ø3.50).

LAN1, 2: Ethernet Connectors (9, 8)

Connector type: RJ-45 + double stacked USB type A connector.
(include USB0/1/2/3 Connector)

LAN (RJ-45)

Pin	Description
1	MDI0+
2	MDI0-
3	MDI1+
4	MDI1-
5	MDI2+
6	MDI2-
7	MDI3+
8	MDI3-



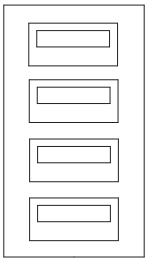
USB (USB type A connector)

Pin	Description
1	+5V
2	USB-
3	USB+
4	GND

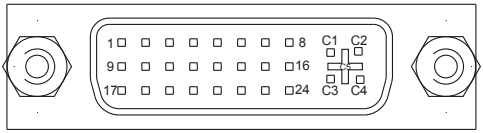
USB1: 4 x USB Port Connector (10)

Connector type: 4-stack USB 3.0/2.0 type A connector.

Pin	Desc.	Pin	Desc.
11	5V	21	5V
12	USBD1-	22	USBD2-
13	USBD1+	23	USBD2+
14	GND1	24	GND3
15	SSRX1-	25	SSRX2-
16	SSRX1+	26	SSRX2+
17	GND2	27	GND4
18	SSTX1-	28	SSTX2-
19	SSTX1+	29	SSTX2+
31	5V	41	5V
32	USBD3-	42	USBD4-
33	USBD3+	43	USBD4+
34	GND5	44	GND7
35	SSRX3-	45	SSRX4-
36	SSRX3+	46	SSRX4+
37	GND6	47	GND8
38	SSTX3-	48	SSTX4-
39	SSTX3+	49	SSTX4+
H1	GND	H4	GND
H2	GND	H5	GND
H3	GND	H6	GND



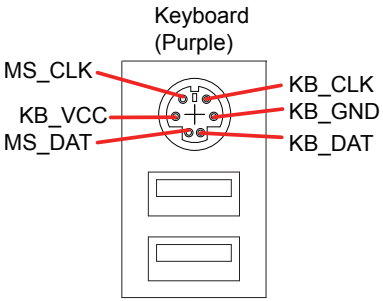
DVI1: DVI-I Connector (12)



Pin	Description	Pin	Description	Pin	Description
1	TX2-	13	N.C.	C1	Analog RED
2	TX2+	14	+5V/50mA	C2	Analog Green
3	TX2/4GND	15	GND	C3	Analog Blue
4	N.C.	16	HTPLG	C4	Analog V_SYNC
5	N.C.	17	TX0-	C5	Analog R, G, B Return
6	DDC_CLK	18	TX0+		
7	DDC_DATA	19	TX0/5GND		
8	CRT_Vsync	20	N.C.		
9	TX1-	21	N.C.		
10	TX1+	22	TXC_GND		
11	TX1/3GND	23	TXC+		
12	N.C.	24	TXC-		

KBUSB1: PS/2 Keyboard and USB x 2 (13)

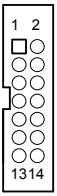
Connector type: PS/2 Keyboard + USB connector.



COM2: Serial Port Connector (16)

Connector type: 2.00mm pitch 2x7-pin box header.

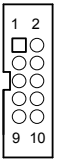
Pin	Desc.	Pin	Desc.
1	DCD2	2	RXD2
3	TXD2	4	DTR2
5	GND	6	DSR2
7	RTS2	8	CTS2
9	RI2	10	NC
11	422TX+_485+	12	422TX-_485-
13	422RX+	14	422RX-



COM3~6: Serial Port Connectors (15, 17, 20, 21)

Connector type: 2.00mm pitch 2x5-pin box header.

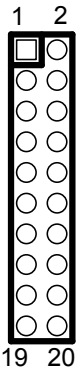
Pin	Desc.	Pin	Desc.
1	DCD1	2	RXD1
3	TXD1	4	DTR1
5	GND	6	DSR1
7	RTS1	8	CTS1
9	RI1	10	NC



DIO1: DIO Port (19)

Connector type: 2.00mm pitch 2x10-pin header.

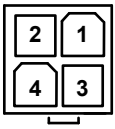
Pin	Desc.	Pin	Desc.
1	DIO0	2	DIO1
3	DIO2	4	DIO3
5	DIO4	6	DIO5
7	DIO6	8	DIO7
9	DIO8	10	DIO9
11	DIO10	12	DIO11
13	DIO12	14	DIO13
15	DIO14	16	DIO15
17	5V	18	GND
19	5V	20	GND



12VIN1: ATX12V Connector (22)

12INV1 supplies the CPU operation ATX +12V (Vcore).

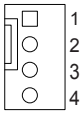
Pin	Description	Pin	Description
2	GND	1	GND
4	+12V	3	+12V



FAN1, 2: Fan Connectors (23, 25)

Connector type: 2.54mm pitch 1x4-pin wafer connector.

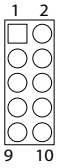
Pin	Description
1	GND
2	+12V
3	FAN_Detect
4	Control



JFRT1: Switches and Indicators (24)

It provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status.
Connector type: 2.54mm pitch 2x5-pin header.

Pin	Description	Pin	Description
1	RESET+	2	RESET-
3	POWER_LED+	4	POWER_LED-
5	HDD_LED+	6	HDD_LED-
7	SPEAKER+	8	SPEAKER-
9	PSON+	10	PSON-



PWROUT1: SATA Power Connector (35)

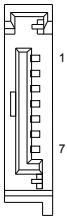
Connector type: 2.50mm pitch 1x4-pin wafer connector.

Pin	Description
1	5V
2	GND
3	GND
4	12V_FAN2

SATA1~6: Serial ATA Connectors (26~31)

High speed transfer rates (150MB/s).

Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND



LPC1: Low Pin Count Connector (34)

Connector type: CVILUX 0.5mm CF20141U0*0-LF connector.

Pin	Desc.	Pin	Desc.
1	LPC_D0	8	LPC_RST#
2	LPC_D1	9	GND
3	LPC_D2	10	LPC_CLK_33Mhz
4	LPC_D3	11	GND
5	GND	12	GND
6	LPC_FRAME#	13	+3.3V
7	SERIRQ	14	+3.3V

MC1: Mini-card Slot (33)

Pin	Desc.	Pin	Desc.
1	Wake	2	+3.3V
3	COEX1	4	GND
5	COEX2	6	+1.5V
7	CLKREQ#	8	UIM_PWR
9	GND	10	UIM_DATA
11	REFCLK-	12	UIM_CLK
13	REFCLK+	14	UIM_RESET
15	GND	16	UIM_VPP
17	UIM_C8/Reserved	18	GND
19	UIM_C4/Reserved	20	W_Disable#
21	GND	22	PERST#
23	PERn0	24	+3.3V
25	PERp0	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3V	40	GND
41	+3.3V	42	LED_WWAN#
43	GND	44	LED_WLAN#
45	Reserved	46	LED_WPAN#
47	Reserved	48	+1.5V
49	Reserved	50	GND
51	Reserved	52	+3.3V

2.3 The Installation Paths of CD Driver

Windows 7

Driver	Path
CHIPSET	\ITX-i77M0\CHIPSET\Win7
ME	\ITX-i77M0\ME\MEI_allOS_8.0.4.1441_PV_5M
GRAPHICS	\ITX-i77M0\GRAPHICS\Win7\Win32
	\ITX-i77M0\GRAPHICS\Win7\Win64
LAN	\ITX-i77M0\ETHERNET\WIN_allos_Ver16.3
AUDIO	\ITX-i77M0\AUDIO\Vista_Win7_R261-32_64 bit
USB3.0	\ITX-i77M0\USB3.0

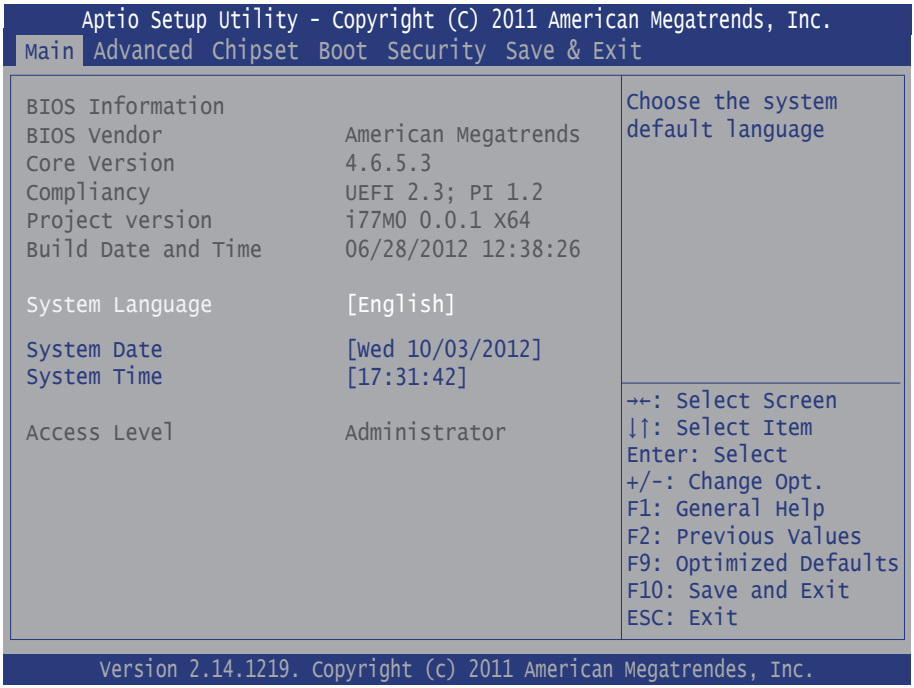
Chapter 3

BIOS

3.1 Main

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS RAM of the system stores the Setup utility and configurations. When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILITY, press **"Delete"** once the power is turned on. When the computer is shut down, the battery on the motherboard supplies the power for BIOS RAM.

The **Main Setup** screen lists the following information:



Setting	Description
BIOS Information	
BIOS Vendor	displays vendor name
Core Version	displays current core version information
Compliancy	displays compliant format
Project Version	displays current BIOS version information
Build Date and Time	the date that the BIOS version was made/updated

System Language	Choose the system default language
System Date	Set the system date. Note that the 'Day' automatically changes when you set the date. ► The date format is: **Day:** Sun to Sat **Month:** 1 to 12 **Date:** 1 to 31 **Year:** 1998 to 2099
System Time	Set the system time. ► The time format is: **Hour:** 00 to 23 **Minute:** 00 to 59 **Second:** 00 to 59

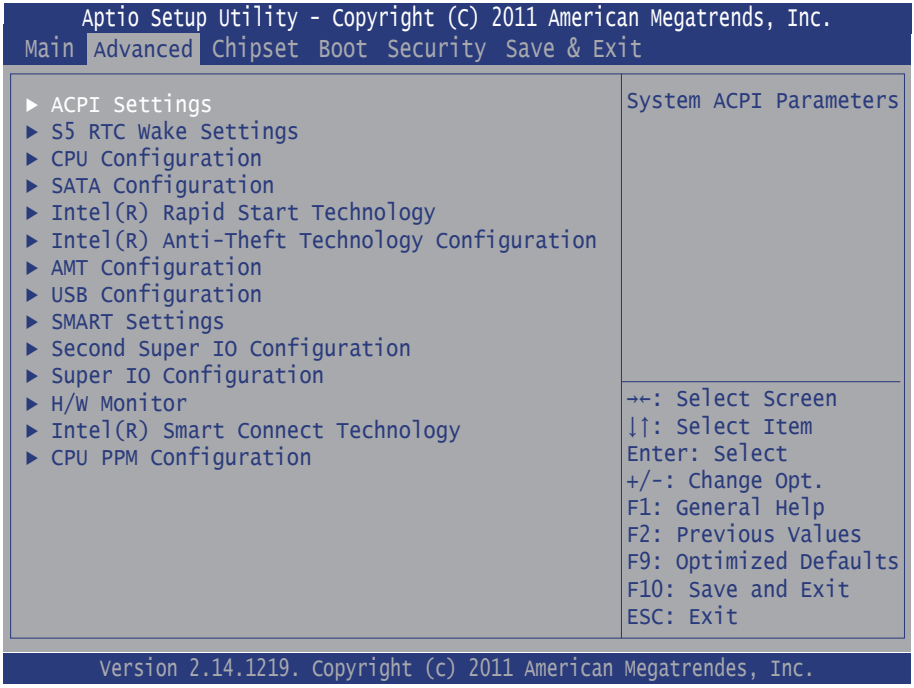
Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

Keystroke	Function
◄ ►	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
▼ ▲	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select "OK" or "Cancel" for exiting and discarding changes. Use "←" and "→" to select and press "Enter" to confirm) On the Sub Menu – Exit current page and return to main menu
Page Up / +	Increase the numeric value on a selected setup item / make change
Page Down -	Decrease the numeric value on a selected setup item / make change
F1	Activate "General Help" screen
F10	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select "OK" or "Cancel" for exiting and saving changes. Use "←" and "→" to select and press "Enter" to confirm)

3.2 Advanced

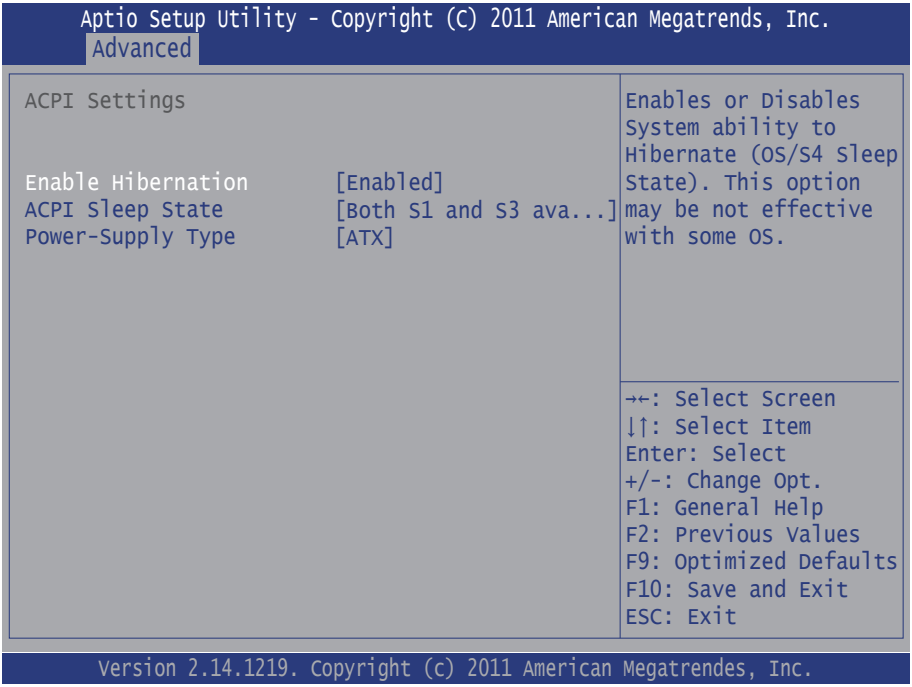
The “Advanced” setting page provides you the options to configure the details of your hardware, such as ACPI, CPU, SATA, AMT, USB and (Second) Super IO.



Setting	Description
ACPI Settings	See Section 3.2.1
S5 RTC Wake Settings	See Section 3.2.2
CPU Configuration	See Section 3.2.3
SATA Configuration	See Section 3.2.4
Intel(R) Rapid Start Technology	See Section 3.2.5
Intel(R) Anti-Theft Technology Configuration	See Section 3.2.6
AMT Configuration	See Section 3.2.7
USB Configuration	See Section 3.2.8
SMART Settings	See Section 3.2.9

Second Super IO Configuration	See Section 3.2.10
Super IO Configuration	See Section 3.2.11
H/W Monitor	See Section 3.2.12
Intel(R) Smart Connect Technology	See Section 3.2.13
CPU PPM Configuration	See Section 3.2.14

3.2.1 ACPI Settings

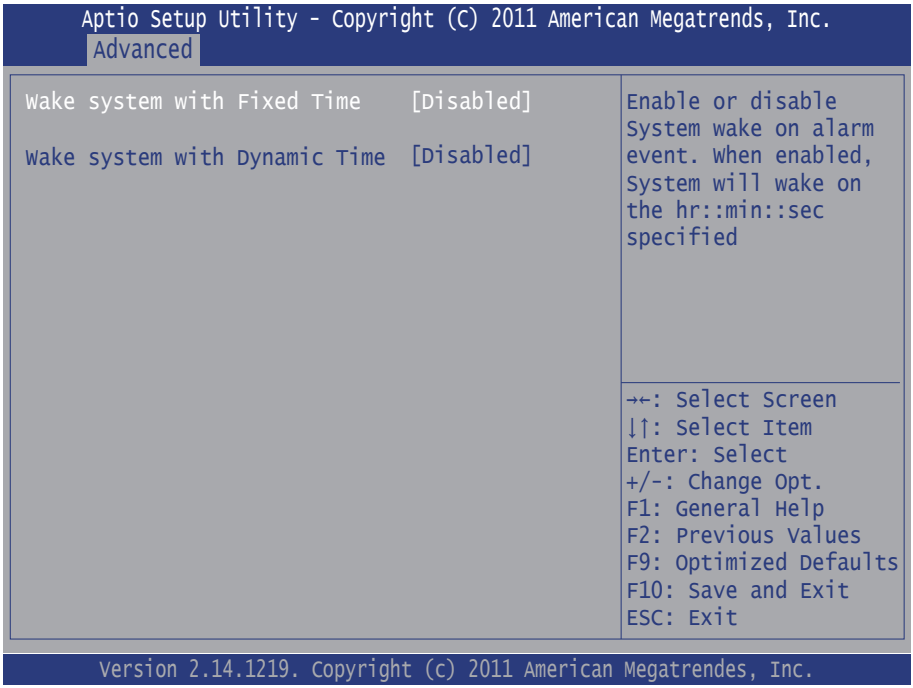


Setting	Description
Enable Hibernation	**Enable** (default) or **Disable** system ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State	Select ACPI sleep state the system will enter when the SUSPEND button is pressed. ► Options: **Suspend Disabled**, **S1 only(CPU Stop Clock)**, **S3 only(Suspend to RAM)**, **Both S1 and S3 available for OS to choose from** (default).
Power-Supply Type	Select Power-Supply Type. ► Options: **AT**, **ATX** (default).

3.2.2 S5 RTC Wake Settings

Enable system to wake from S5 using RTC alarm.



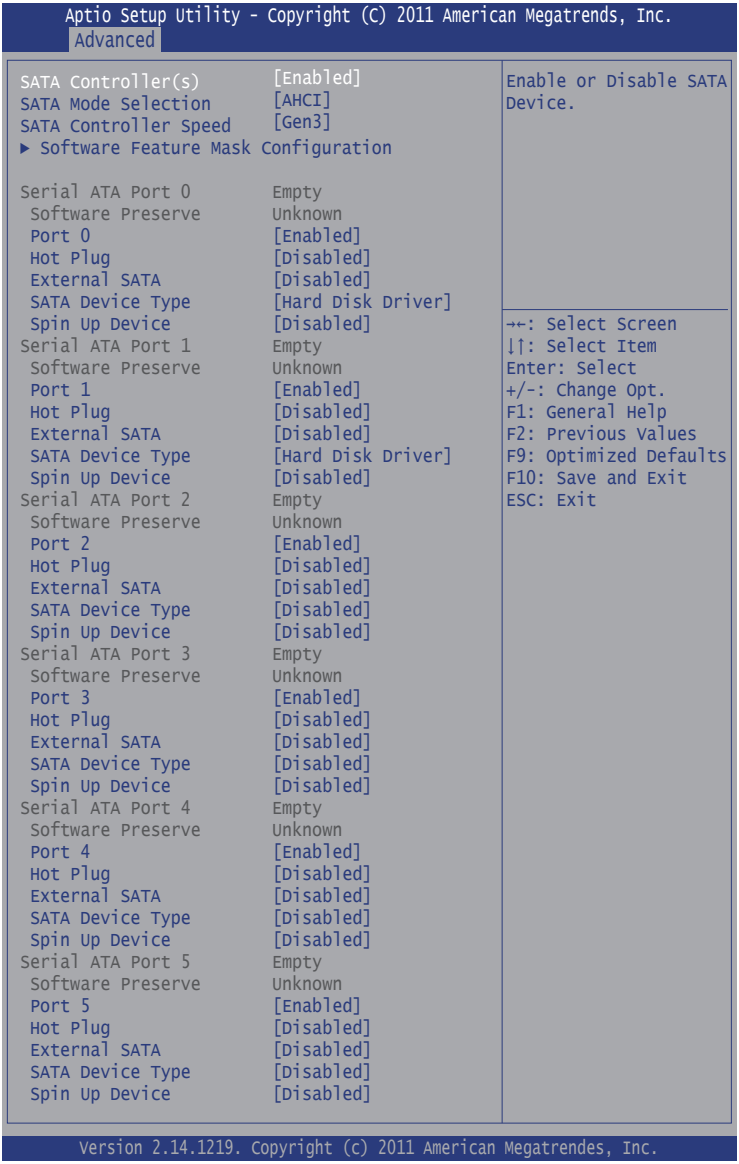
Setting	Description
Wake system with Fixed Time	**Enable** or **Disable** (default) System wake on alarm event. When enabled, System will wake on the hr::min::sec specified.

Wake system with Dynamic Time	**Enable** or **Disable** (default) System wake on alarm event. When enabled, System will wake on the current time + Increase minute(s).

3.2.3 CPU Configuration

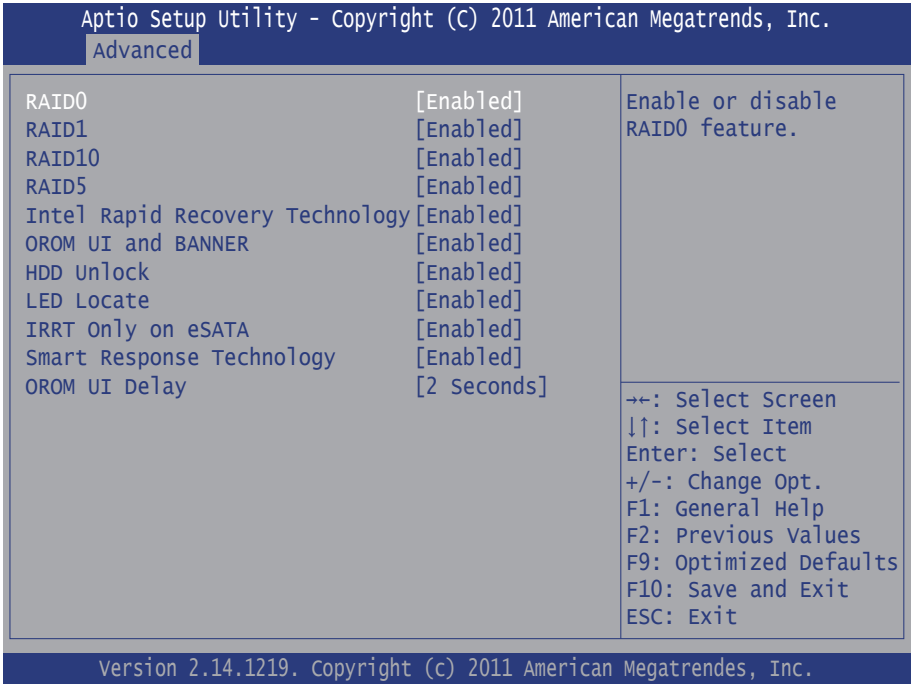
Setting	Description
Hyper-threading	**Enabled** (default) for Windows XP and Linux (OS optimized for Hyper-threading Technology) and **Disabled** for other OS (OS not optimized for Hyper-threading Technology). When Disabled, only one thread per enabled core is enabled.
Active Processor Cores	Number of cores to enable in each processor package. ► Options: **All** (default), **1**, **2**, **3**
Limit CPUID Maximum	Disabled for Windows XP ► Options: **Enabled** and **Disabled** (default).
Execute Disable Bit	XP can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.) ► Options: **Enabled** (default) and **Disabled**.
Intel Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. ► Options: **Enabled** and **Disabled** (default).
Hardware Prefetcher	To turn on/off the Mid Level Cache (L2) streamer prefetcher. ► Options: **Enabled** (default) and **Disabled**.
Adjacent Cache Line Prefetch	To turn on/off prefetching of adjacent cache lines. ► Options: **Enabled** (default) and **Disabled**.

3.2.4 SATA Configuration



Setting	Description
SATA Controller(s)	**Enable** (default) or **Disable** SATA Device.
SATA Mode Selection	Determine how SATA controller(s) operate. ► Options: **IDE**, **AHCI** (default) and **RAID**.
SATA Controller Speed	Indicates the maximum speed the SATA controller can support. ► Options: **Gen1**, **Gen2**, **Gen3** (default)
Software Feature Mask Configuration	See Software Feature Mask Configuration tab
Port 0~5	**Enable** (default) or **Disable** SATA Port.
Hot Plug	Designates this port as Hot Pluggable. ► Options: **Enabled** and **Disabled** (default).
External SATA	External SATA Support. ► Options: **Enabled** and **Disabled** (default).
SATA Device Type	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive. ► Options: **Hard Disk Driver** (default) and **Solid State Drive**.
Spin Up Device	On an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to the device. ► Options: **Enabled** and **Disabled** (default).

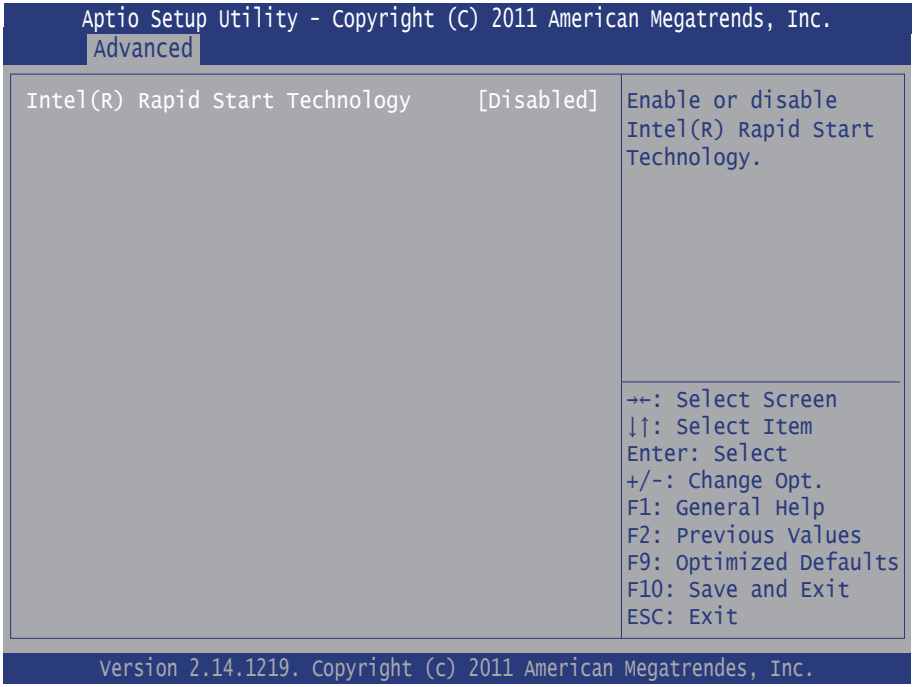
Software Feature Mask Configuration



Setting	Description
RAID0/1/10/5	**Enable** (default) or **Disable** RAID0/1/10/5 feature.
Intel Rapid Recovery Technology	**Enable** (default) or **Disable** Intel Rapid Recovery Technology.
OROM UI and BANNER	If enabled, then the OROM UI is shown. Otherwise, no OROM banner or information will be displayed if all disks and RAID volumes are Normal. ► Options: **Enabled** (default) and **Disabled**.
HDD Unlock	If enabled, indicates that the HDD password unlock in the OS is enabled. ► Options: **Enabled** (default) and **Disabled**.

LED Locate	If enabled, indicates that the LED/SGPIO hardware is attached and ping to locate feature is enabled on the OS. ► Options: **Enabled** (default) and **Disabled**.
IRRT Only on eSATA	If **enabled** (default), then only IRRT volumes can span internal and eSATA drives. If **disabled**, then any RAID volume can span internal and eSATA drives.
Smart Response Technology	**Enable** (default) or **Disable** Smart Response Technology.
OROM UI Delay	If enabled, indicates the delay of the OROM UI Splash Screen in a normal status. ► Options: **2** (default) **/4/6/8 Seconds**

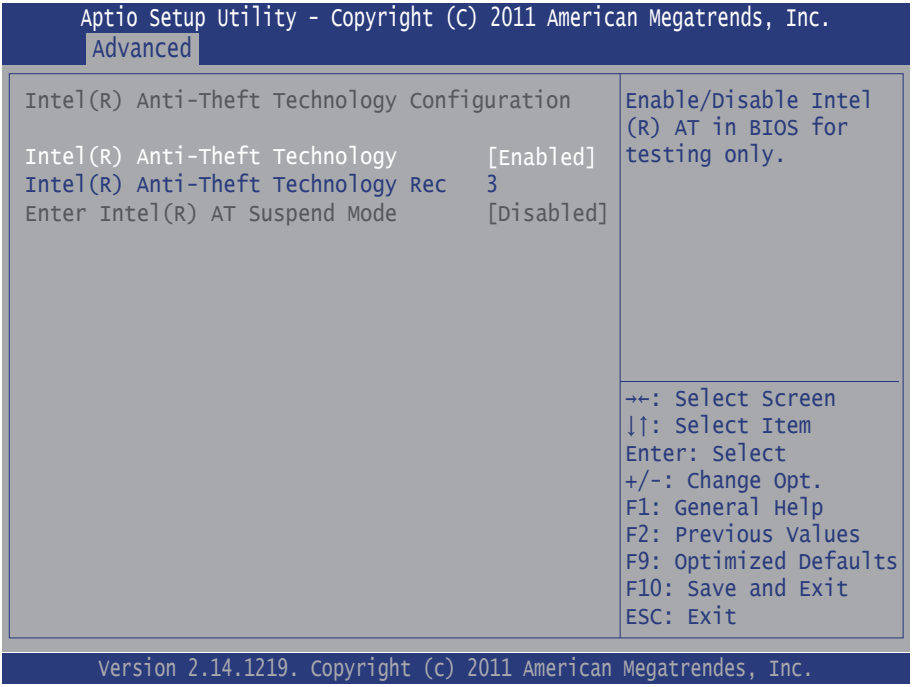
3.2.5 Intel(R) Rapid Start Technology



Setting	Description
Intel(R) Rapid Start Technology	**Enable** or **Disable** (default) Intel(R) Rapid Start Technology.

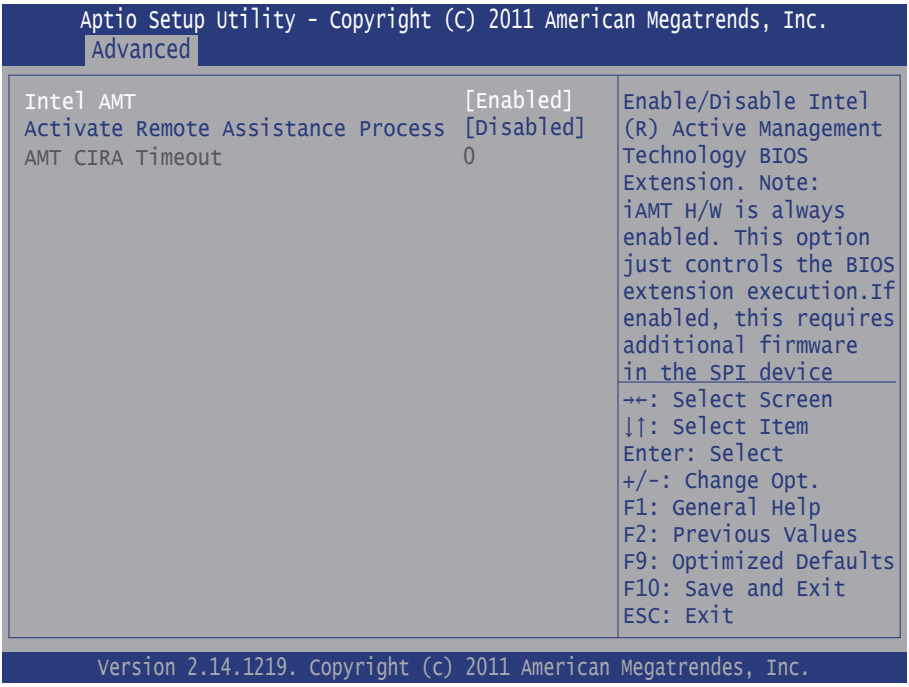
3.2.6 Intel(R) Anti-Theft Technology Configuration

Disabling Intel(R) AT allows User to login to platform. This is strictly for testing only. This does not disable Intel(R) AT Services in ME.



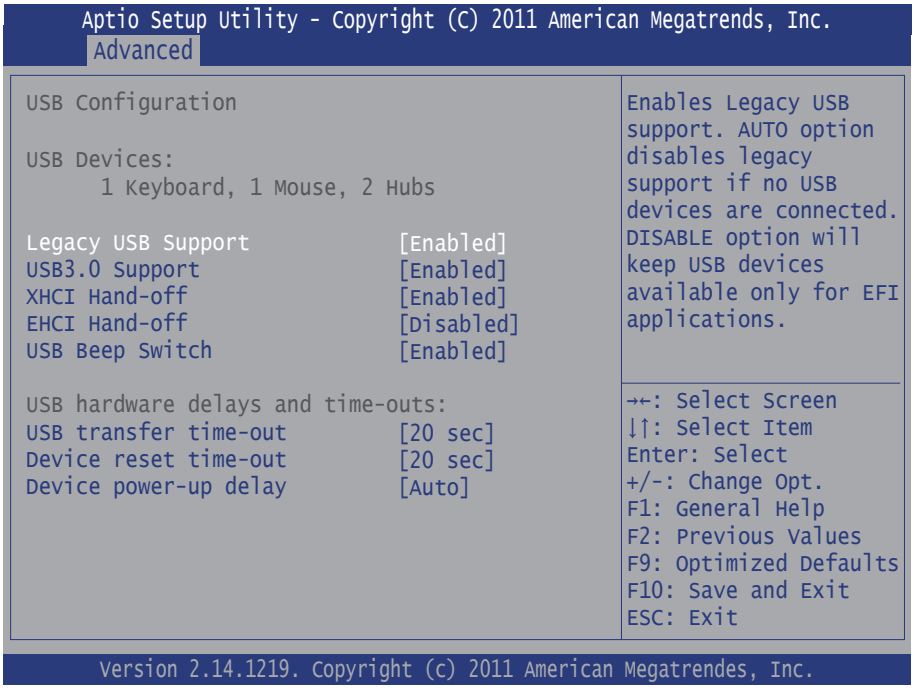
Setting	Description
Intel(R) Anti-Theft Technology	**Enable** or **Disable** (default) Intel(R) AT in BIOS for testing only.
Intel(R) Anti-Theft Technology Rec	Set the number of times Recovery attempted will be allowed.

3.2.7 AMT Configuration



Setting	Description
Intel AMT	**Enable** (default) or **Disable** Intel (R) Active Management Technology BIOS Extension. Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device
Activate Remote Assistance Process	Trigger CIRA boot. ► Options: **Enabled** and **Disabled** (default).

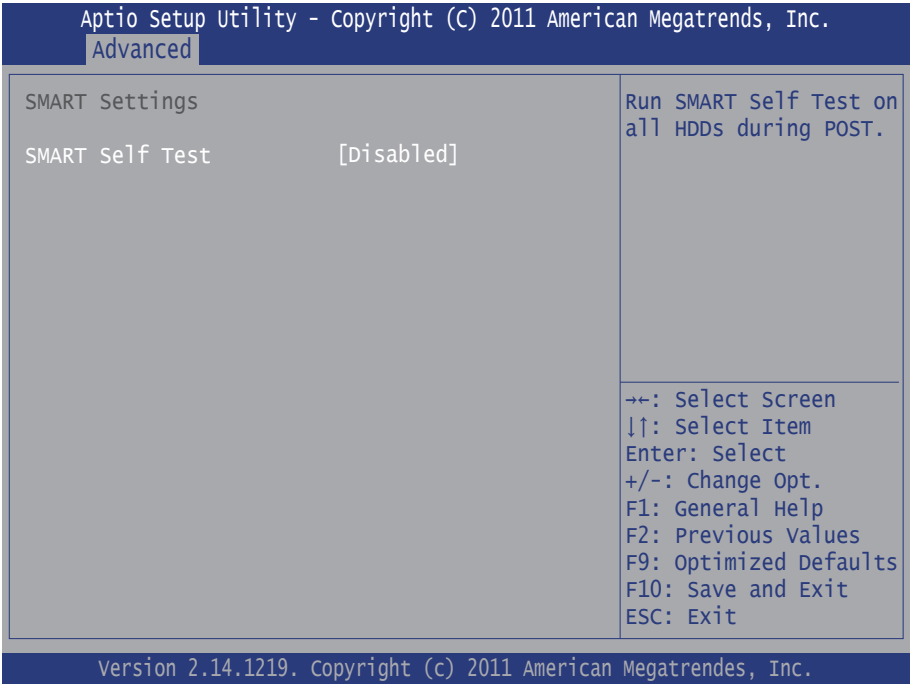
3.2.8 USB Configuration



Setting	Description
USB Devices:	
Legacy USB Support	**Enables** (default) Legacy USB support. **AUTO** option disables legacy support if no USB devices are connected. **DISABLE** option will keep USB devices available only for EFI applications.
USB3.0 Support	**Enable** (default) or **Disable** USB3.0 (XHCI) Controller support.
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver. ► Options: **Enabled** (default) and **Disabled**.

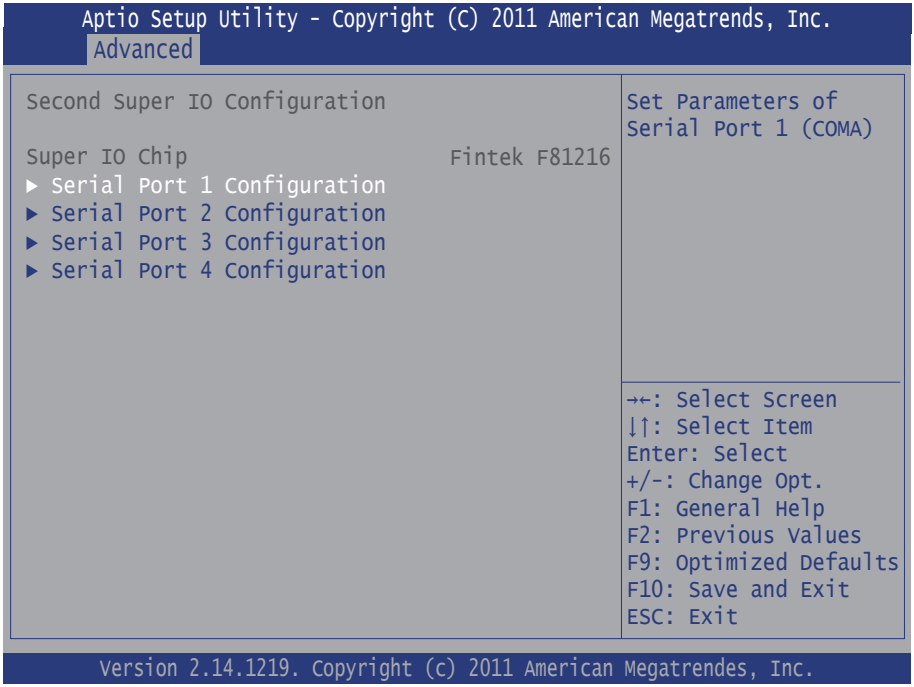
EHCI Hand-off	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver. ► Options: **Enabled** and **Disabled** (default).
USB Beep Switch	**Enable** (default) or **Disable** USB Beep sound.
USB hardware delays and time-outs:	
USB transfer time-out	The time-out value for Control, Bulk, and Interrupt transfers. ► Options: **1/5/10/20 sec** (default)
Device reset time-out	USB mass storage device Start Unit command time-out. ► Options: **10/20** (default)**/30/40 sec**
Device power-up delay	Maximum time the device will take before it properly reports itself to the host controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from hub descriptor. ► Options: **Auto** (default) and **Manual**

3.2.9 SMART Settings

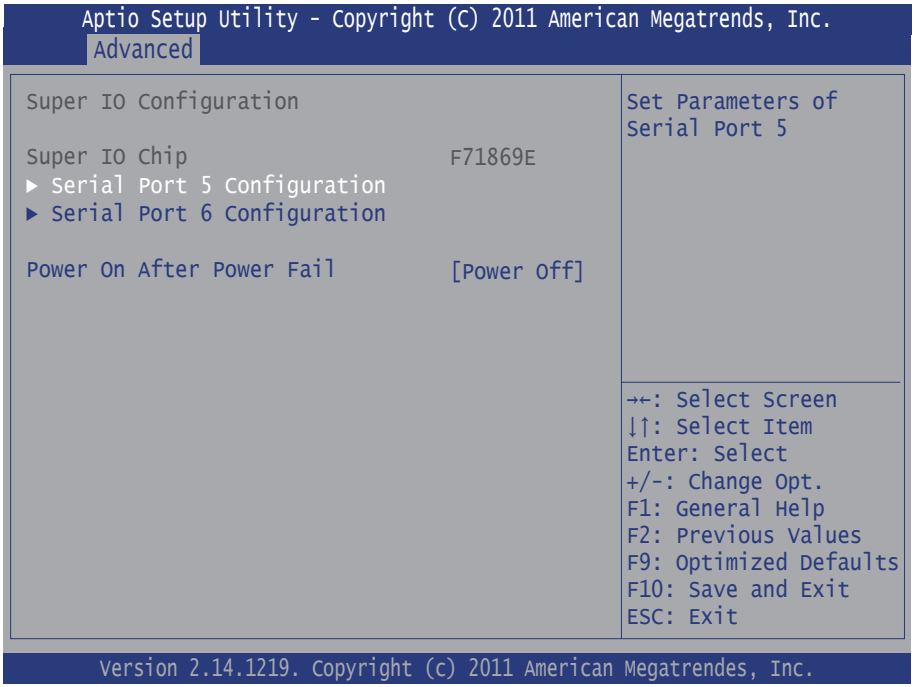


Setting	Description
SMART Self Test	Run SMART Self Test on all HDDs during POST. ► Options: **Enabled** and **Disabled** (default).

3.2.10 Second Super IO Configuration

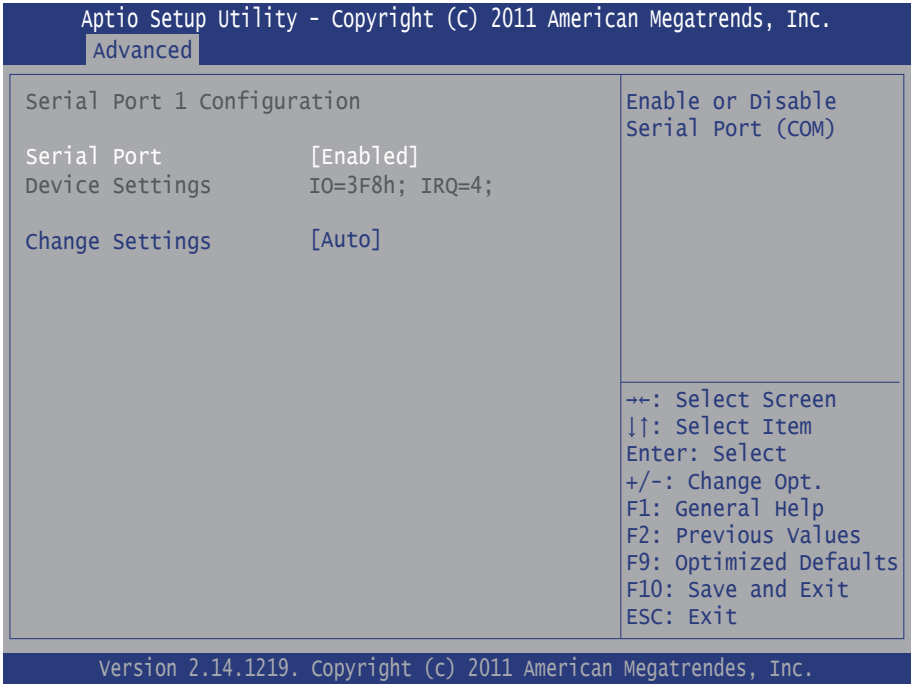


3.2.11 Super IO Configuration



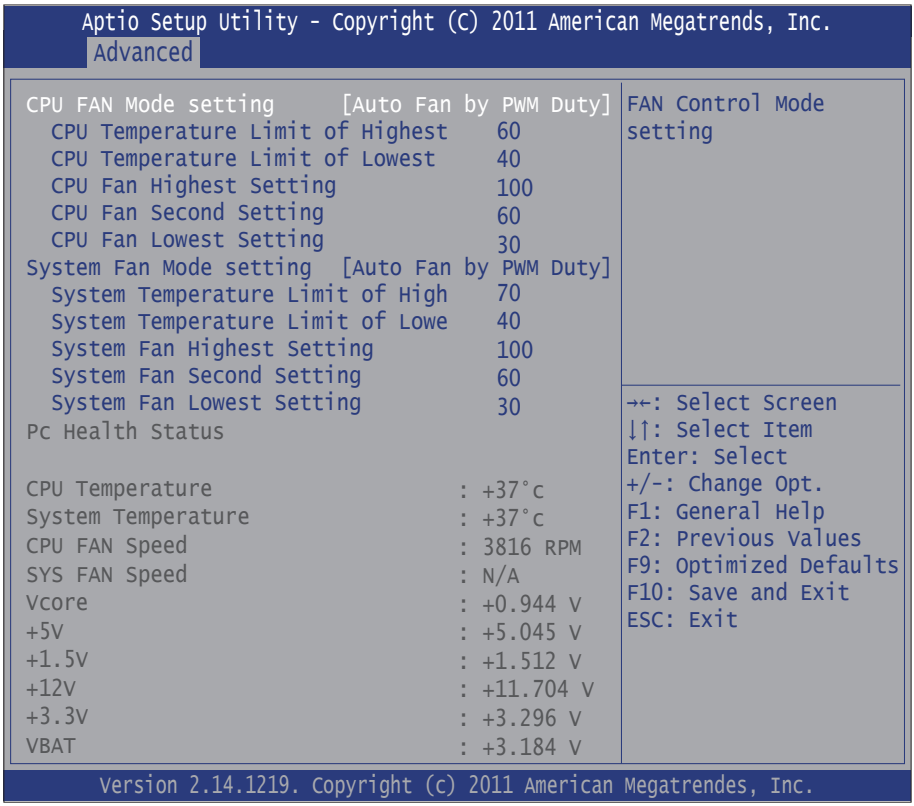
Setting	Description
Power On After Power Fail	Specify what state to go to when power is re-applied after a power failure. ► Options: **Power Off** (default) and **Power On**

Serial Port 1~6 Configuration



Setting	Description
Serial Port	**Enable** (default) or **Disable** Serial Port (COM)
Change Settings	Select an optimal setting for Super IO device.

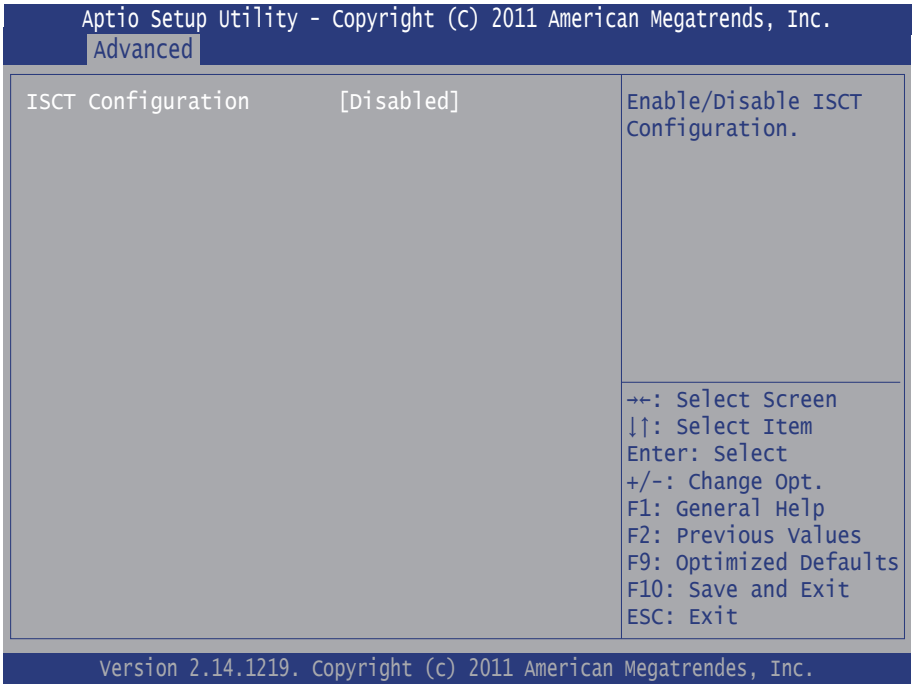
3.2.12 H/W Monitor



Setting	Description
CPU/System FAN Mode setting	Fan Control Mode Setting ► Options: **Manual Duty Mode** and **Auto Fan by PWM Duty** (default).
CPU/System Temperature Limit of Highest	Highest Temperature Setting. Min=0 Max=127 Please input Dec number:
CPU/System Temperature Limit of Lowest	Lowest Temperature Setting. Min=0 Max=127 Please input Dec number:
CPU/System Fan Highest Setting	Highest Speed Value Min=0 Max=100 Please input Dec number:

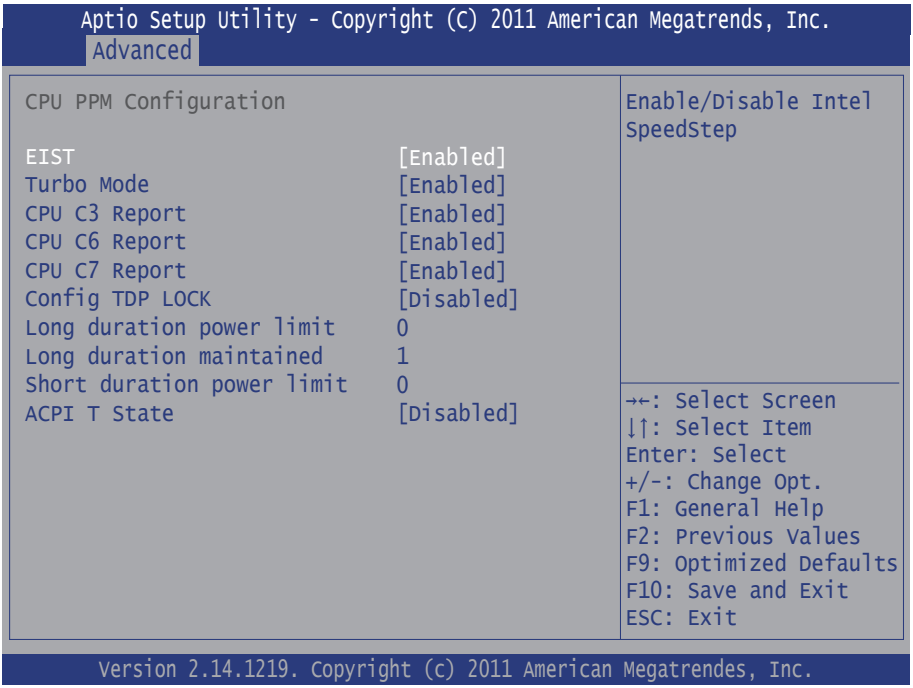
CPU/System Fan Second Setting	Second Speed Value Min=0 Max=100 Please input Dec number:
CPU/System Fan Lowest Setting	Lowest Speed Value Min=0 Max=100 Please input Dec number:

3.2.13 Intel(R) Smart Connect Technology



Setting	Description
ISCT Configuration	**Enable** or **Disable** (default) ISCT Configuration

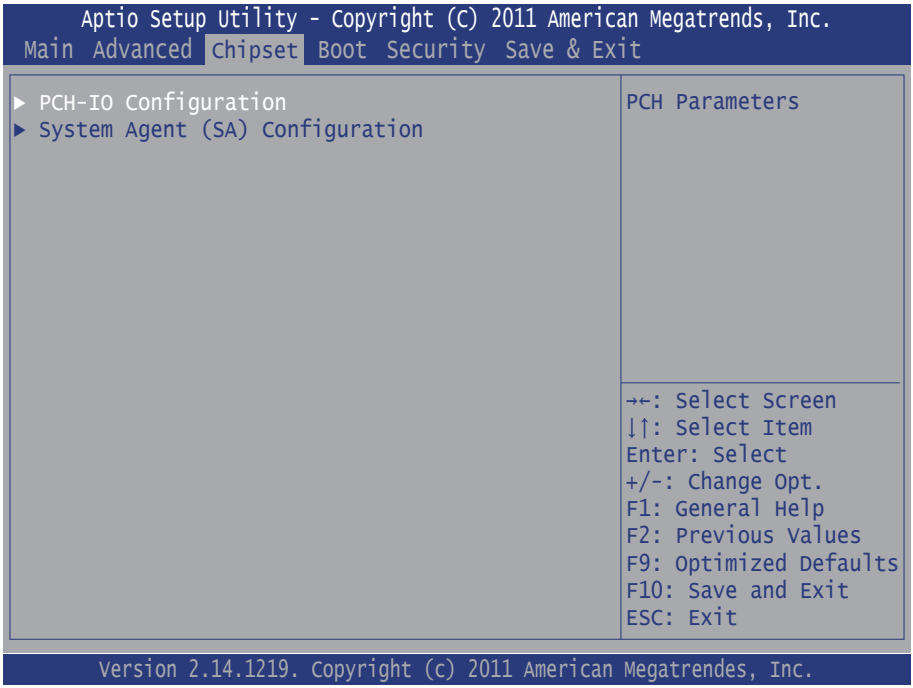
3.2.14 CPU PPM Configuration



Setting	Description
EIST	**Enable** (default) or **Disable** Intel SpeedStep
Turbo Mode	**Enable** (default) or **Disable** Turbo Mode
CPU C3 Report	**Enable** (default) or **Disable** CPU C3(ACPI C2) report to OS
CPU C6 Report	**Enable** (default) or **Disable** CPU C6(ACPI C3) report to OS
CPU C7 Report	**Enable** (default) or **Disable** CPU C7(ACPI C3) report to OS
Config TDP LOCK	Lock the Config TDP Control register ► Options: **Enabled** and **Disabled** (default)
Long duration power limit	Long duration power limit in Watts, 0 means use factory default.

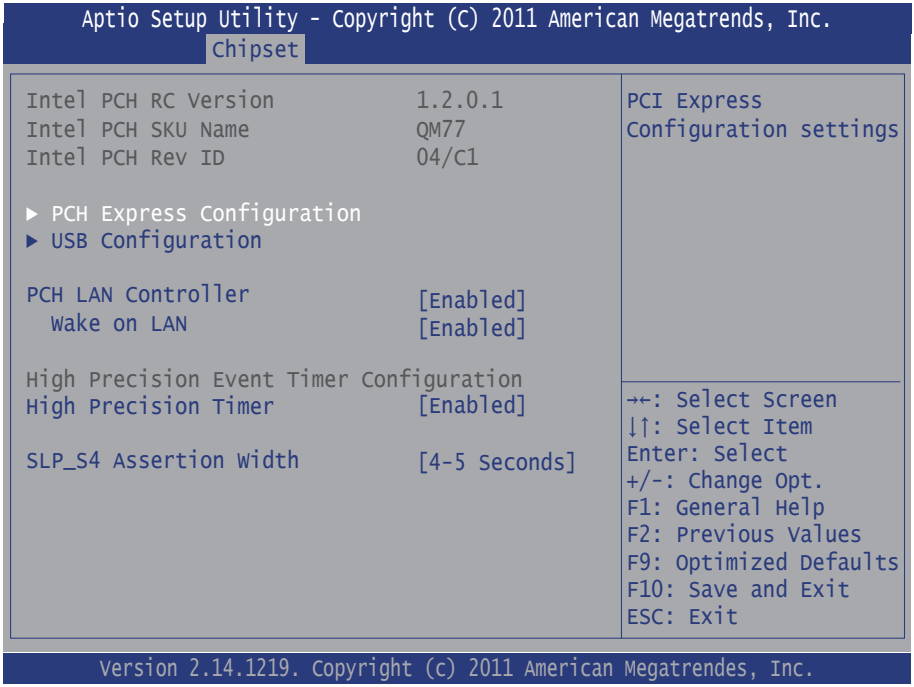
Long duration maintained	Time window which the long duration power is maintained.
Short duration power limit	Short duration power limit in watts, 0 means use factory default.
ACPI T State	**Enable** or **Disable** (default) ACPI T state support

3.3 Chipset



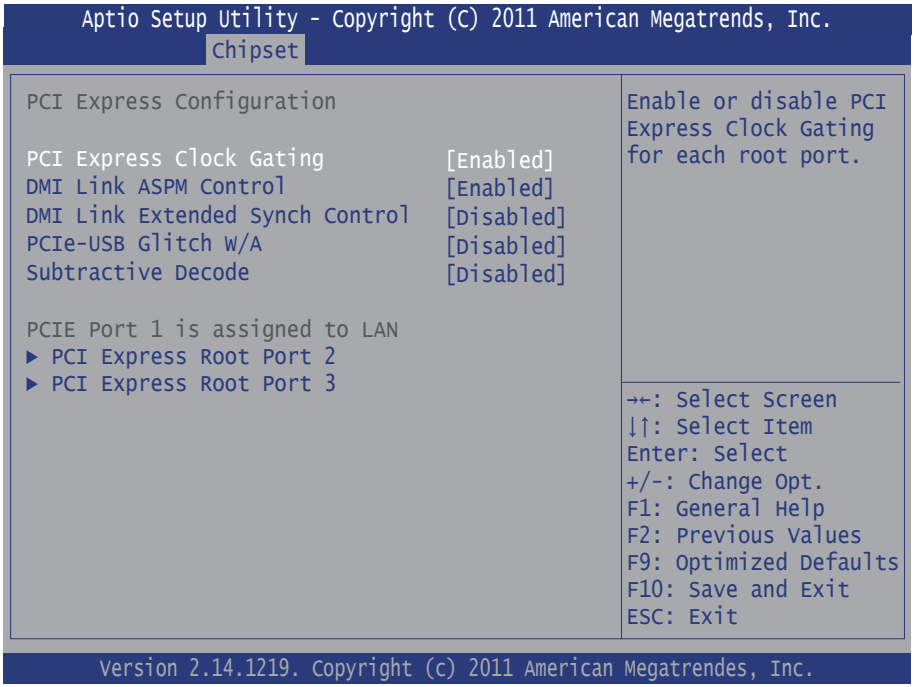
Setting	Description
PCH-IO Configuration	See Section 3.3.1
System Agent (SA) Configuration	See Section 3.3.2

3.3.1 PCH-IO Configuration

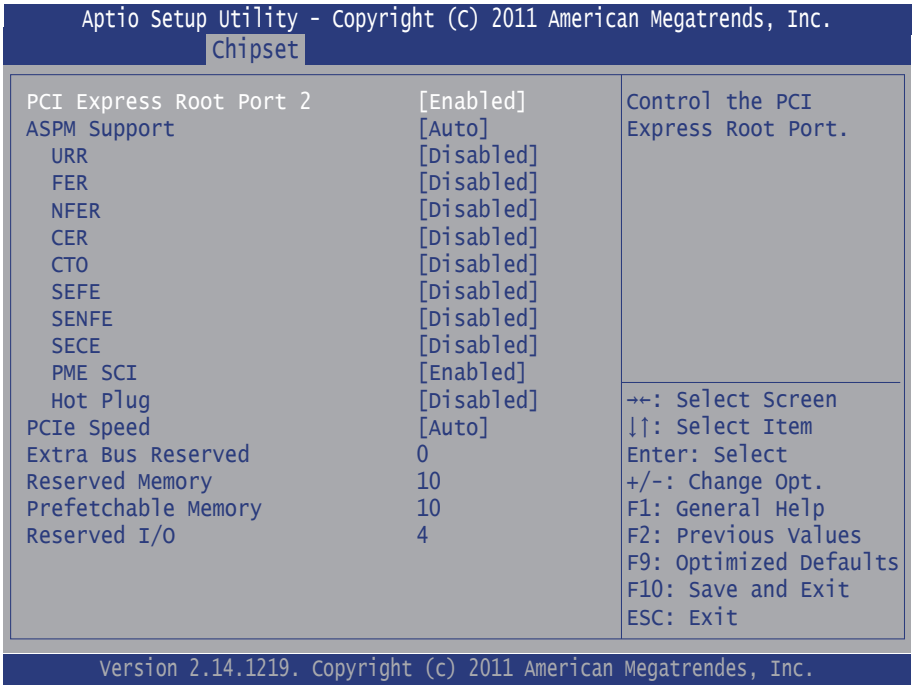


Setting	Description
PCH Express Configuration	See PCH Express Configuration tab
USB Configuration	See USB Configuration tab
PCH LAN Controller	**Enable** (default) or **Disable** onboard NIC.
Wake on LAN	**Enable** (default) or **Disable** integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)
High Precision Event Timer Configuration	
High Precision Timer	**Enable** (default) or **Disable** the High Precision Event Timer.
SLP_S4 Assertion Width	Select a minimum assertion width of the SLP_S4# signal. ► Options: **Disabled** (default)**, 1-2/2-3/3-4/4-5 Seconds**

PCI Express Configuration



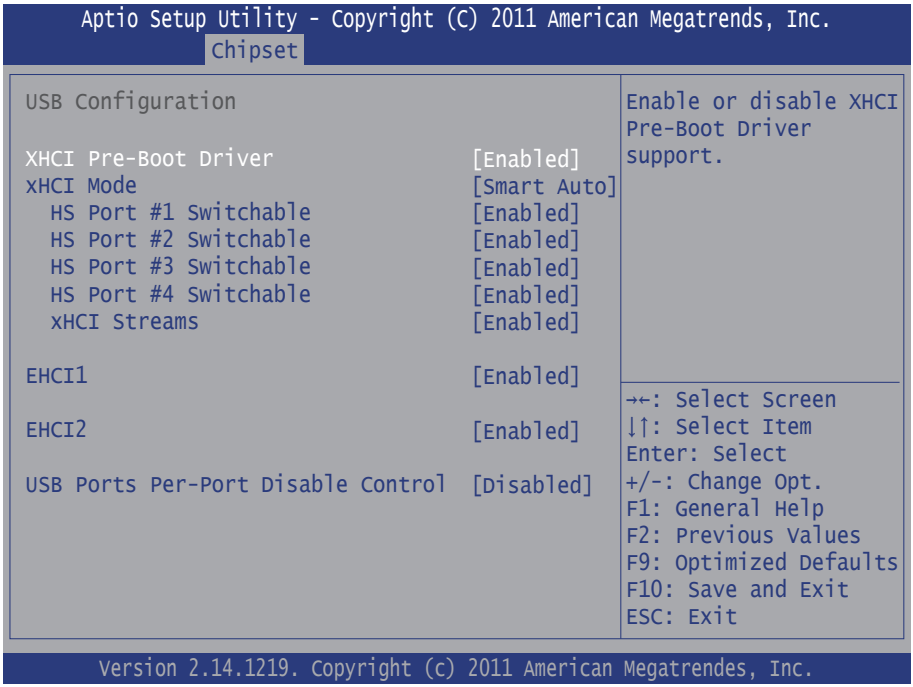
Setting	Description
PCI Express Clock Gating	**Enable** (default) or **Disable** PCI Express Clock Gating for each root port.
DMI Link ASPM Control	The control of Active State Power Management on both NB side and SB side of the DMI Link. ► Options: **Enabled** (default) and **Disabled**.
DMI Link Extended Synch Control	The control of Extended Synch on SB side of the DMI Link. ► Options: **Enabled** and **Disabled** (default).
PCIe-USB Glitch W/A	PCIe-USB Glitch W/A for bad USB devices connected behind PCIE/PEG Port. ► Options: **Enabled** and **Disabled** (default).
Subtractive Decode	**Enable** or **Disable** (default) PCI Express Subtractive Decode.



Setting	Description
PCI Express Root Port 2/3	Control the PCI Express Root Port. ► Options: **Enabled** (default) and **Disabled**.
ASPM Support	Set the ASPM Level: Force L0 - Force all links to L0 State; AUTO - BIOS auto configure; DISABLE - Disable ASPM ► Options: **Disabled**, **L0s**, **L1**, **L0sL1**, **Auto** (default)
URR	**Enable** or **Disable** (default) PCI Express Unsupported Request Reporting.
FER	**Enable** or **Disable** (default) PCI Express Device Fatal Error Reporting.
NFER	**Enable** or **Disable** (default) PCI Express Device Non-Fatal Error Reporting.

CER	**Enable** or **Disable** (default) PCI Express Device Correctable Error Reporting.
CTO	**Enable** or **Disable** (default) PCI Express Completion Timer TO.
SEFE	**Enable** or **Disable** (default) Root PCI Express System Error on Fatal Error.
SENFE	**Enable** or **Disable** (default) Root PCI Express System Error on Non-Fatal Error.
SECE	**Enable** or **Disable** (default) Root PCI Express System Error on Correctable Error.
PME SCI	**Enable** (default) or **Disable** PCI Express PME SCI.
Hot Plug	**Enable** or **Disable** (default) PCI Express Hot Plug.
PCIe Speed	Select PCI Express port speed. ► Options: **Auto** (default), **Gen1**, **Gen2**
Extra Bus Reserved	Extra Bus Reserved (0~7) for bridges behind this Root Bridge.
Reserved Memory	Reserved Memory (1~20) Range for this Root Bridge.
Prefetchable Memory	Prefetchable Memory (1~20) Range for this Root Bridge.
Reserved I/O	Reserved I/O (4k/8k/12k/16k/20k) Range for this Root Bridge.

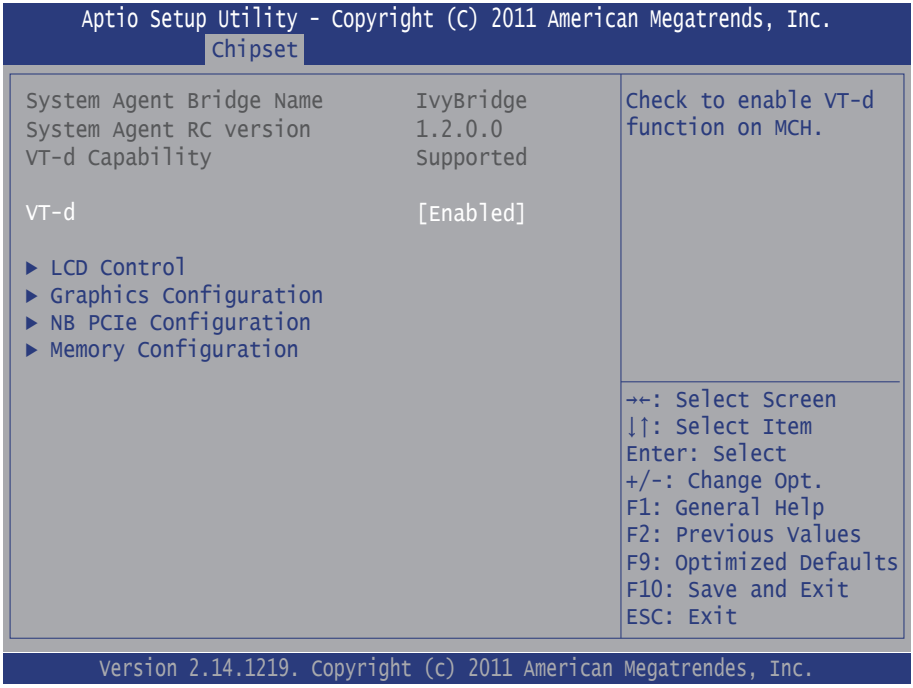
USB Configuration



Setting	Description
XHCI Pre-Boot Driver	**Enable** (default) or **Disable** XHCI Pre-Boot Driver support.
xHCI Mode	Mode of operation of xHCI controller. ► Options: **Smart Auto** (default), **Auto**, **Enabled**, **Disabled**
HS Port #1/2/3/4 Switchable	Always for HS port switching between xHCI and EHCI. If disabled, port is routed to EHCI. If HS port is routed to xHCI, the corresponding SS port is enabled. ► Options: **Enabled** (default) and **Disabled**.
xHCI Streams	**Enable** (default) or **Disable** xHCI Maximum Primary Stream Array Size.

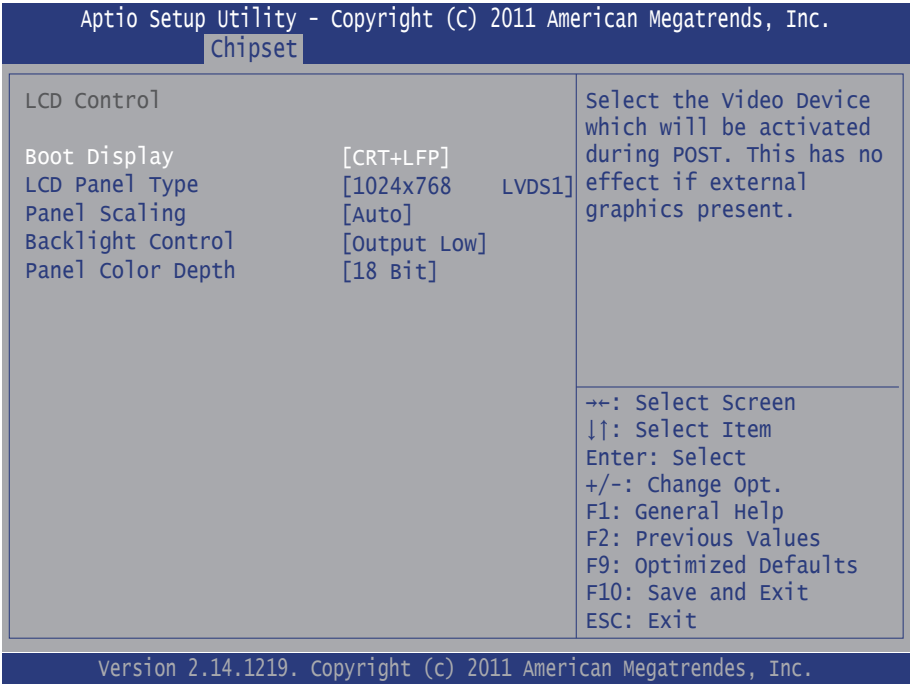
EHCI1/2	Control the USB EHCI (USB 2.0) functions. One EHCI controller must always be enabled. ► Options: **Enabled** (default) and **Disabled**.
USB Ports Per-Port Disable Control	Control each of the USB ports (0~13) disabling. ► Options: **Enabled** and **Disabled** (default).

3.3.2 System Agent (SA) Configuration



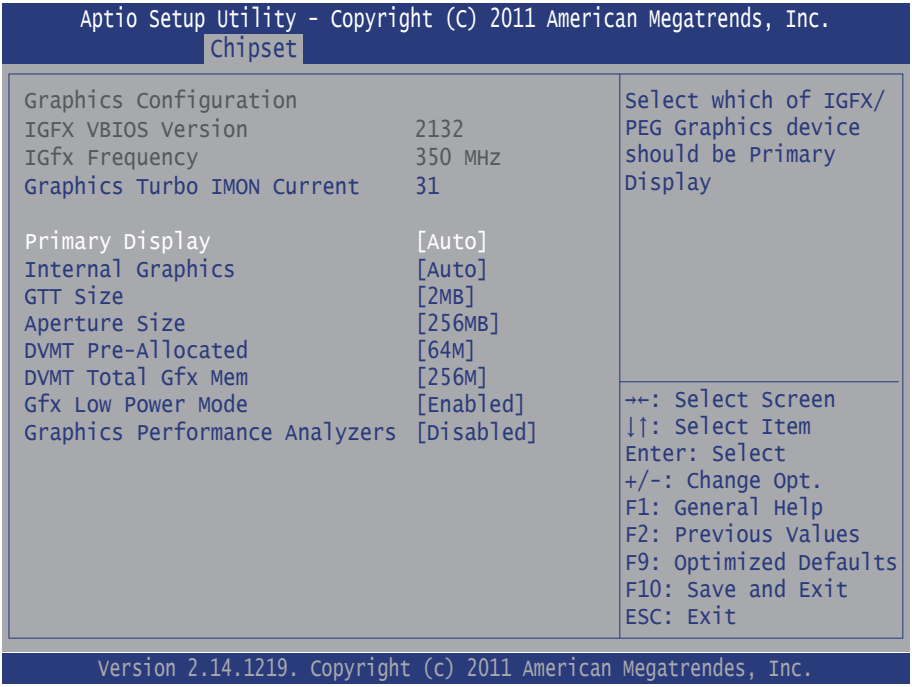
Setting	Description
VT-d	Check to enable VT-d function on MCH. ► Options: **Enabled** (default) and **Disabled**.
LCD Control	See LCD Control tab
Graphics Configuration	See Graphics Configuration tab
NB PCIe Configuration	See NB PCIe Configuration tab
Memory Configuration	See Memory Configuration tab

LCD Control



Setting	Description
Boot Display	Select the Video Device which will be activated during POST. This has no effect if external graphics present. ► Options: **VBIOS Default**, **CRT**, **DVI**, **LFP**, **CRT+LFP** (default), **DVI+LFP**
LCD Panel Type	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item. ► Options: **VBIOS Default**, **640x480 LVDS ~ 2048x1536 LVDS**
Panel Scaling	Select the LCD panel scaling option used by the Internal Graphics Device. ► Options: **Auto** (default), **Off**, **Force Scaling**
Backlight Control	Back Light Control Setting ► Options: **Output Low**, **Output High**
Panel Color Depth	Select the LFP Panel Color Depth ► Options: **18 Bit** (default), **24 Bit**

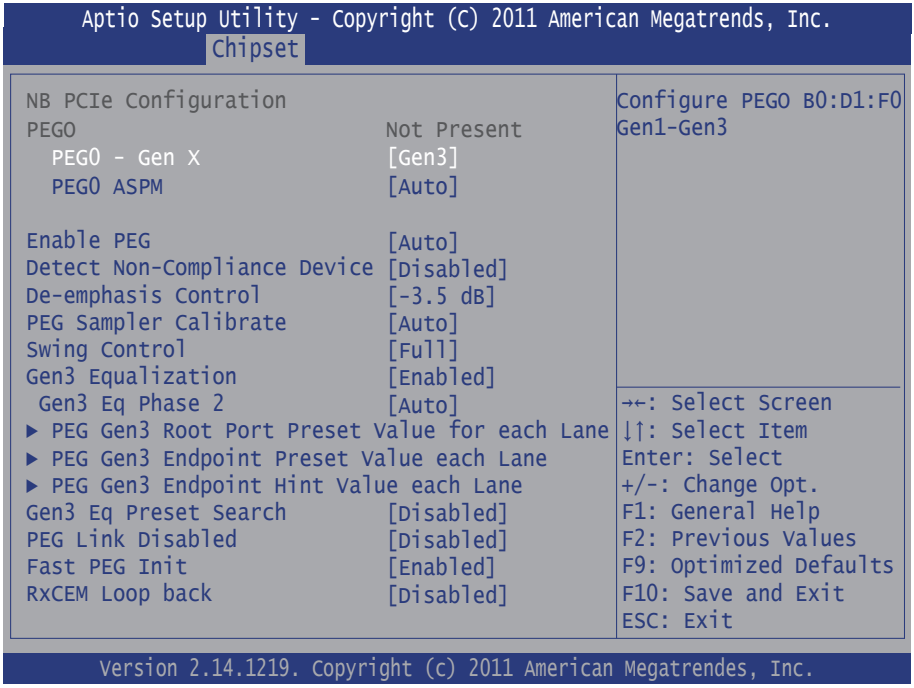
Graphics Configuration



Setting	Description
Graphics Turbo IMON Current	Graphics turbo IMON current values supported (14-31)
Primary Display	Select which of IGFX/PEG Graphics device should be Primary Display ► Options: **Auto** (default), **IGFX**, **PEG**
Internal Graphics	Keep IGD enabled based on the setup options. ► Options: **Auto** (default), **Disabled**, **Enabled**
GTT Size	Select the GTT Size ► Options: **1MB**, **2MB** (default)
Aperture Size	Select the Aperture Size ► Options: **128MB**, **256MB** (default), **512MB**
DVMT Pre-Allocated	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device. ► Options: **32/64** (default) **/96/128/160/192/224/ 256/288/320/352/384/416/448/480/512/1024M**

DVMT Total Gfx Mem	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device ► Options: **128M**, **256M** (default), **MAX**
Gfx Low Power Mode	This option is applicable for SFF only. ► Options: **Enabled** (default) and **Disabled**.
Graphics Perfor-mance Analyzers	**Enable** or **Disable** (default) Intel Graphics Perfor-mance Analyzers Counters.

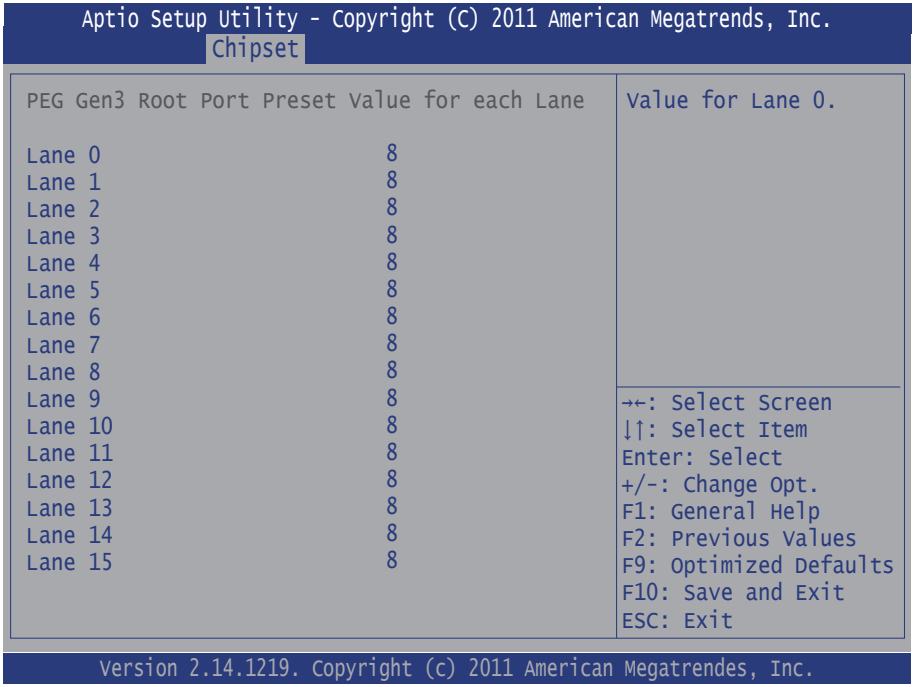
NB PCIe Configuration



Setting	Description
PEG0 - Gen X	Configure PEG0 B0:D1:F0 Gen1-Gen3 ► Options: **Auto**, **Gen1**, **Gen2**, **Gen3** (default)

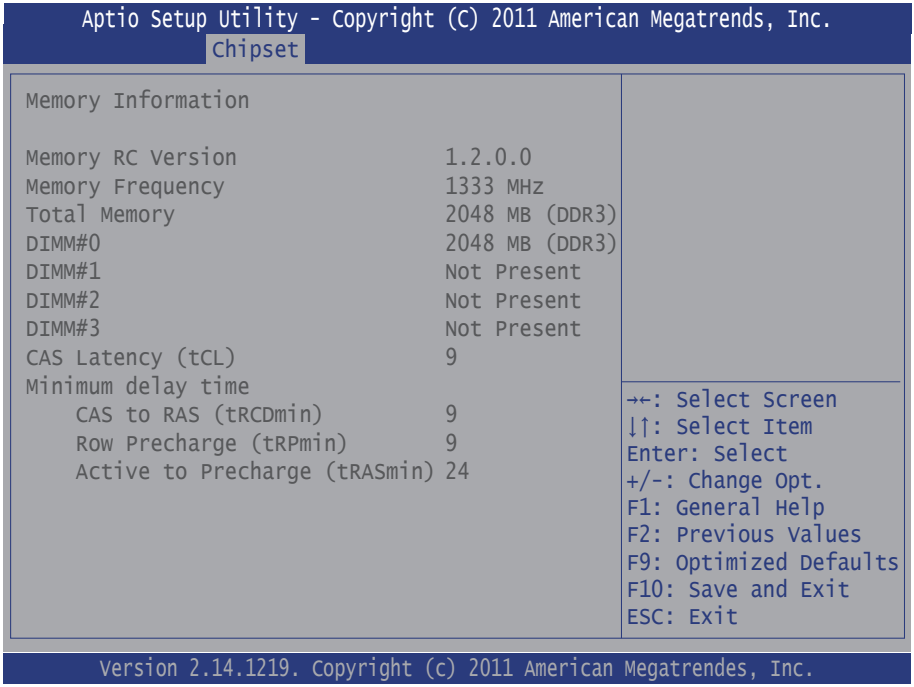
PEG0 ASPM	Control ASPM support for the PEG: Device 1 Function 0. This has no effect if PEG is not the currently active device. ► Options: **Disabled**, **Auto** (default), **ASPM L0s**, **ASPM L1**, **ASPM L0sL1**
Enable PEG	To enable or disable the PEG. ► Options: **Disabled**, **Enabled**, **Auto** (default)
Detect Non-Compliance Device	Detect Non-Compliance PCI Express Device in PEG ► Options: **Enabled** and **Disabled** (default).
De-emphasis Control	Configure the De-emphasis control on PEG ► Options: **-6 dB**, **-3.5 dB** (default)
PEG Sampler Calibrate	**Enable** or **Disable** PEG Sampler Calibrate. **Auto** (default) means disabled for SNB MB/DT. Enbaled for IVB A0 B0.
Swing Control	Perform PEG Swing Control, on IVB C0 and later. ► Options: **Reduced**, **Half** and **Full** (default).
Gen3 Equalization	Perform PEG Gen3 Equalization steps ► Options: **Enabled** (default) and **Disabled**.
Gen3 Eq Phase 2	Perform PEG Gen3 Equalization Phase 2 ► Options: **Auto** (default), **Enabled** and **Disabled**.
PEG Gen3...	See PEG Gen3... tab
Gen3 Eq Preset Search	Perform PEG Gen3 Preset Search algorithm, on IVB C0 and Later. ► Options: **Enabled** and **Disabled** (default)
PEG Link Disabled	**Enable** or **Disable** (default) PCIe link disable mechanism for additional power saving.
Fast PEG Init	**Enable** (default) or **Disable** Fast PEG Init. Some optimization if no PEG devices present in cold boot.
RxCEM Loop back	**Enable** or **Disable** (default) RxCEM Loop back.

PEG Gen3...

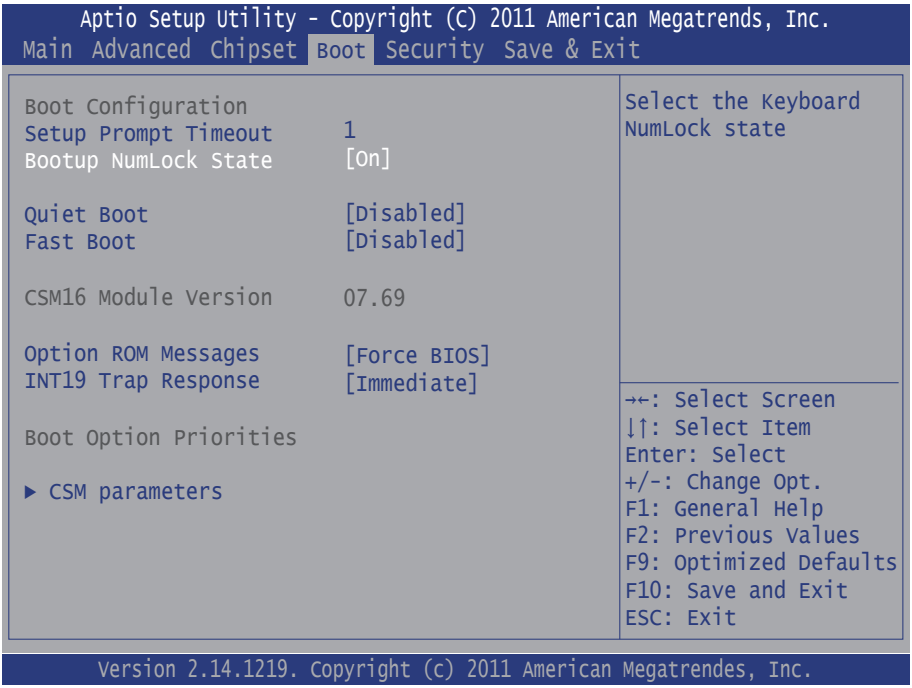


Setting	Description
Lane 0~15	Value for Lane 0~15. ► Options: **1~11**

Memory Configuration



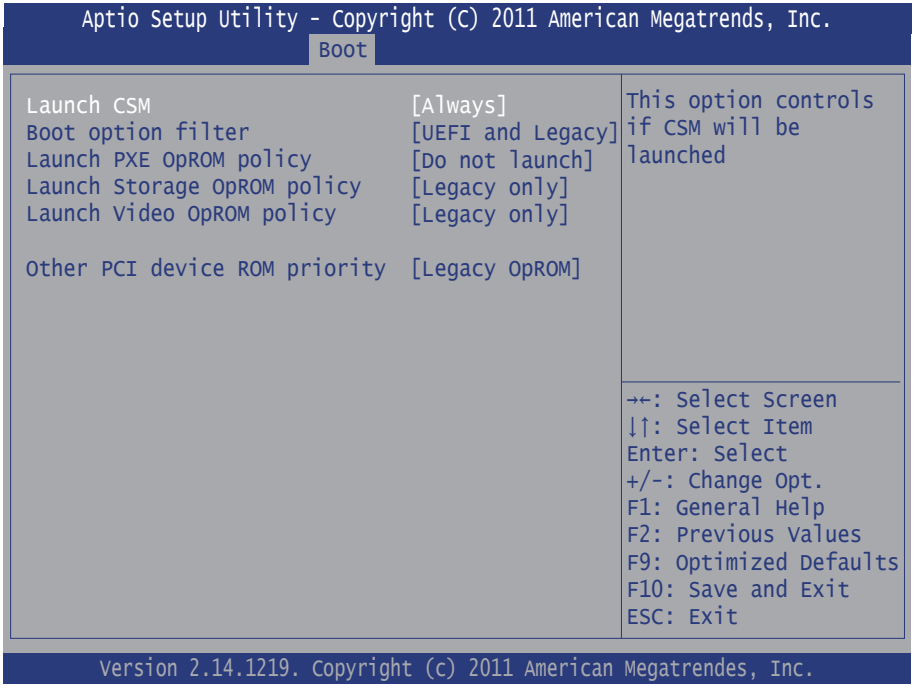
3.4 Boot



Setting	Description
Setup Prompt Time-out	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	Select the keyboard NumLock state ► Options: **On** (default), **Off**
Quiet Boot	**Enable** or **Disable** (default) Quiet Boot option.
Fast Boot	**Enable** or **Disable** (default) boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.
Option ROM Messages	Set display mode for Option ROM. Options: **Force BIOS** (default) and **Keep Current**.
INT19 Trap Response	BIOS reaction on INT19 trapping by Option ROM: IMMEDIATE - execute the trap right away; POSTPONED - execute the trap during legacy boot. ► Options: **Immediate** (default) and **Postponed**.

CSM parameters	See Section 3.4.1

3.4.1 CSM parameters

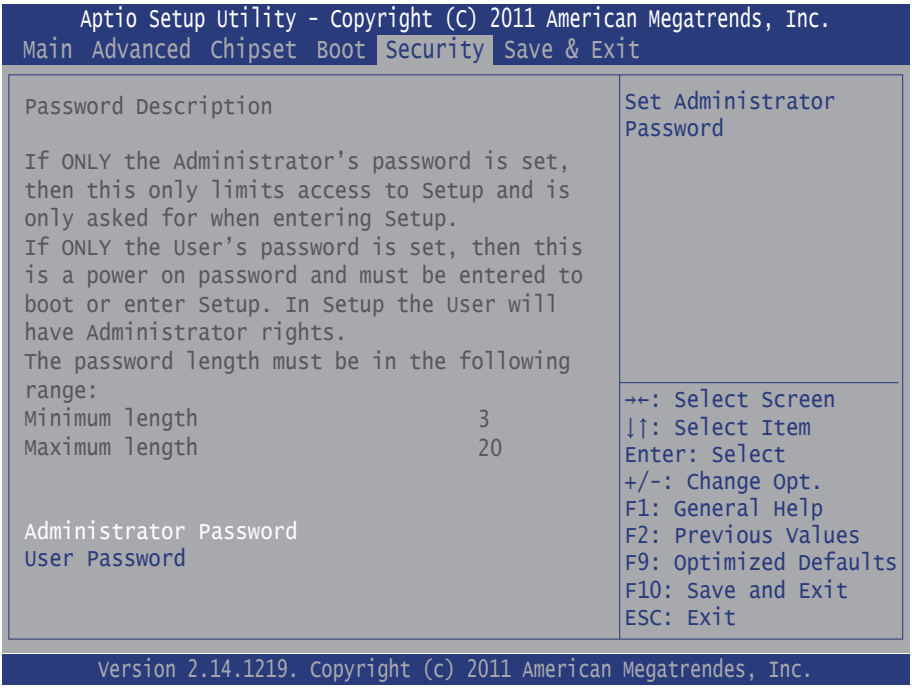


Setting	Description
Launch CSM	This option controls if CSM will be launched. ► Options: **Always** (default), **Never**.
Boot option filter	This option controls what devices system can boot to ► Options: **UEFI and Legacy** (default), **Legacy only**, **UEFI only**
Launch PXE OpROM policy	Controls the execution of UEFI and Legacy PXE OpROM. ► Options: **Do not launch** (default), **UEFI only**, **Legacy only**.

Launch Storage OpROM policy	Controls the execution of UEFI and Legacy Storage OpROM. ► Options: **Do not launch**, **UEFI only**, **Legacy only** (default).
Launch Video OpROM policy	Controls the execution of UEFI and Legacy Video OpROM. ► Options: **Do not launch**, **UEFI only**, **Legacy only** (default).
Other PCI device ROM priority	For PCI devices other than Network, Mass storage or Video defines which OpROM to launch ► Options: **UEFI OpROM**, **Legacy OpROM** (default)

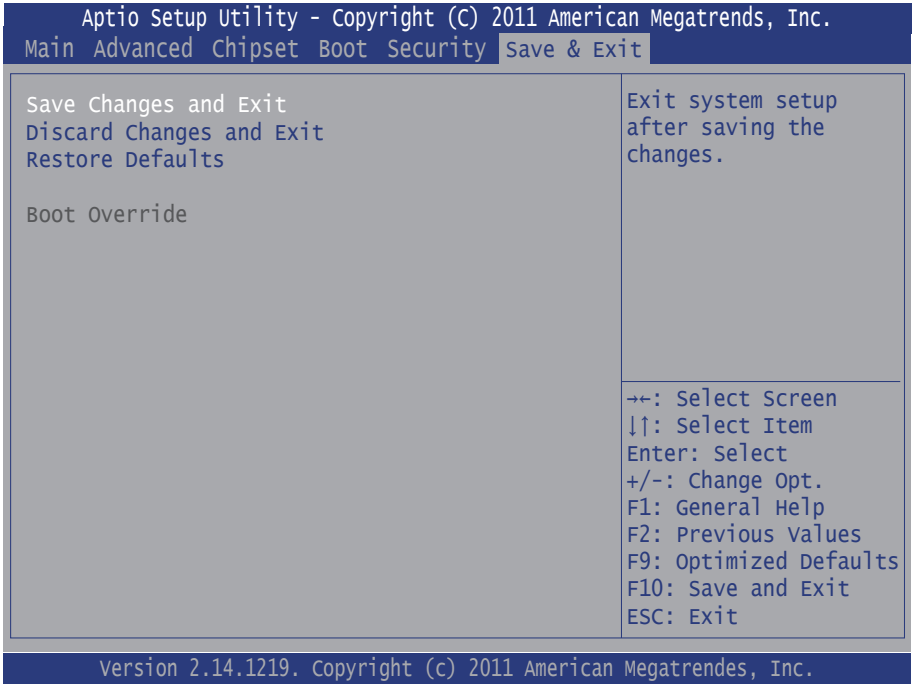
3.5 Security

The **Security** menu sets up the administrator or user password. Once an administrator password is set up, this BIOS SETUP utility is limited to access and will ask for the password each time any access is attempted.



Setting	Description
Administrator/User Password	To set up an administrator password: 1. Select **Administrator Password**. The screen then pops up an **Create New Password** dialog. 2. Enter your desired password that is no less than 3 characters and no more than 20 characters. 3. Hit [Enter] key to submit.

3.6 Save & Exit Options



Setting	Description
Save Changes and Exit	Saves the changes and resets the system. ► Enter the item and then a dialog box pops up: **Save configuration and exit?**
Discard Changes and Exit	Exit system setup without saving any changes. ► Enter the item and then a dialog box pops up: **Quit without saving?**
Restore Defaults	Restore/Load Default values for all the setup options. ► Enter the item and then a dialog box pops up: **Load Optimized Defaults?**
Boot Override	**Boot Override** presents a list of boot devices on screen. Select the device to boot up the system regardless of the currently configured boot priority.

3.7 AMI BIOS Checkpoints

3.7.1 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

3.7.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed

0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.

0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available

0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)

0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable

0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found

0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

Appendix

Appendix A: I/O Port Address Map

Each peripheral device in the system is assigned with a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0x00000060-0x00000060	Standard PS / 2 Keyboard
0x00000064-0x00000064	Standard PS / 2 Keyboard
0x000002F0-0x000002F7	Communications Port (COM5)
0x000002E0-0x000002E7	Communications Port (COM6)
0x000003F8-0x000003FF	Communications Port (COM1)
0x0000E000-0x0000EFFF	Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 2 - 1E12
0x000002F8-0x000002FF	Communications Port (COM2)
0x000003E8-0x000003EF	Communications Port (COM3)
0x000002E8-0x000002EF	Communications Port (COM4)
0x0000F000-0x0000F03F	Intel(R) HD Graphics 4000
0x000003B0-0x000003BB	Intel(R) HD Graphics 4000
0x000003C0-0x000003DF	Intel(R) HD Graphics 4000
0x00000000-0x00000CF7	PCI bus
0x00000000-0x00000CF7	Direct memory access controller
0x00000D00-0x0000FFFF	PCI bus
0x00000070-0x00000077	System CMOS/real time clock
0x00000070-0x00000077	Motherboard resources
0x0000F0E0-0x0000F0E7	Intel(R) Active Management Technology - SOL (COM7)
0x00000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000044-0x0000005F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000084-0x00000086	Motherboard resources

0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources
0x000004D0-0x000004D1	Motherboard resources
0x000004D0-0x000004D1	Programmable interrupt controller
0x00000A00-0x00000A1F	Motherboard resources
0x00000290-0x0000029F	Motherboard resources
0x00000454-0x00000457	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x00000200-0x0000020F	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x00000400-0x00000453	Motherboard resources
0x00000458-0x0000047F	Motherboard resources
0x00000500-0x0000057F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller

0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000000F0-0x000000FF	Numeric data processor
0x0000F040-0x0000F05F	Intel(R) 7 Series/C216 Chipset Family SMBus Host Controller - 1E22
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer
0x0000F0D0-0x0000F0D7	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E03
0x0000F0C0-0x0000F0C3	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E03
0x0000F0B0-0x0000F0B7	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E03
0x0000F0A0-0x0000F0A3	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E03
0x0000F060-0x0000F07F	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E03
0x00000081-0x00000091	Direct memory access controller
0x00000093-0x0000009F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller

Appendix B: BIOS Memory Map

Address	Device Description
0xF7E38000-0xF7E383FF	Intel(R) 7 Series/C216 Chipset Family USB Enhanced Host Controller - 1E2D
0xF7C00000-0xF7DFFFFF	Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 2 - 1E12
0xF7C00000-0xF7DFFFFF	Intel(R) 82583V Gigabit Network Connection #2
0xF7E20000-0xF7E2FFFF	Intel (R) USB 3.0 Extensible Host Controller
0xF7800000-0xF7BFFFFF	Intel(R) HD Graphics 4000
0xE0000000-0xEFFFFFFF	Intel(R) HD Graphics 4000
0xA0000-0xBFFFF	Intel(R) HD Graphics 4000
0xA0000-0xBFFFF	PCI bus
0xF7E3C000-0xF7E3C00F	Intel(R) Management Engine Interface
0xD0000-0xD3FFF	PCI bus
0xD4000-0xD7FFF	PCI bus
0xD8000-0xDBFFF	PCI bus
0xDC000-0xDFFFF	PCI bus
0xE0000-0xE3FFF	PCI bus
0xE4000-0xE7FFF	PCI bus
0x7DA00000-0xFEAFFFFF	PCI bus
0x7DA00000-0xFEAFFFFF	Motherboard resources
0xF7E00000-0xF7E1FFFF	Intel(R) 82579LM Gigabit Network Connection
0xF7E39000-0xF7E39FFF	Intel(R) 82579LM Gigabit Network Connection
0xF7E3A000-0xF7E3AFFF	Intel(R) Active Management Technology - SOL (COM7)
0xFED40000-0xFED44FFF	System board
0x20000000-0x201FFFFF	System board
0x40004000-0x40004FFF	System board
0xFF000000-0xFFFFFFFF	Intel(R) 82802 Firmware Hub Device

0xFF000000-0xFFFFFFFF	Motherboard resources
0xFED1C000-0xFED1FFFF	Motherboard resources
0xFED10000-0xFED17FFF	Motherboard resources
0xFED18000-0xFED18FFF	Motherboard resources
0xFED19000-0xFED19FFF	Motherboard resources
0xF8000000-0xFBFFFFFF	Motherboard resources
0xFED20000-0xFED3FFFF	Motherboard resources
0xFED90000-0xFED93FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFEE00000-0xFEEFFFFF	Motherboard resources
0xF7D40000-0xF7D5FFFF	Intel(R) 82583V Gigabit Network Connection #2
0xF7D60000-0xF7D63FFF	Intel(R) 82583V Gigabit Network Connection #2
0xF7E30000-0xF7E33FFF	High Definition Audio Controller
0xF7E35000-0xF7E350FF	Intel(R) 7 Series/C216 Chipset Family SMBus Host Controller - 1E22
0xFED00000-0xFED003FF	High Precision Event Timer, HPET
0xF7E36000-0xF7E367FF	Intel(R) 7 Series/C216 Chipset Family SATA AHCI Controller - 1E03
0xF7E37000-0xF7E373FF	Intel(R) 7 Series/C216 Chipset Family USB Enhanced Host Controller - 1E26

Appendix C: Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the required service. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 12	Microsoft PS/2 Mouse
IRQ 1	Standard PS / 2 Keyboard
IRQ 5	Communications Port (COM5)
IRQ 7	Communications Port (COM6)
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 3	Intel(R) 7 Series/C216 Chipset Family SMBus Host Controller - 1E22
IRQ 10	Communications Port (COM3)
IRQ 11	Communications Port (COM4)
IRQ 8	System CMOS/real time clock
IRQ 13	Numeric data processor
IRQ 0	System timer

Appendix D: Digital I/O Setting

Below are the source codes written in C, please take them for Digital I/O application examples. The default I/O address is 6Eh.

C Language Code

```
//==== History ====//
//compile by TCPP 3.0
//R00     5/18/2010          1st modify

//#include "ring1726.h"
#include <stdio.h>
#include <dos.h>
#include <conio.h>

#define EC_CMD_Port                 0x6C
#define  EC_DATA_Port    0x68

unsigned long Process_686C_Command_Write(unsigned long m_ECCMD, un-
signed long m_ECDATA);
unsigned long Process_686C_Command_Read(unsigned long m_ECCMD );
unsigned long ECU_Write_686C_RAM_BYTE( unsigned long
ECUMemAddr,unsigned long ECUMemData );
unsigned long ECU_Read_686C_RAM_BYTE( unsigned long ECUMemAddr );
unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int REG_INDEX);
void SMB_Byte_WRITE(int SMPORT, int DeviceID, int REG_INDEX, int REG_
DATA);



char APName[]=       "\t\tMB-M671 DIO Testing Program\n"
                     "\t==========================================\n" ;

char APHelp[]=    "\n - Pass 'A' key for inver state of DIO GP1x"
                                "\n - Pass 'S' key for inver state of DIO GP2x"
                                "\n - Pass 'D' key for inver state of DIO GP3x"
                     "\n - Pass 'Esc' key for Exit"
                     "\n" ;

void main(void){
          char getkey = 0;
     //   char DIOSTS=0;
     //   char tempJ=0;
```

```
    //    char tempA=0;
          unsigned char GP2xVal,GP3xVal,GP1xVal;
          int SMB_PORT_AD  = 0xF040;
          //--int SMB_DEVICE_ADD = 0x9C;  /*75111R's Add=6eh */
          int SMB_DEVICE_ADD = 0x6E;       /*75111R's Add=6eh */

          clrscr();  //clear screen
          printf(APName);
          printf(APHelp);

          //pg DIO as output
          //0:input 1:Output
/*        Index 10, GPIO1x Output pin control          */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x10,0xff);
          delay(10);
/*        Index 20, GPIO2x Output pin control          */
//poweron defalult 0x00::::  SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_
ADD,0x20,0x00); //pg as Input
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x20,0xff);
/*        Index 40, GPIO3x Output pin control          */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x40,0x0f);
          delay(10);

          //pg DIO default LOW
/*        Index 11, GPIO1x Output Data value           */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,0x00);
          GP1xVal = 0;
          delay(10);

/*        Index 21, GPIO2x Output Data value           */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x21,0x00);
          GP2xVal = 0;
          delay(10);

/*        Index 41, GPIO3x Output Data value           */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x41,0x00);
          GP3xVal = 0;

          gotoxy(1,9);
          //printf("DIO Status: Low \n");

          do{
                    if (getkey != 27){
                              while (!kbhit());
```

```
getkey = getch();
switch (getkey){
        case ‘D’:
        case ‘d’:
                if (GP3xVal == 0)
                {
                        GP3xVal = 1; //DIO
                        //pg DIO high
                        SMB_Byte_

                        gotoxy(1,10);
                        printf(“GP3x Status:

                }
                else
                {
                        GP3xVal = 0; //DIO
                        //pg DIO LOW
                        SMB_Byte_

                        gotoxy(1,10);
                        printf(“GP3x Status:
                }

                break;
        case ‘A’:
        case ‘a’:
                if (GP1xVal == 0)
                {
                        GP1xVal = 1; //DIO
                        //pg DIO high
                        SMB_Byte_

                        gotoxy(1,8);
                        printf(“GP1x Status:

                }
                else
                {
                        GP1xVal = 0; //DIO
                        //pg DIO LOW
                        SMB_Byte_

                        gotoxy(1,8);
```

```
                                                    printf("GP1x Status:
                                        }
                                    break;
                                case 'S':
                                case 's':
                                        if (GP2xVal == 0)
                                        {
                                            GP2xVal = 1; //DIO
                                            //pg DIO high
                                            SMB_Byte_

                                            gotoxy(1,9);
                                            printf("GP2x Status:

                                        }
                                        else
                                        {
                                            GP2xVal = 0; //DIO
                                            //pg DIO LOW
                                            SMB_Byte_

                                            gotoxy(1,9);
                                            printf("GP2x Status:
                                        }
                                    break;
                                default:
                                    break;
                            };
                            //-printf( "Input: [%c]       ", getkey);  //DEBUG
                    };
            }while (getkey != 27); //ESC ascii==27
            //pg all DIO as Input
}


unsigned long Process_686C_Command_Write(unsigned long m_ECCMD, un-
{
 //-----------------------------------------------------------------------
 int     i,temp;
 unsigned long m_OutBuf;
 //-----------------------------------------------------------------------
 m_OutBuf=inportb(0x6C);
 if ( ( m_OutBuf&0x00000003) > 0 )
    {
```

```
      // temp=inportb(0x68);
      return 0xFFFFFFFF;
     }

 outport(0x6C,m_ECCMD);
 for ( i=0; i<=4000; i++ )
 {
    m_OutBuf=inportb(0x6C);
    if ( ( m_OutBuf&0x00000002) == 0 )  break;
 }
  if ( i < 3999 )
     {
       outport(0x68,m_ECDATA);
        for ( i=0; i<=4000; i++ )
        {
          m_OutBuf=inportb(0x6C);
          if ( ( m_OutBuf&0x00000002) == 0 )
                {    return 0x00000000;  }
        }
     }

 if ( i > 3999 )   m_OutBuf=inportb(0x68);
 return 0xFFFFFFFF;
}
//---------------------------------------------------------------------------
unsigned long Process_686C_Command_Read(unsigned long m_ECCMD )
{
int i,temp;
 unsigned long m_OutBuf,m_InBuf;
 m_OutBuf=inportb(0x6C);
if ( ( m_OutBuf&0x00000003) > 0 )
    {
       temp=inportb(0x68);
       return 0xFFFFFFFF;

     }
 m_InBuf = m_ECCMD;
 outport(0x6C,m_InBuf);
 for ( i=0; i<=3500; i++ )
 {
    m_OutBuf=inportb(0x6C);
   if ( ( m_OutBuf&0x00000001) > 0 )
    {
      temp=inportb(0x68);
```

```
      temp= (temp & 0x000000FF ) ;
      return temp;
     // break;
    }
 }
 if ( i > 3499 )
    {
    temp=inportb(0x68);
    return 0xFFFFFFFF;
     }
 return 0xFFFFFFFF;
 }

//---------------------------------------------------------------------------
 unsigned long ECU_Read_686C_RAM_BYTE( unsigned long ECUMemAddr )
{
  unsigned long uDATA1,uDATA2,ECRamAddrH,ECRamAddrL;
  ECRamAddrL=ECUMemAddr%256;   ECRamAddrH=ECUMemAddr/256;
  //
  uDATA1=Process_686C_Command_Write(0x000000A3, ECRamAddrH );
  if ( uDATA1==0xFFFFFFFF ) { return 0xFFFFFFFF; }
  //
  uDATA1=Process_686C_Command_Write(0x000000A2, ECRamAddrL );
  if ( uDATA1==0xFFFFFFFF ) { return 0xFFFFFFFF; }
  //
  uDATA1=Process_686C_Command_Read( 0x000000A4 );
  if ( uDATA1 > 0x000000FF ) { return 0xFFFFFFFF; }
  uDATA2=Process_686C_Command_Read( 0x000000A4 );
  if ( uDATA2 > 0x000000FF ) { return 0xFFFFFFFF; }
  if (uDATA1==uDATA2) return uDATA1;
  else return  0xFFFFFFFF;
}
//---------------------------------------------------------------------------
 unsigned long ECU_Write_686C_RAM_BYTE( unsigned long
ECUMemAddr,unsigned long ECUMemData )
{
  unsigned long uDATA, RD_DATA, ECRamAddrH, ECRamAddrL;
  ECRamAddrL=ECUMemAddr%256;   ECRamAddrH=ECUMemAddr/256;
  //
  uDATA=Process_686C_Command_Write(0x000000A3, ECRamAddrH );
  if ( uDATA==0xFFFFFFFF ) { return 0xFFFFFFFF;}
  //
  uDATA=Process_686C_Command_Write(0x000000A2, ECRamAddrL );
  if ( uDATA==0xFFFFFFFF ) { return 0xFFFFFFFF;}
```

```
  //
  uDATA=Process_686C_Command_Write(0x000000A5, ECUMemData );
  if ( uDATA==0xFFFFFFFF ) { return 0xFFFFFFFF;}
  //
  return  0x00000000;
}
//-------------------------------------------------------------------------


unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int REG_INDEX)
{
        unsigned char SMB_R;
        outportb(SMPORT+02, 0x00);          /* clear */
        outportb(SMPORT+00, 0xff);          /* clear */
        delay(10);
        outportb(SMPORT+04, DeviceID+1);        /* clear */
        outportb(SMPORT+03, REG_INDEX);           /* clear */
        outportb(SMPORT+02, 0x48);          /* read_byte */
        delay(10);
        //printf(" %02x ",inportb(SMPORT+05));
        SMB_R= inportb(SMPORT+05);
        return SMB_R;
}

void SMB_Byte_WRITE(int SMPORT, int DeviceID, int REG_INDEX, int REG_
DATA)
{
        outportb(SMPORT+02, 0x00);          /* clear */
        outportb(SMPORT+00, 0xff);          /* clear */
        delay(10);
        outportb(SMPORT+04, DeviceID);                /* clear */
        outportb(SMPORT+03, REG_INDEX);           /* clear */
        outportb(SMPORT+05, REG_DATA);            /* read_byte */
        outportb(SMPORT+02, 0x48);          /* read_byte */
/*      delay(10);
        printf(" %02x ",inportb(SMPORT+05)); */
}
```

Digital IO Usage Table (Super IO Chipset F75111)

Pin	Description	Chipset Pin#	Chipset Pin Description
1	DIO0	10	GPIO10
2	DIO1	11	GPIO11
3	DIO2	12	GPIO12
4	DIO3	3	GPIO13
5	DIO4	9	GPIO14
6	DIO5	19	GPIO15
7	DIO6	4	GPIO16
8	DIO7	5	GPIO17
9	DIO8	6	GPIO20
10	DIO9	7	GPIO21
11	DIO10	8	GPIO22
12	DIO11	24	GPIO23
13	DIO12	23	GPIO24
14	DIO13	22	GPIO25
15	DIO14	21	GPIO26
16	DIO15	20	GPIO27

Appendix E: Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitor the activity of CPU. Application software depends on its own requirement to trigger WDT with adequate timer setting. Before WDT time-out, the functional normal system will reload the WDT. The WDT never times out for a normal system. Then, WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255-level watchdog timer by software programming. Below are the source codes written in C, please take them as WDT application example.

```
/*-----    Include Header Area -----*/
#include “math.h”
#include “stdio.h”
#include “dos.h”

/*-----    routing, sub-routing -----*/

void main()
{
        outportb(0x2e, 0x87);              /* initial IO port */
        outportb(0x2e, 0x87);          /* twice,  */

        outportb(0x2e, 0x07);          /* point to logical device */
        outportb(0x2e+1, 0x07);          /* select logical device 7 */
        outportb(0x2e, 0xf5);          /* select offset f5h */
        outportb(0x2e+1, 0x40);          /* set bit5 = 1 to clear bit5 */
        outportb(0x2e, 0xf0);          /* select offset f0h */
        outportb(0x2e+1, 0x81);          /* set bit7 =1 to enable WDTRST# */
        outportb(0x2e, 0xf6);          /* select offset f6h */
        outportb(0x2e+1, 0x05);          /* update offset f6h to 0ah :10sec */
        outportb(0x2e, 0xf5);          /* select offset f5h */
        outportb(0x2e+1, 0x20);          /* set bit5 = 1 enable watch dog time
*/

        outportb(0x2e, 0xAA);          /* stop program F71869E, Exit */
}
```

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