ITX-i67M0

Mini-ITX Industrial Motherboard

User's Manual

Version 1.2

2012.11

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Chapter 1

Introduction

1.1 Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

1.2 Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class B

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-- Reorient or relocate the receiving antenna.

-- Increase the separation between the equipment and receiver.

-- Connect the equipment into an outlet on a circuit different from that to

which the receiver is connected.

-- Consult the dealer or an experienced radio/TV technician for help.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain

unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

1.3 About This User's Manual

This user's manual provides general information and installation instructions about the product. This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. please consult your vendor before further handling.

1.4 Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.

2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.

3. Use a grounded wrist strap when handling computer components.

4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

1.5 Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

1.6 Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor.com.tw

E-mail:info@arbor.com.tw

1.7 Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

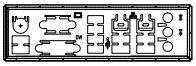
Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

1.8 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

1 x ITX-i67M0 Mini-ITX industrial motherboard

1 x Driver CD
1 x Quick Installation Guide



1 x I/O Bracket

If any of the above items is damaged or missing, contact your vendor immediately.

1.9 Ordering Information

ITX-i67M0	Intel® rPGA988 socket embedded Mini-ITX motherboard
CPF-67M0-C1	CPU cooling fan for rPGA988 CPU
CBK-11-67M0-00	Cable kit 2 x Two ports COM cables 1 x COM Flat cable 1 x USB cable 2 x SATA cables 1 x SATA Power cable

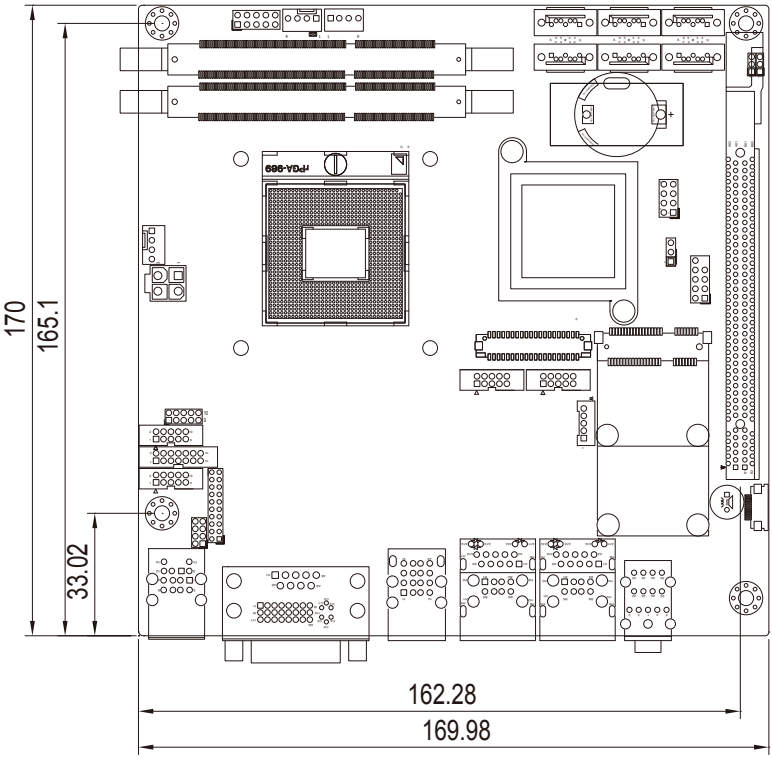
1.10 Recommended CPU List

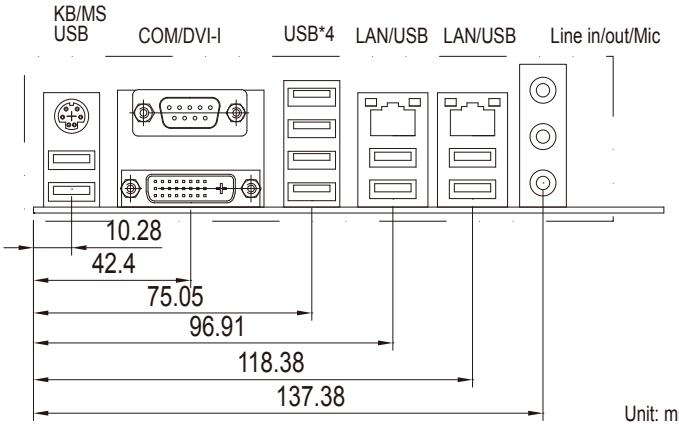
i7-2710QE 2.1GHz Core™ Processor
i5-2510E 2.5GHz Core™ Processor
i3-2330E 2.2GHz Core™ Processor
B810 1.6GHz Celeron® Processor

1.11 Specifications

Form Factor	Mini-ITX Industrial Motherboard
CPU	Intel® Core™ i7/i5/i3, Celeron® processor in rPGA988 (Socket G2)
Chipset	Intel® QM67
System Memory	2 x 204-pin DDR3 SO-DIMM sockets supporting 1066/1333 MHz SDRAM up to 8GB
Graphics Controller	Integrated Intel® HD Graphics 3000
	DVI-I/ Dual Channels 18/24-bit LVDS
I/O Chip	Fintek F71869ED + Fintek F81216AD
BIOS	AMI BIOS 64Mb SPI ROM
Audio	Realtek ALC886 Audio Codec (Line-in/ Line-out/ Mic-in)
Storage	6 x SATA ports: 2 x Serial ATA 3.0 ports with 600MB/s HDD transfer rate 4 x Serial ATA 2.0 ports with 300MB/s HDD transfer rate Support RAID 0, 1 , 5, 10
Ethernet	1 x Intel® 82579LM PCIe GbE PHY w/ iAMT 1 x Intel® 82583V GbE controller
USB Port	12 x USB 2.0 ports: 6 ports with double stacked USB type A connector 4 ports with four stacked USB type A connector 2 ports by internal pin header
Serial Port	6 x COM ports: 5 x RS-232 ports 1 x RS-232/422/485 selectable port w/ auto-flow control
KB/MS	One 6-pin mini-DIN connector for PS/2 Keyboard & Mouse via Y-Cable
Digital I/O	16-bit programmable Digital Input/Output
Expansion Bus	1 x Mini-card slot 1 x PCIe x16 slot
Watchdog Timer	1~255 levels reset
Power Consumption	3.5A@12V (Max.) with i7-2710QE
Power Requirement	DC 12V input only
Certification	CE, FCC class B
Operation Temp.	-20°C ~ 70°C (-4°F ~ 158°F)
Storage Temp.	-20°C ~ 80°C (-4°F ~ 176°F)
Humidity	0% ~ 95% (non-condensing)
Dimension (L x W)	170 x 170 mm (6.7" x 6.7")

1.12 Board Dimensions

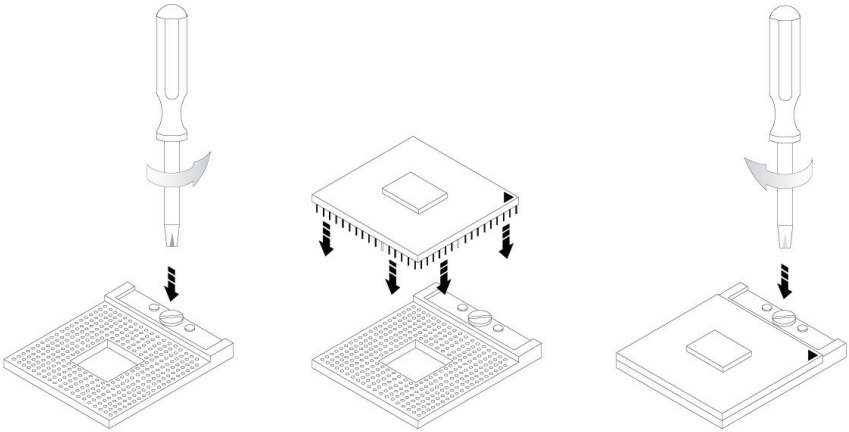




1.13 Installing the CPU

The processor socket comes with a screw to secure the CPU. As shown in the picture bellow, loose the screw first before inserting the CPU.

Place the CPU into the socket by making sure the notch on the corner of the CPU correspond to the notch on the inside of the socket. Once the CPU slides into the socket, lock the screw.



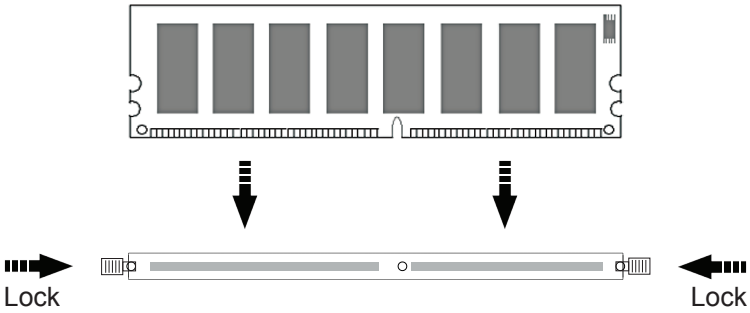
Make sure that heatsink is in complete contact with top surface of the CPU to avoid the CPU's overheating problem.

If not, it would cause your system or CPU to be hanged, unstable, damaged.

1.14 Installing the Memory

To install the memory module, locate the vertical SO-DIMM slot on the board and perform these procedures:

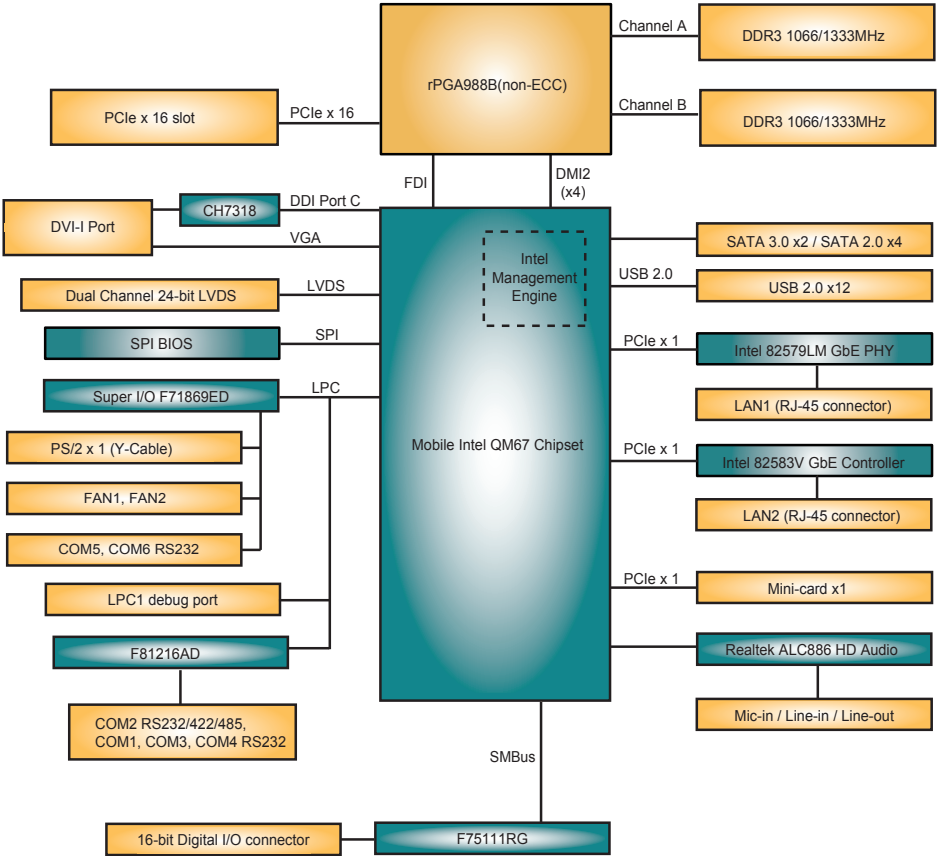
1. Hold the memory module and align key of the memory module with those on the vertical SO-DIMM slot.
2. Gently push the memory module uprightly in a right way so that clips of the vertical SO-DIMM slot may close to lock the memory module in place. Push until the memory module touches the bottom of the vertical SO-DIMM slot.
3. To remove the memory module, just press the clips of vertical SO-DIMM slot with both hands.



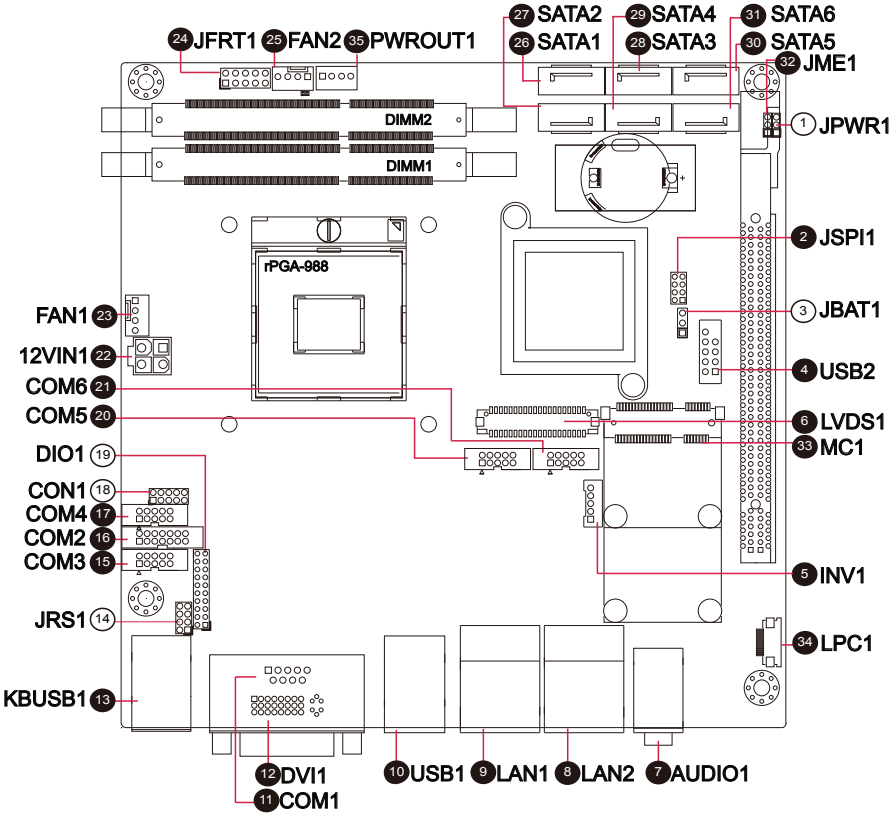
Chapter 2

Installation

2.1 Block Diagram



2.2 Jumpers and Connectors



Jumpers

Jumper Settings

The jumper is “short” (closed) when the jumper cap is placed on pins. If not, that means the jumper is “open.”


Pin open

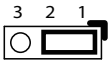
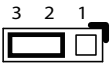

Pin short (closed)

Pin 2-3 short (closed)

Pin 1-2 short (closed)

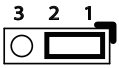
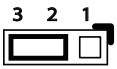
JPWR1: AT/ATX Power Mode Selection (1)

Connector type: 2.00mm pitch 1x3-pin header.

Pin	Power Mode Selection	
1-2	ATX Mode (Default)	
2-3	AT Mode	

JBAT1: Clear CMOS Setting (3)

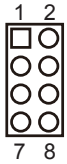
Connector type: 2.00mm pitch 1x3-pin header.

Pin	Mode	
1-2	Keep CMOS data (Default)	
2-3	Clear CMOS data	

JRS1: COM2 RS-232 / 422 / 485 Selection (14)

Connector type: 2.00mm pitch 2x4-pin header

	Assignment		
Pin	RS-232 (Default)	RS-422	RS-485
1-2	Short	Open	Open
3-4	Open	Short	Open
5-6	Open	Open	Short
7-8 **	Short	Short	Open/Short



** 485 Auto-Flow selection, OFF: Enable, ON: Disable

CON1: COM3/4 Power Source Select on Pin 9 (18)

Connector type: 2.00mm pitch 2x5-pin header
Default setting: Standard

Pin 9 Power Source Special Support	COM3 CON1	COM4 CON1
Standard (RI) (Default)	7-9	8-10
POS: 12V/1A on Pin 9	1-3	2-4
POS: 5V/1A on Pin 9	3-5	4-6

JME1: ME Function Select (32)

Connector type: 2.00mm pitch 1x3-pin header

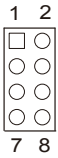
Pin	Power Mode Selection	
1-2	ME Enable/ME Flash disable (Default)	
2-3	ME Disable/ME Flash enable	

Connectors

JSPI1: SPI Flash for External SPI Programming Tools (2)

Connector type: 2.54mm pitch 2x4-pin header

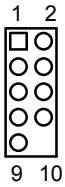
Pin	Desc.	Pin	Desc.
1	V_3P3_SPI	2	GND
3	SPI_CS0_R	4	SPI_CLK_R
5	SPI_SO_R	6	SPI_SI_R
7	NC	8	NC



USB2: USB Port Connector (4)

Connector type: 2.54mm pitch 2x5-pin header.

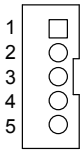
Pin	Description	Pin	Description
1	+5V	2	+5V
3	USBD2-	4	USBD3-
5	USBD2+	6	USBD3+
7	GND	8	GND
9	GND	10	N/C (Key)



INV1: LCD Inverter Connector (5)

Connector type: 2.00mm pitch 1x5 box wafer connector.

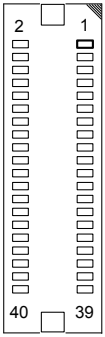
Pin	Description
1	+12V
2	GND
3	Backlight on/off
4	Brightness control
5	GND



LVDS1: LVDS Connector (6)

Connector type: DF-13-40DP-1.25V connector.

Pin	Description	Pin	Description
2	VCC3	1	VCC3
4	GND	3	GND
6	VCC5	5	VCC5
8	GND	7	GND
10	LVDSA_DATA1-	9	LVDSA_DATA0-
12	LVDSA_DATA1	11	LVDSA_DATA0
14	GND	13	GND
16	LVDSA_DATA3-	15	LVDSA_DATA2-
18	LVDSA_DATA3	17	LVDSA_DATA2



20	GND	19	GND
22	LVDSB_CLK-	21	LVDSA_CLK-
24	LVDSB_CLK	23	LVDSA_CLK
26	GND	25	GND
28	LVDSB_DATA1-	27	LVDSB_DATA0-
30	LVDSB_DATA1	29	LVDSB_DATA0
32	GND	31	GND
34	LVDSB_DATA3-	33	LVDSB_DATA2-
36	LVDSB_DATA3	35	LVDSB_DATA2
38	GND	37	GND
40	NC	39	GPIO

AUDIO1: Audio Interface Port (7)

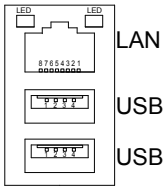
Connector type: triple stacked audio jacks (Stereo ø3.50).

LAN1, 2: Ethernet Connectors (include USB0/1/2/3 Connector) (9, 8)

Connector type: RJ-45 + double stacked USB type A connector.

LAN (RJ-45)

Pin	Description
1	MDI0+
2	MDI0-
3	MDI1+
4	MDI1-
5	MDI2+
6	MDI2-
7	MDI3+
8	MDI3-

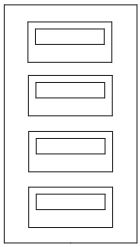


USB (USB type A connector)	
Pin	**Description**
1	+5V
2	USB-
3	USB+
4	GND

USB1: 4 x USB Port Connector (10)

Connector type: 4 stack USB type A connector.

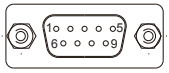
Pin	Description	Pin	Description
11	5V	21	5V
12	USBD1-	22	USBD2-
13	USBD1+	23	USBD2+
14	GND	24	GND
31	5V	41	5V
32	USBD3-	42	USBD4-
33	USBD3+	43	USBD4+
34	GND	44	GND
G1	GND	G4	GND
G2	GND	G5	GND
G3	GND	G6	GND



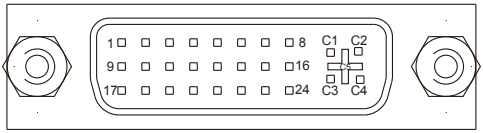
COM1: RS-232 Connector (11)

Connector type: D-sub 9-pin male connector

Pin	Desc.	Pin	Desc.
1	DCD	6	DSR
2	RX	7	RTS
3	TX	8	CTS
4	DTR	9	RI
5	GND	10	NC



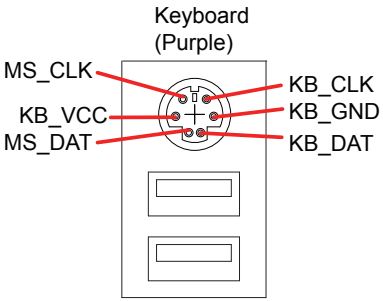
DVI1: DVI-I Connector (12)



Pin	Description	Pin	Description	Pin	Description
1	TX2-	13	N/C	C1	Analog RED
2	TX2+	14	+5V/50mA	C2	Analog Green
3	TX2/4GND	15	GND	C3	Analog Blue
4	N/C	16	HTPLG	C4	Analog V_SYNC
5	N/C	17	TX0-	C5	Analog R, G, B Return
6	DDC_CLK	18	TX0+		
7	DDC_DATA	19	TX0/5GND		
8	CRT_Vsync	20	N/C		
9	TX1-	21	N/C		
10	TX1+	22	TXC_GND		
11	TX1/3GND	23	TXC+		
12	N/C	24	TXC-		

KBUSB1: PS/2 Keyboard and USB x 2 (13)

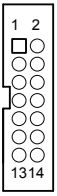
Connector type: PS/2 Keyboard + USB connector.



COM2: Serial Port Connector (16)

Connector type: 2.00mm pitch 2x7-pin box header

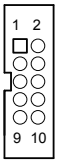
Pin	Desc.	Pin	Desc.
1	DCD2	2	RXD2
3	TXD2	4	DTR2
5	GND	6	DSR2
7	RTS2	8	CTS2
9	RI2	10	NC
11	422TX+_485+	12	422TX-_485-
13	422RX+	14	422RX-



COM3~6: Serial Port Connectors (15, 17, 20, 21)

Connector type: 2.00mm pitch 2x5-pin box header

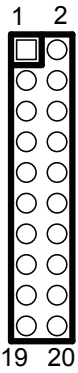
Pin	Desc.	Pin	Desc.
1	DCD1	2	RXD1
3	TXD1	4	DTR1
5	GND	6	DSR1
7	RTS1	8	CTS1
9	RI1	10	NC



DIO1: DIO Port (19)

Connector type: 2.00mm pitch 2x10-pin header

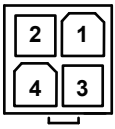
Pin	Desc.	Pin	Desc.
1	DIO0	2	DIO1
3	DIO2	4	DIO3
5	DIO4	6	DIO5
7	DIO6	8	DIO7
9	DIO8	10	DIO9
11	DIO10	12	DIO11
13	DIO12	14	DIO13
15	DIO14	16	DIO15
17	5V	18	GND
19	5V	20	GND



12VIN1: ATX12V Connector (22)

12INV1 supplies the CPU operation ATX +12V (Vcore).

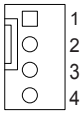
Pin	Description	Pin	Description
2	GND	1	GND
4	+12V	3	+12V



FAN1, 2: Fan Connectors (23, 25)

Connector type: 2.54mm pitch 1x4-pin wafer connector.

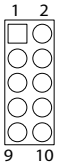
Pin	Description
1	GND
2	+12V
3	FAN_Detect
4	Control



JFRT1: Switches and Indicators (24)

It provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status.
Connector type: 2.54mm pitch 2x5-pin header.

Pin	Description	Pin	Description
1	RESET+	2	RESET-
3	POWER_LED+	4	POWER_LED-
5	HDD_LED+	6	HDD_LED-
7	SPEAKER+	8	SPEAKER-
9	PSON+	10	PSON-



PWROUT1: SATA Power Connector (35)

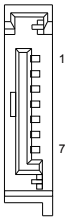
Connector type: 2.50mm pitch 1x4-pin wafer connector.

Pin	Description
1	5V
2	GND
3	GND
4	12V_FAN2

SATA1~6: Serial ATA Connectors (26~31)

High speed transfer rates (150MB/s).

Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

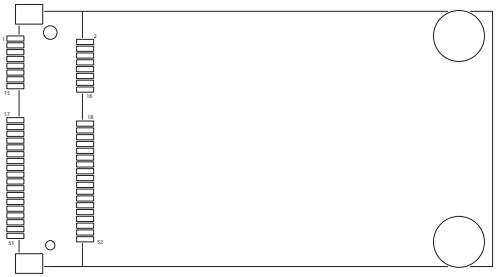


LPC1: Low Pin Count Connector (34)

Connector type: CVILUX 0.5mm CF20141U0*0-LF connector

Pin	Desc.	Pin	Desc.
1	LPC_D0	8	LPC_RST#
2	LPC_D1	9	GND
3	LPC_D2	10	LPC_CLK_33Mhz
4	LPC_D3	11	GND
5	GND	12	GND
6	LPC_FRAME#	13	+3.3V
7	SERIRQ	14	+3.3V

MC1: Mini-card Slot (33)



Pin	Desc.	Pin	Desc.
1	Wake	2	+3.3V
3	COEX1	4	GND
5	COEX2	6	+1.5V
7	CLKREQ#	8	UIM_PWR
9	GND	10	UIM_DATA
11	REFCLK-	12	UIM_CLK
13	REFCLK+	14	UIM_RESET
15	GND	16	UIM_VPP
17	UIM_C8/Reserved	18	GND
19	UIM_C4/Reserved	20	W_Disable#
21	GND	22	PERST#
23	PERn0	24	+3.3V
25	PERp0	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3V	40	GND
41	+3.3V	42	LED_WWAN#
43	GND	44	LED_WLAN#
45	Reserved	46	LED_WPAN#
47	Reserved	48	+1.5V
49	Reserved	50	GND
51	Reserved	52	+3.3V

2.3 The Installation Paths of CD Driver

Windows XP

Driver	Path
CHIPSET	\CHIPSET\INTEL\INF 9.2.0.1021
NET Framework	\NET Framework\NET Framework 3.5
ME	\ME\AMT_INTEL_V7.0.0.1109
GRAPHICS	\GRAPHICS\INTEL\Winxp_14464
LAN	\ETHERNET\INTEL\82583V\WIN_allos_ Ver16.3
AUDIO	\AUDIO\Realtek_HD\XP_2000 WDM_R261 32_64 bit

Windows 7

Driver	Path
CHIPSET	\CHIPSET\INTEL\INF 9.2.0.1021
ME	\ME\AMT_INTEL_V7.0.0.1109
GRAPHICS	\GRAPHICS\INTEL_Win7_32\2291 \GRAPHICS\INTEL_Win7_64\2291
LAN	\ETHERNET\INTEL\82583V\WIN_allos_ Ver16.3
AUDIO	\AUDIO\Realtek_HD\Vista_Win7_R261-32_64 bit

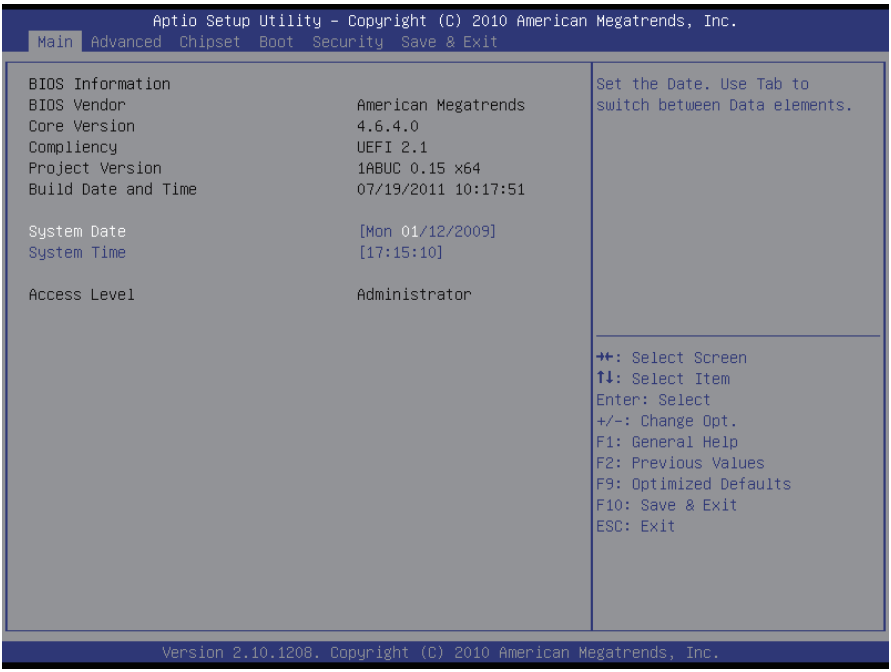
Chapter 3

BIOS

3.1 BIOS Main Setup

The AMI BIOS provides a setup utility program for specifying the system configurations and settings which are stored in the BIOS ROM of the system. When you turn on the computer, the AMI BIOS is immediately activated. After you have entered the setup utility, use the left/right arrow keys to highlight a particular configuration screen from the top menu bar or use the down arrow key to access and configure the information below.

NOTE: In order to increase system stability and performance, our engineering staff are constantly improving the BIOS menu. The BIOS setup screens and descriptions illustrated in this manual are for your reference only, and may not completely match what you see on your screen.



BIOS Information

Display the BIOS information.

System Date

Set the system date. Note that the 'Day' automatically changes when you set the date.

The date format is:

Day : Sun to Sat
Month : 1 to 12
Date : 1 to 31
Year : 1999 to 2099

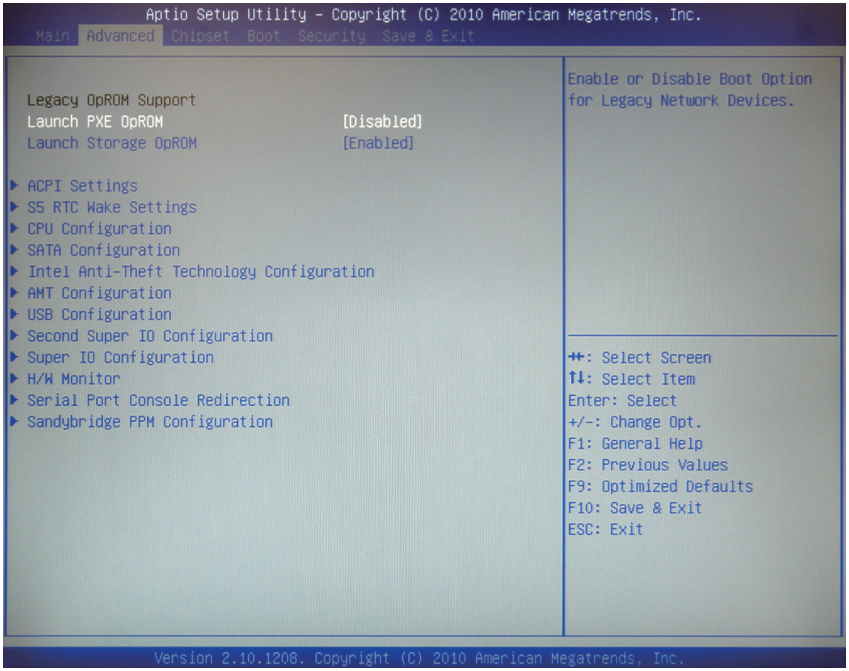
System Time

Set the system time.

The time format is:

Hour : 00 to 23
Minute : 00 to 59
Second : 00 to 59

3.2 Advanced Settings



Legacy OpROM Support

Launch PXE OpROM

Enable or disable the boot option for legacy network devices.

Launch Storage OpROM

Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.

ACPI Settings

Enable/disable the Advanced Configuration and Power Interface (ACPI).

S5 RTC Wake Settings

Enable system to wake from S5 using RTC alarm.

CPU Configuration

This section is used to configure the CPU. It will also display detected CPU information.

SATA Configuration

This section is used to configure the SATA drives.

Intel Anti-Theft Technology Configuration

Configure the Intel® Anti-Theft Technology function.

AMT Configuration

Configure Active Management Technology parameters.

USB Configuration

Configure the USB devices.

Second Super IO Configuration

This section is used to configure the 2nd I/O functions supported by the onboard Super I/O chip.

Super IO Configuration

This section is used to configure the I/O functions supported by the onboard Super I/O chip.

H/W Monitor

This section is used to configure the hardware monitoring events, such as temperature, fan speed and voltages.

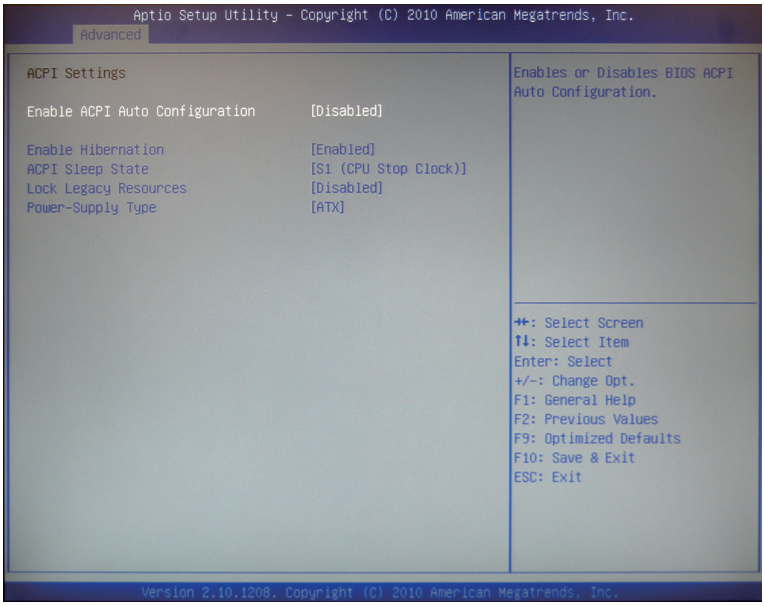
Serial Port Console Redirection

The section allows to configure console redirection options. Console redirection further allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.

Sandybridge PPM Configuration

Configure periodic permanent magnetic (PPM).

3.2.1 ACPI Settings



Enable ACPI Auto Configuration

This item allows you to enable/disable ACPI (Advanced Configuration and Power Interface) Auto Configuration.
Setting: Disabled (Default), Enabled.

Enable Hibernation

Enable or disable the Hibernation function. This allows the operating system to control power to the computer's disk, monitor and peripheral devices.
Setting: Enabled (Default), Disabled

ACPI Sleep State

This item allows you to select ACPI Sleep State.
ACPI sleep state enables you to send the system in a low-power consuming sleep mode.

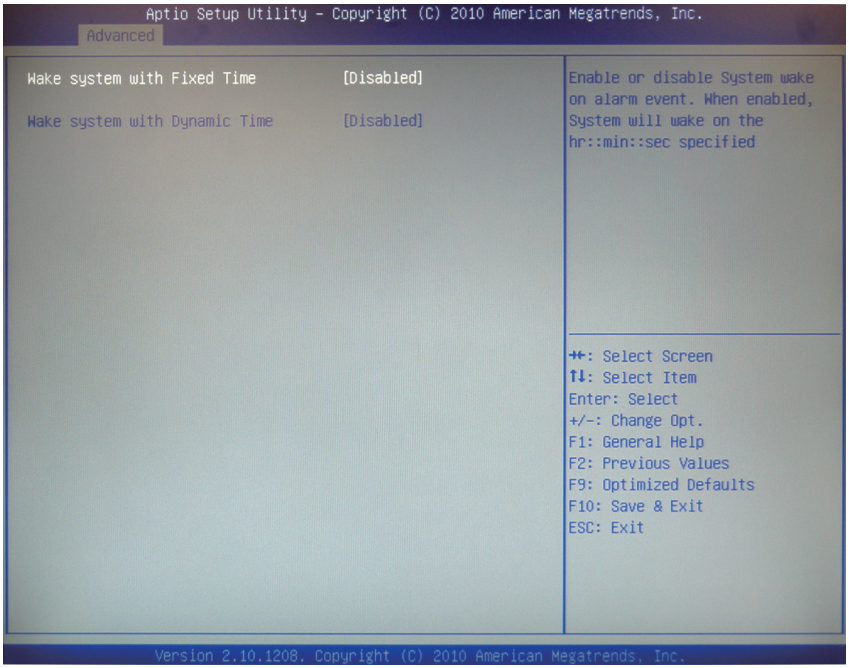
Lock Legacy Resources

Enable or Disable system lock of legacy resources.

Power-Supply Type

Setting: AT (Default), ATX.

3.2.2 S5 RTC Wake Settings



Wake System with Fixed Time

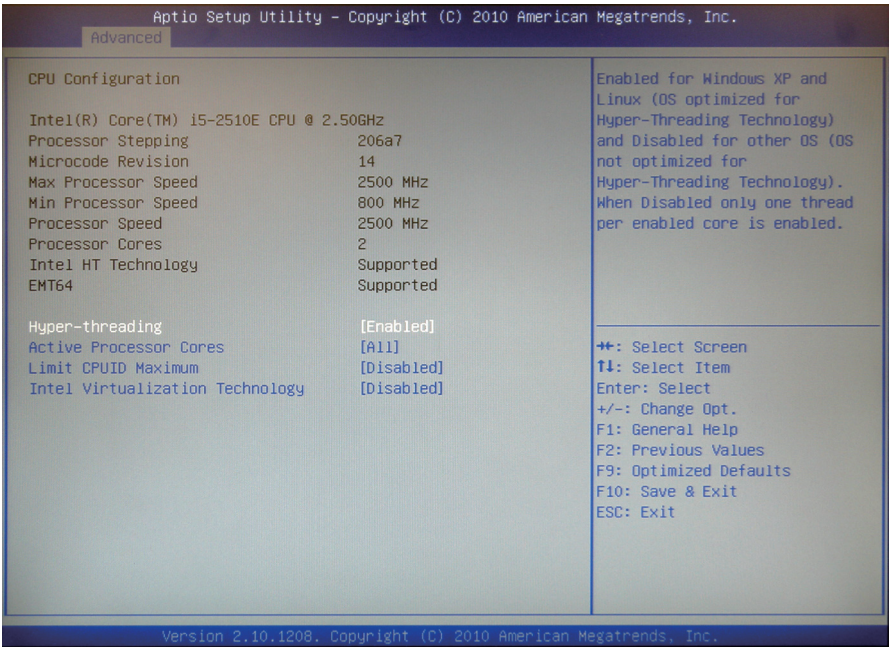
Enable or disable system wake on alarm event. When enabled, system will wake on the hr::min::sec specified.

Wake System with Dynamic Time

Enable or disable system wake on alarm event. When enabled, system will wake on the current time + Increase minute(s).

3.2.3 CPU Configuration

The CPU Configuration setup screen varies depending on the installed processor.



Hyper-threading

This item is used to enable or disable the processor's Hyper-threading feature.

Enabled for Windows XP and Linux (OS optimized for Hyper-threading Technology) and disabled for other OS (OS not optimized for Hyper-threading Technology).

When disabled, only one thread per enabled core is enabled.

Active Processor Cores

Number of cores to enable in each processor package.

Limit CPUID Maximum

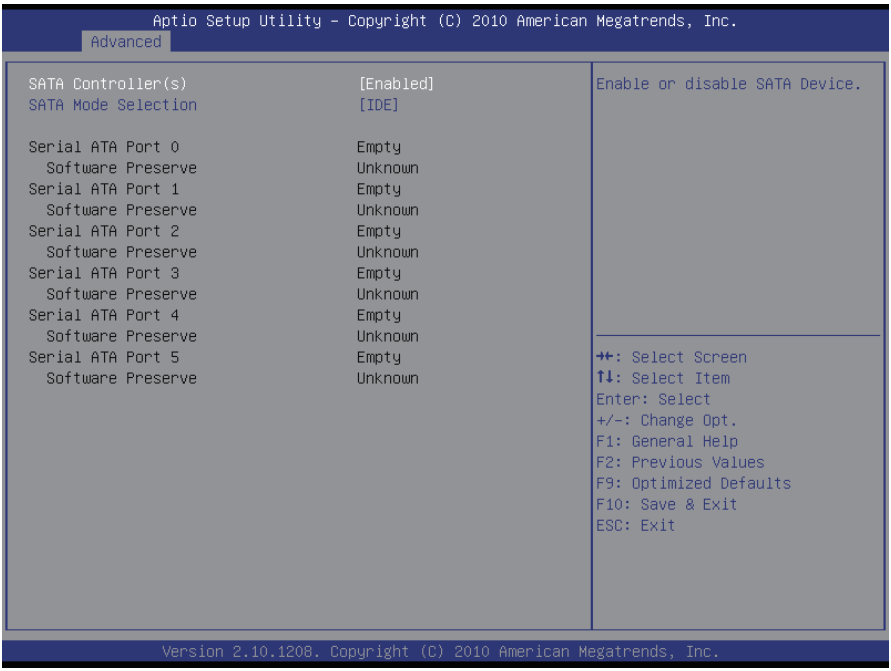
Enable or disable the Limit CPUID Maximum.

Intel Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

3.2.4 SATA Configuration

It allows you to select the operation mode for SATA controller.



SATA Controller(s)

Enable or disable SATA devices.

SATA Mode Selection

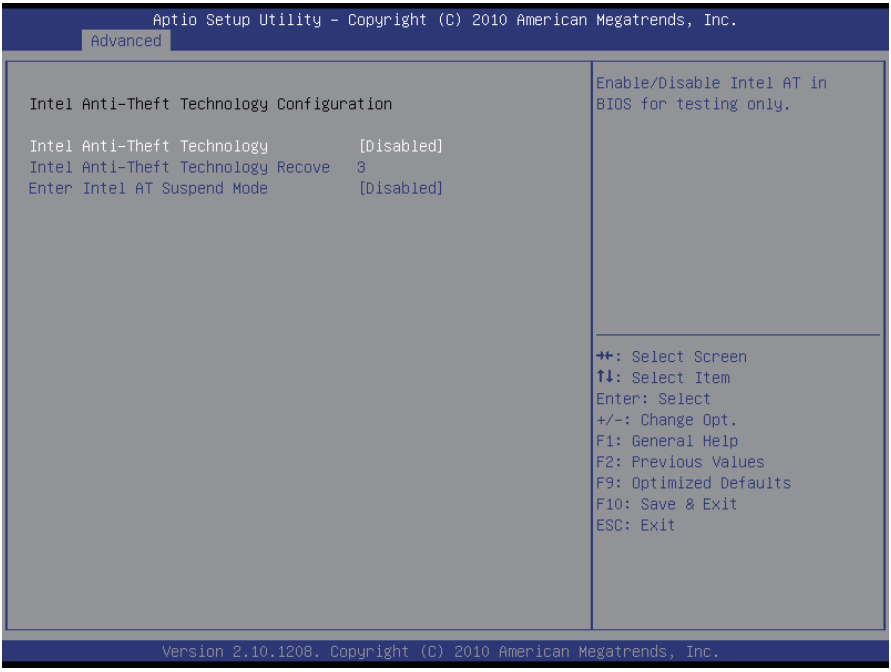
The choice: Disable; IDE (Default), AHCI, RAID

IDE: Set the Serial ATA drives as Parallel ATA storage devices.

AHCI: Allow the Serial ATA devices to use AHCI (Advanced Host Controller Interface).

RAID: Create RAID or Intel Matrix Storage configuration on Serial ATA devices.

3.2.5 Intel Anti-Theft Technology Configuration



Intel Anti-Theft Technology

Enable or disable Intel® Anti-Theft Technology function in BIOS.

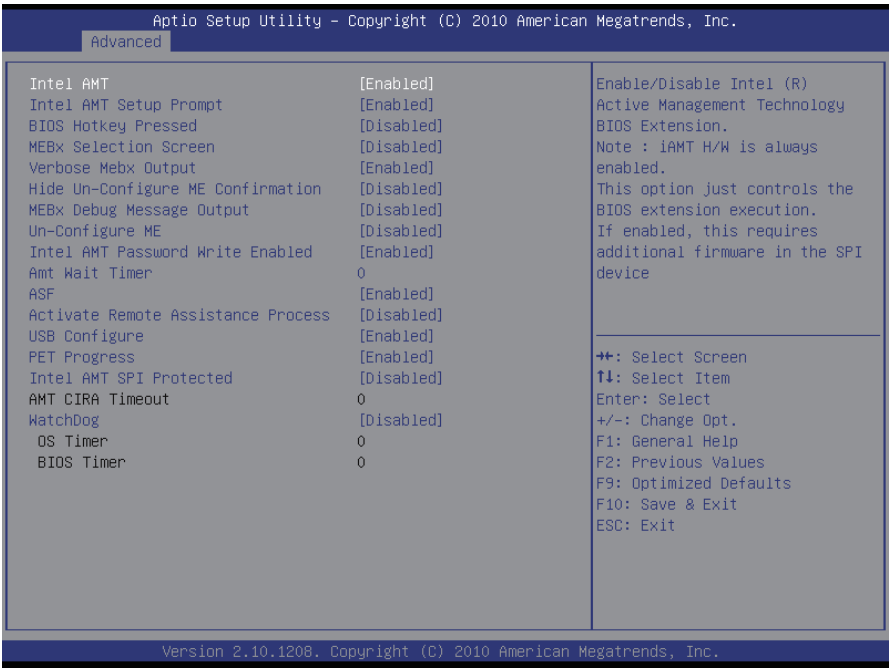
Intel Anti-Theft Technology Recovery

Set the number of times recovery attempted will be allowed.

Enter Intel AT Suspend Mode

Enable or disable the request that platform enters AT suspend mode.

3.2.6 AMT Configuration



Intel AMT

Enable/Disable Intel® Active Management Technology BIOS Extension. NOTE: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

Intel AMT Setup Prompt

OEMFLag Bit 0:
Enable/Disable Intel AMT Setup Prompt to wait for hot-key to enter setup.

BIOS Hotkey Pressed

OEMFLag Bit 1:
Enable/Disable BIOS hotkey press.

MeBx Selection Screen

OEMFLag Bit 2:
Enable/Disable MEBx selection screen.

Verbose Mebx Output

OEMFLag Bit 3:
Enable/Disable Verbose Mebx Output.

Hide Un-Configure ME Confirmation

OEMFLag Bit 6:
Hide Un-Configure ME without password Confirmation Prompt.

MeBx Debug Message Output

OEMFLag Bit 14:
Enable MEBx debug message output.

Un-Configure ME

OEMFLag Bit 15:
Un-Configure ME without password.

Intel AMT Password Write Enabled

Enable/Disable Intel AMT Password Write. Password is writable when set Enable.

Amt Wait Timer

Set timer to wait before sending ASF_GET_BOOT_OPTIONS.

ASF

Enable/Disable Alert Specification Format.

Activate Remote Assistance Process

Trigger CIRA boot.

USB Configure

Enable/Disable USB Configure function.

PET Progress

User can enable/disable PET Events progress to received PET events or not.

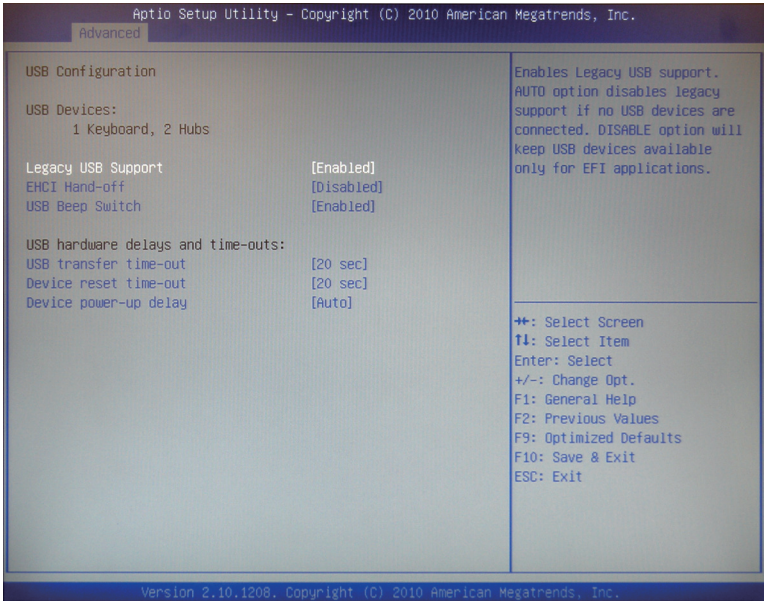
Intel Amt SPI Protected

Enable/Disable Intel AMT SPI write protect.

WatchDog

Enable/Disable WatchDog Timer.

3.2.7 USB Configuration



Legacy USB Support

Enable support for legacy USB. AUTO option disables legacy support if no USB devices are connected.
The choice: Enabled (Default); Auto; Disabled

EHCI Hand-Off

Allow you to enable support for operating systems without an EHCI hand-off feature. Do not disable the BIOS EHCI Hand-off option if you are running a Windows® operating system with USB device.
The choice: Enabled (Default); Disabled

USB Beep Switch

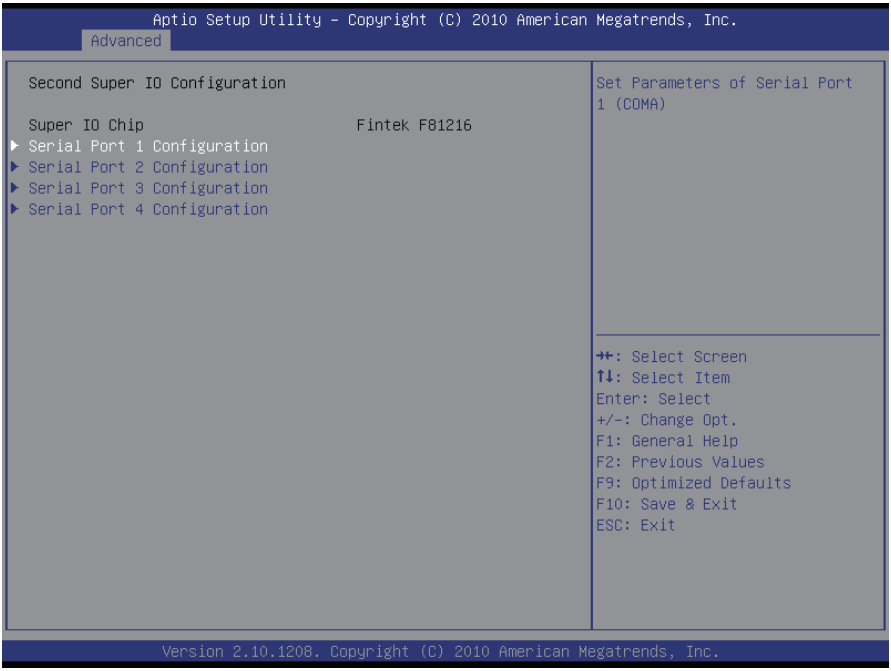
Enable/Disable USB Beep sound.

USB hardware delays and time-outs

USB transfer time-out — The time-out value for control, bulk, and interrupt transfers. Default setting: 20 sec
Device reset time-out — USB mass storage device start unit command time-out. Default setting: 20 sec
Device power-up delay — Maximum time the device will take before it properly reports itself to the host controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from hub descriptor. The choice: Auto (Default); Manual

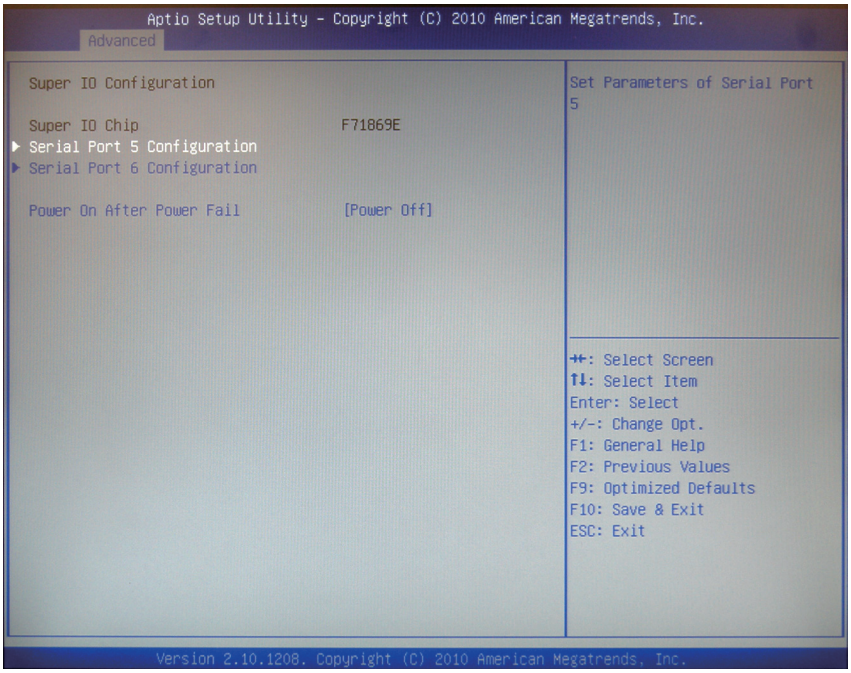
3.2.8 Second Super IO Configuration

You can use this item to set up or change the Second Super IO configuration for FDD controllers, parallel ports and serial ports.



3.2.9 Super IO Configuration

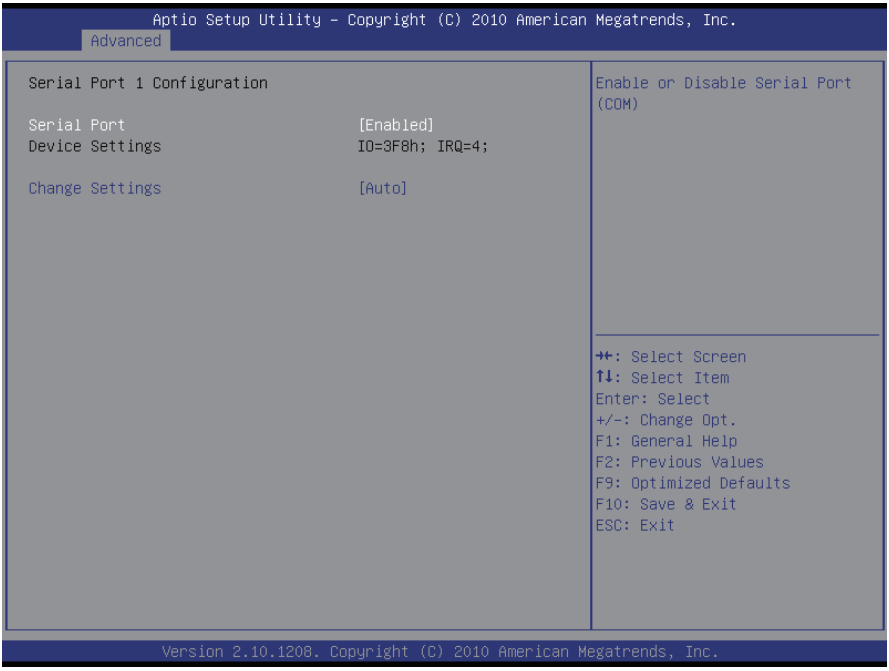
You can use this item to set up or change the Super IO configuration for FDD controllers, parallel ports and serial ports.



Power On After Power Fail

Specify what state to go to when power is re-applied after a power failure.

Serial Port Configuration



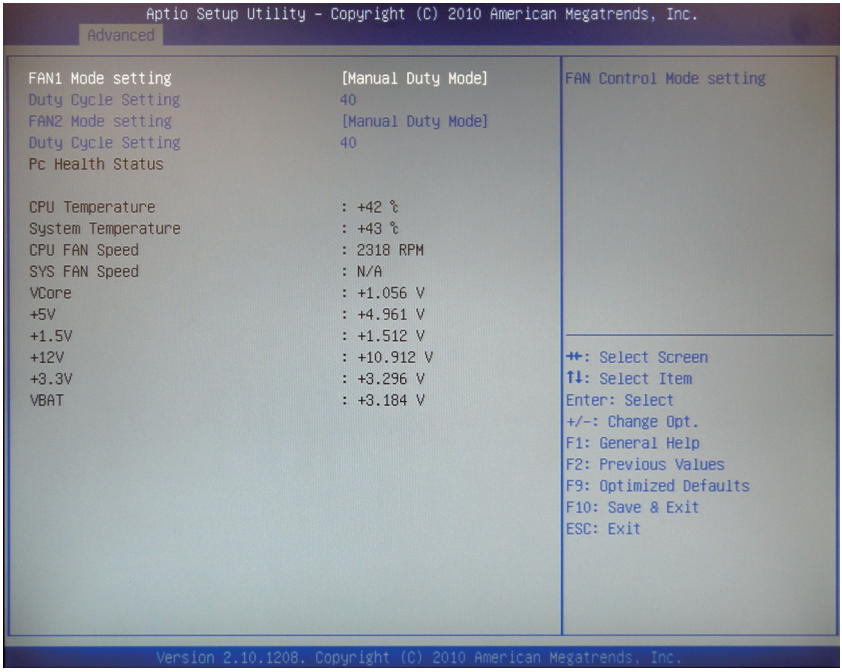
Serial Port

Use the Serial port option to enable or disable the serial port.
The choice: Enabled, Disabled

Change Settings

Use the Change Settings option to change the serial port's IO port address and interrupt address.
The choice:
Auto
IO=3F8h; IRQ=4,
IO=3F8h; IRQ=3,4,5,6,7,10,11,12
IO=2F8h; IRQ=3,4,5,6,7,10,11,12
IO=3E8h; IRQ=3,4,5,6,7,10,11,12
IO=2E8h; IRQ=3,4,5,6,7,10,11,12

3.2.10 H/W Monitor



FAN1~2 Mode Setting

Allow you to select FAN control mode.

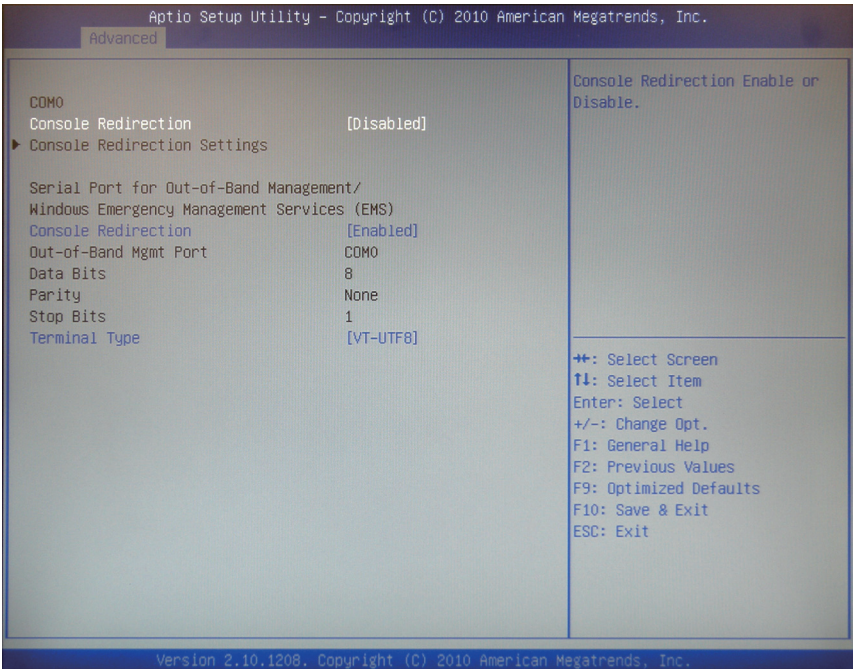
Duty Cycle Setting

Set Fan at fixed Duty-Cycle, Min=0% Max=100%, please input Dec number.

PC Health Status

The hardware monitor menu shows the operating temperature, fan speeds and system voltages.

3.2.11 Serial Port Console Redirection



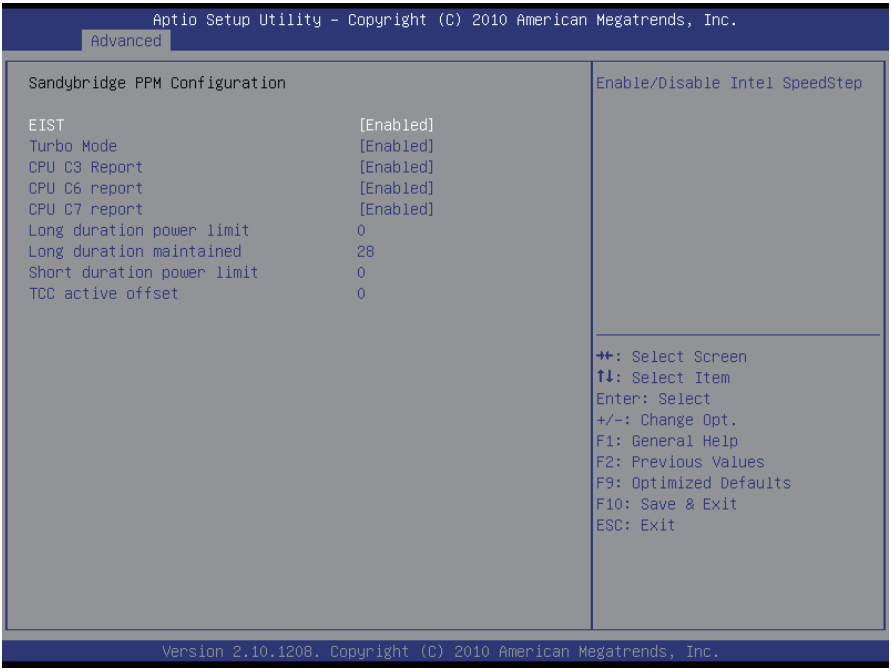
Console Redirection

Console Redirection Enable or Disable.

Terminal Type

VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100.

3.2.12 Sandybridge PPM Configuration



EIST

Enable/Disable Intel SpeedStep.

Turbo Mode

Enable/Disable Turbo Mode.

CPU C3 Report

Enable/Disable CPU C3(ACPI C2) report to OS.

CPU C6 Report

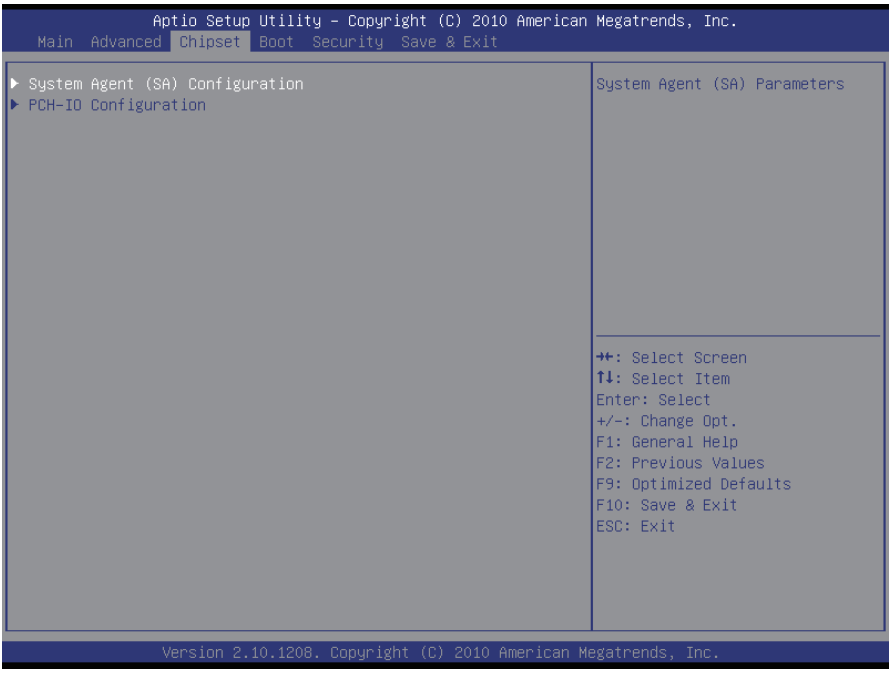
Enable/Disable CPU C6(ACPI C3) report to OS.

CPU C7 Report

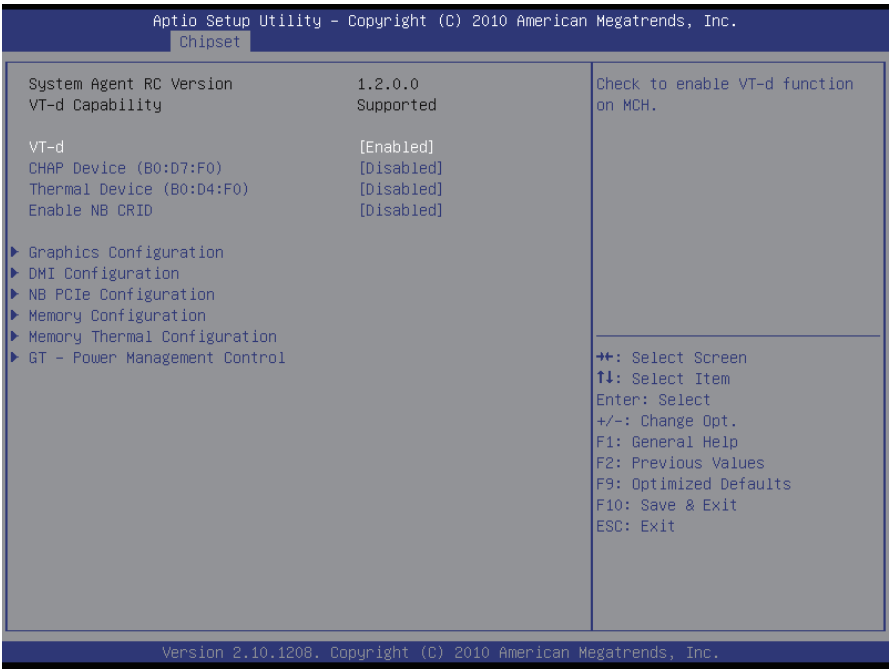
Enable/Disable CPU C7(ACPI C3) report to OS.

3.3 Chipset

This section allows you to configure and improve your system; also, set up some system features according to your preference.



3.3.1 System Agent (SA) Configuration



VT-d

Enable VT-d function on MCH.

CHAP Device (B0:D7:F0)

Enable or disable SA CHAP Device.

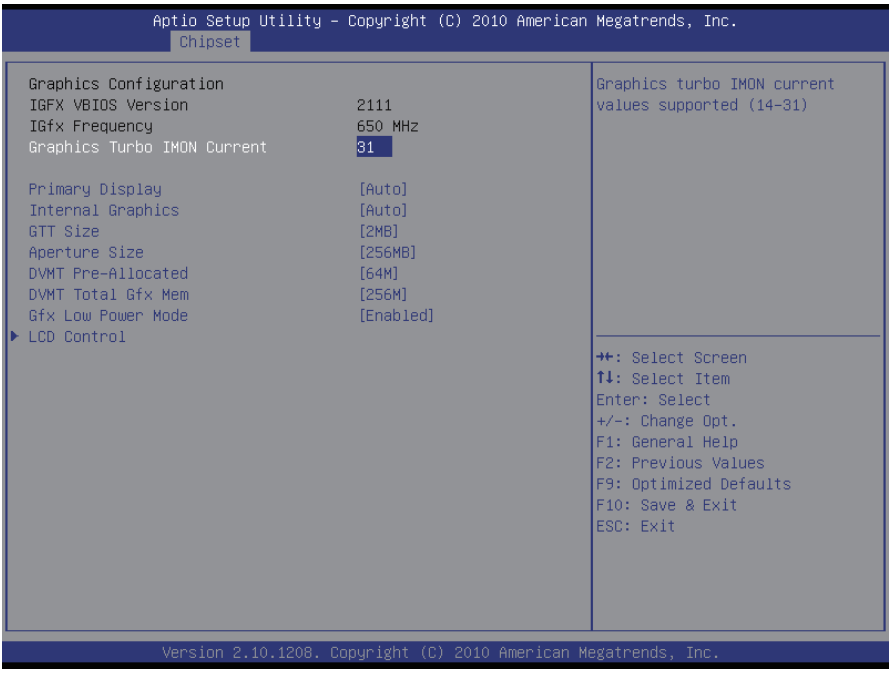
Thermal Device (B0:D4 F0)

Enable or disable SA Thermal Device.

Enable NB CRID

Enable or disable NB CRID WorkAround.

Graphics Configuration



Primary Display

Select which of IGFX/PEG/PCI Graphics Devices should be Primary Display or select SG for Switchable Gfx.

Internal Graphics

Keep IGD enabled based on the option.

GTT Size

Select the GTT Size: 1MB, 2MB.

Aperture Size

Select the Aperture Size: 128MB, 256MB, 512MB.

DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device: 0M~512M.

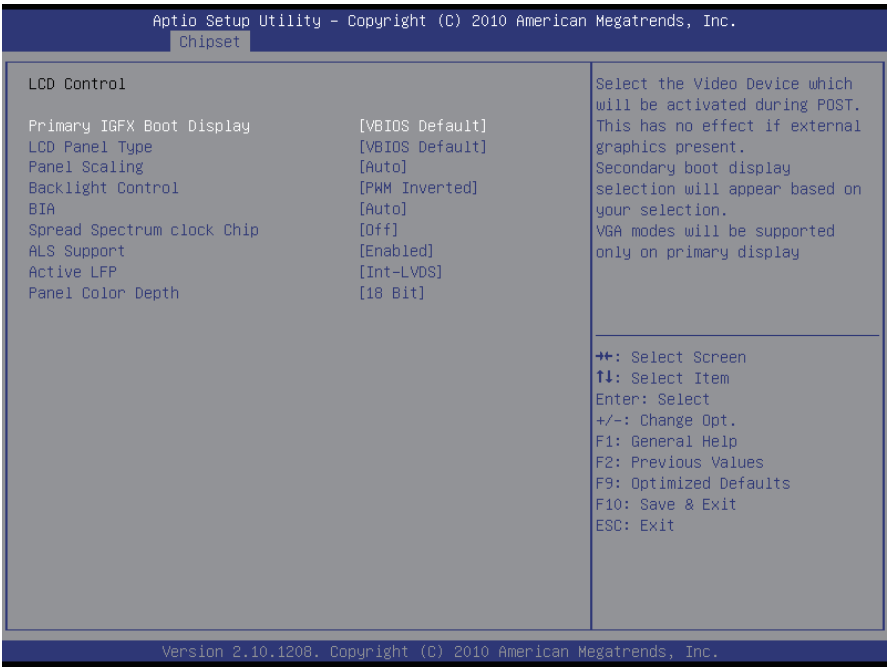
DVMT Total Gfx Mem

Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device: 128M, 256M, MAX.

Gfx Low Power Mode

This option is applicable for SFF only.

LCD Control



Primary IGFX Boot Display

Select the Video Device which will be activated during POST. This has no effect if external graphics present.
Secondary boot display selection will appear based on your selection.
VGA modes will be supported only on primary display.

LCD Panel Type

Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item: VBIOS Default, 640x480 LVDS ~ 2048x1536 LVDS.

Panel Scaling

Select the LCD panel scaling option used by the Internal Graphics Device: Auto, Off, Force Scaling.

Backlight Control

The choice: PWM Inverted (Default), PWM Normal, GMBus Inverted and GMBus Normal.

BIA

The choice: VBIOS Default, Disabled and Level 1/2/3/4/5.

Spread Spectrum clock Chip

The default setting is Off. Other options are:
Hardware: Spread is controlled by chip.
Software: Spread is controlled by BIOS.

ALS Support

Enabled or Disabled. Valid only for ACPI.
Legacy = ALS support through the IGD INT10 function.
ACPI = ALS support through an ACPI ALS driver.

Active LFP

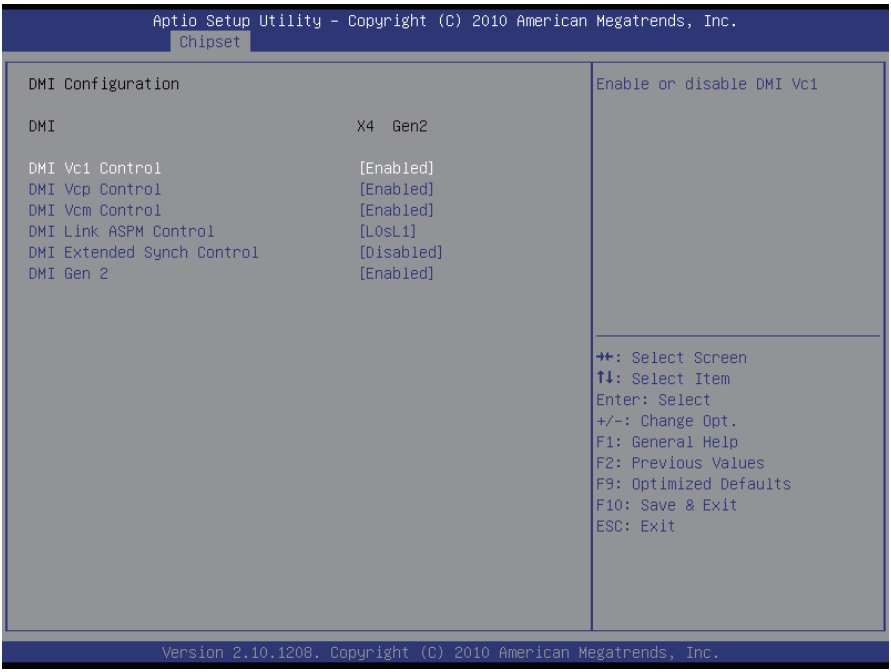
Select the Active LFP Configuration.
No LVDS: VBIOS does not enable LVDS.
Int-LVDS: VBIOS enables LVDS driver by Integrated encoder.
SDVO LVDS: VBIOS enables LVDS driver by SDVO encoder.
eDP Port-A: LFP driven by Int-DisplayPort encoder from Port-A.

Panel Color Depth

Select the LFP panel color depth: 18 Bit, 24 Bit.

DMI Configuration

Control various DMI functions.



DMI Vc1/Vcp/Vcm Control

Enable or disable DMI Vc1/Vcp/Vcm.

DMI Link ASPM Control

Enable or disable the control of Active State Power Management on SA side of the DMI Link.
The choice: Disabled, L0s, L1, L0sL1

DMI Extended Synch Control

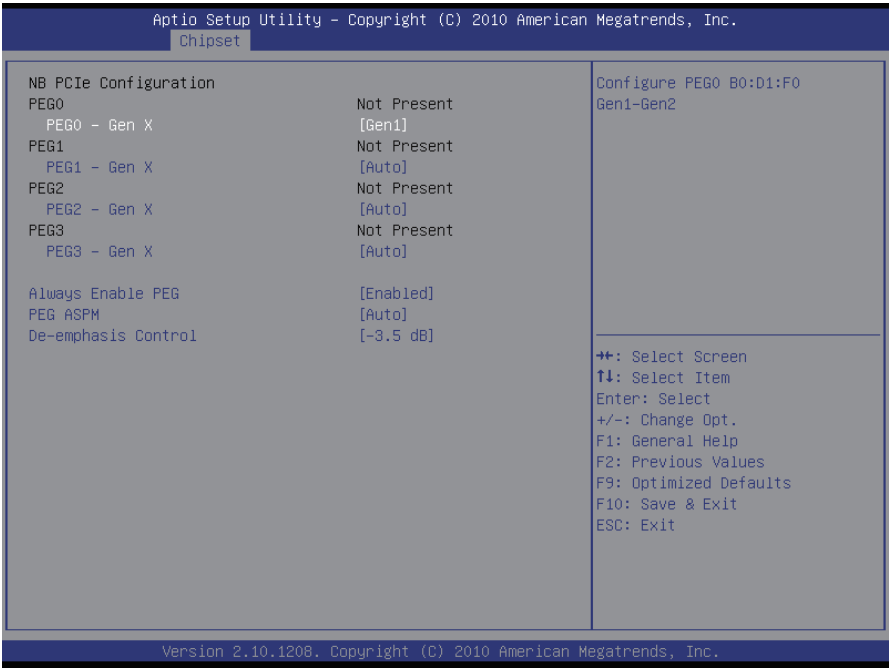
Enable or disable DMI Extended Synchronization.

DMI Gen 2

Enable or disable DMI Gen 2.

NB PCIe Configuration

Configure NB PCIe Express Settings.



PEG0 – Gen X

Configure PEG0 B0:D1:F0 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

PEG1 – Gen X

Configure PEG1 B0:D1:F1 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

PEG2 – Gen X

Configure PEG2 B0:D1:F2 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

PEG3 – Gen X

Configure PEG3 B0:D6:F0 Gen1-Gen2.
The choice: Auto, Gen1, Gen2

Always Enable PEG

Enable the PEG slot.

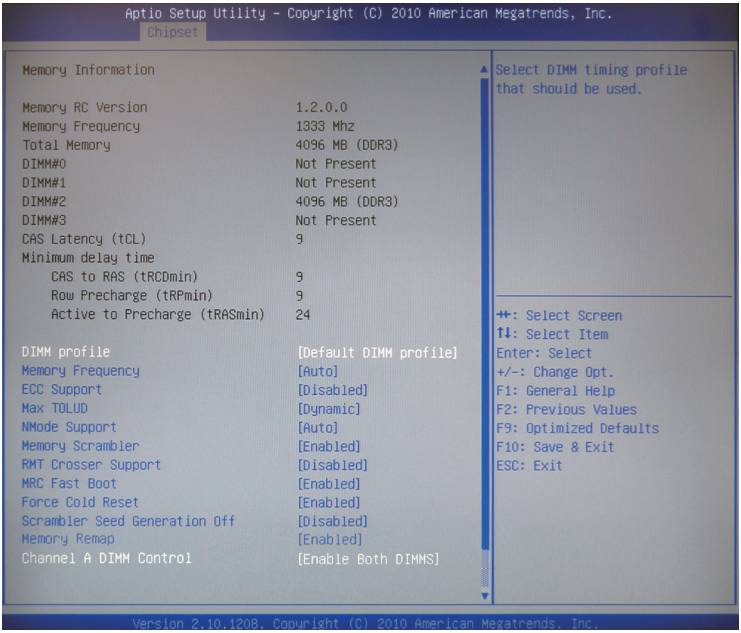
PEG ASPM

Control ASPM support for the PEG Device. This has no effect if PEG is not the currently active device.
The choice: Disabled, Auto, ASPM L0s, ASPM L1, ASPM L0sL1

De-emphasis Control

Configure the De-emphasis control on PEG.
The choice: -6 dB, -3.5 dB

Memory Configuration



DIMM profile

Select DIMM timing profile that should be used.
The choice: Default DIMM profile, XMP profile 1, XMP profile 2

Memory Frequency

Maximum Memory Frequency Selections in Mhz.
The choice: Auto, 1067, 1333, 1600, 1867, 2133

ECC Support

Enable or disable DDR Ecc Support.

Max TOLUD

Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.
The choice: Dynamic, 1GB, 1.25 GB, 1.5 GB, 1.75 GB, 2GB, 2.25 GB, 2.5 GB, 2.75 GB, 3 GB, 3.25 GB

NMode Support

NMode Support Option.
The choice: Auto, 1 N Mode, 2 N Mode

Memory Scrambler

Enable or disable Memory Scrambler support.

RMT Crosser Support

Enable or disable RmtCrosserEnable support.

MRC Fast Boot

Enable or disable MRC fast boot.

Force Cold Reset

Force cold reset or choose MRC cold reset mode, when cold boot is required during MRC execution.
NOTE: If ME 5.0MB is present, Force cold reset is required!

Scrambler Seed Generation Off

Control Memory Scrambler Seed Generation.
Enable - do not generate scrambler seed.
Disable - generate scrambler seed always.

Memory Remap

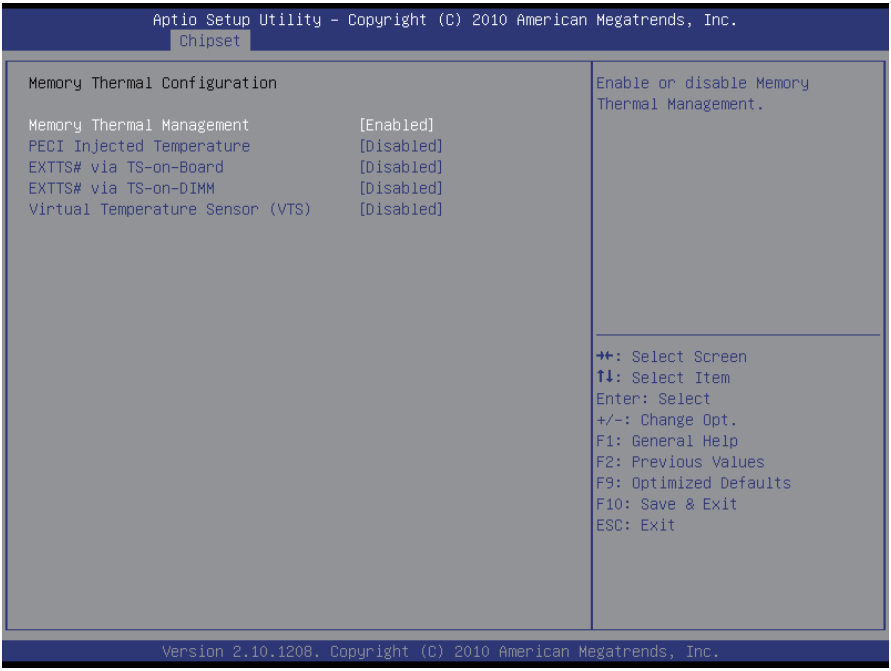
Enable or disable memory remap above 4G.

Channel A DIMM Control

Enable or disable dimms on channel A/B.

Memory Thermal Configuration

Memory Thermal Configuration Options.



Memory Thermal Management

Enable or disable Memory Thermal Management.

PECI Injected Temperature

Enable or disable memory temperatures to be injected to the processor via PECI.

ExTT# via TS-on-Board

Enable or disable routing TS-on-Board's ALERT# and THERM# to EXTTS# pins on the PCH.

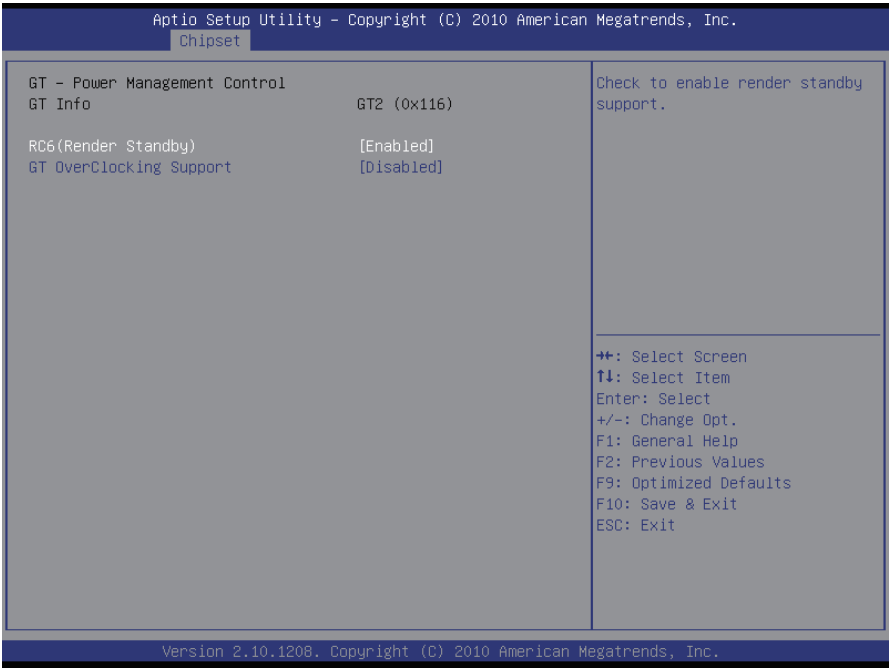
ExTT# via TS-on-DIMM

Enable or disable routing TS-on-DIMM's ALERT# to EXTTS# pin on the PCH.

Virtual Temperature Sensor (VTS)

Enable or disable Virtual Temperature Sensor.

GT – Power Management Control



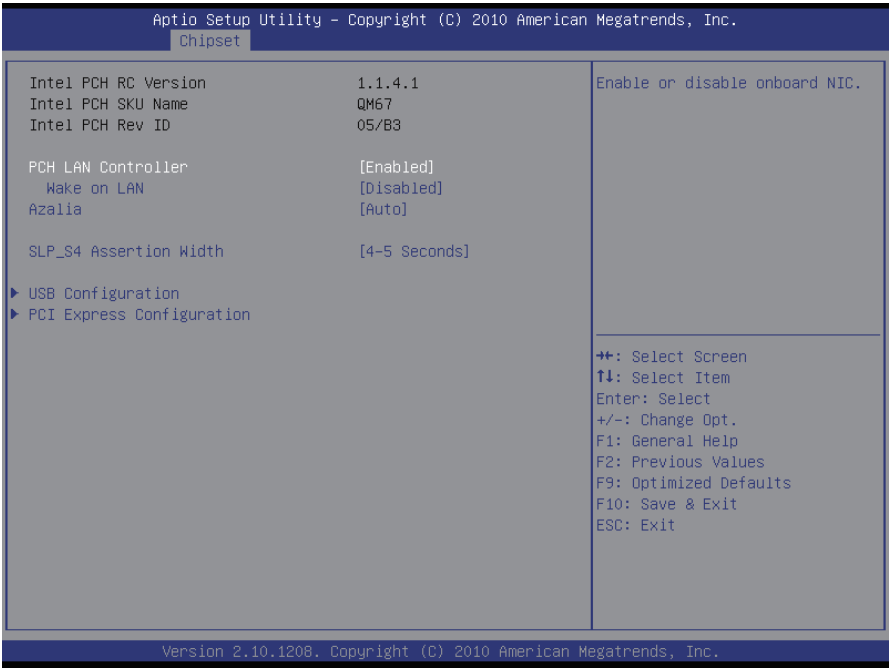
RC6 (Render Standby)

Check to enable render standby support.

GT Overclocking Support

Enable or disable GT Overclocking Support.

3.3.2 PCH-IO Configuration



PCH LAN Controller

Enable or disable onboard NIC.

Wake on LAN

Enable or disable integrated LAN to wake the system.

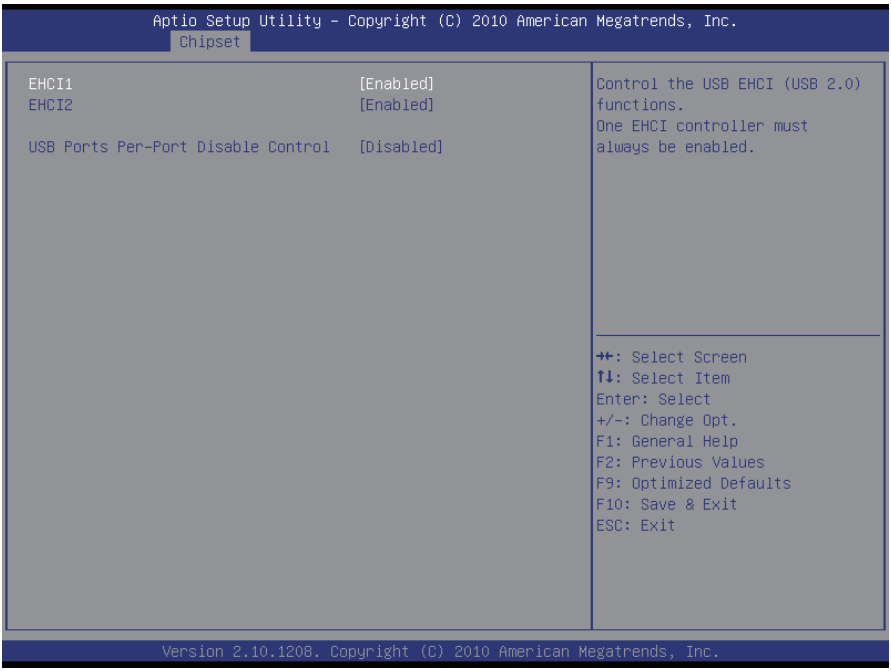
Azalia

Control detection of the Azalia device.
Disabled = Azalia will be unconditionally disabled.
Enabled = Azalia will be unconditionally enabled.
Auto = Azalia will be enabled if present, disabled otherwise.

SLP_S4 Assertion Width

Select a minimum assertion width of the SLP_S4# signal.
The choice: 1-2 Seconds, 2-3 Seconds, 3-4 Seconds, 4-5 Seconds

USB Configuration



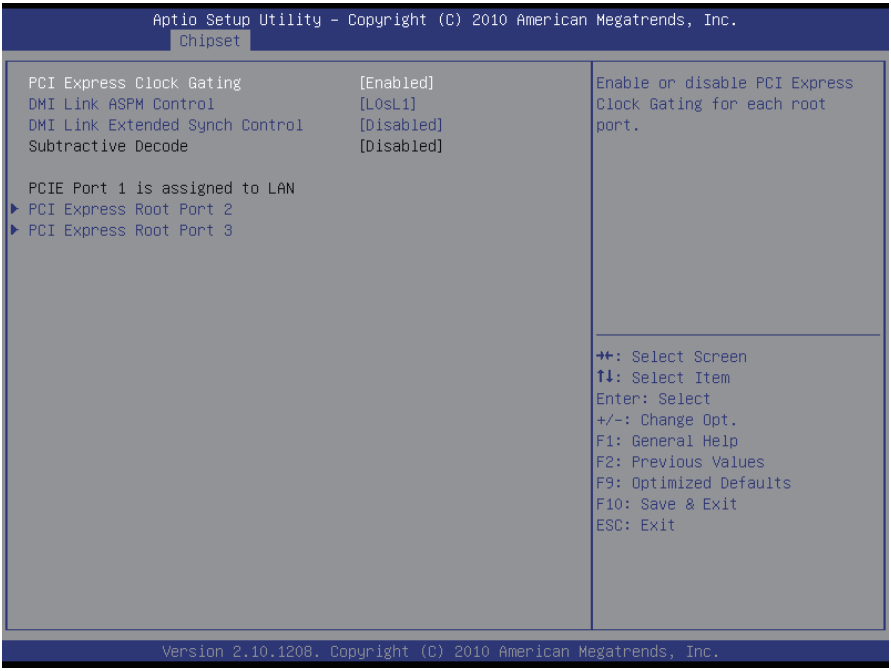
EHCI1~2

Control the USB EHCI (USB2.0) functions.
One EHCI controller must always be enabled.

USB Ports Per-Port Disable Control

Enable or disable each of the USB ports (0~9).

PCI Express Configuration



PCI Express Clock Gating

Enable or disable PCI Express Clock Gating for each root port.

DMI Link ASPM Control

The control of Active State Power Management on both NB side and SB side of the DMI Link.

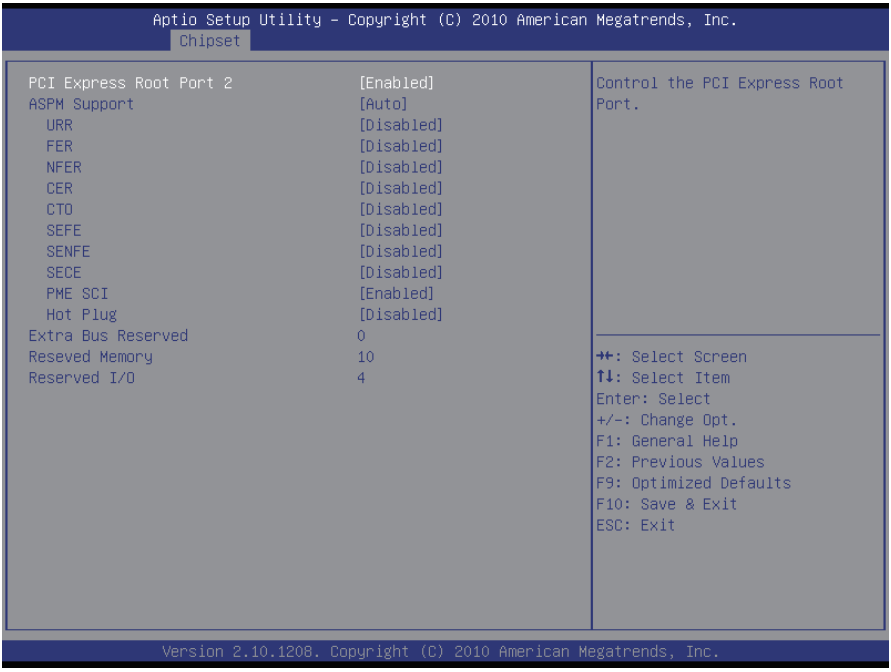
DMI Link Extended Synch Control

The control of Extended Synch on SB side of the DMI Link.

Subtractive Decode

Enable or disable Subtractive Decode.

PCI Express Root Port 2~3



PCI Express Root Port

Control the PCI Express Root Port.

ASPM Support

Set the ASPM Level to Disabled, L0s, L1, L0sL1, Auto
Force L0 - Force all links to L0 State
AUTO - BIOS auto configuration
DISABLE - Disable ASPM

URR

Enable or disable PCI Express Unsupported Request Reporting.

FER

Enable or disable PCI Express Device Fatal Error Reporting.

NFER

Enable or disable PCI Express Device Non-Fatal Error Reporting.

CER

Enable or disable PCI Express Device Correctable Error Reporting.

CTO

Enable or disable PCI Express Completion Timer TO.

SEFE

Enable or disable Root PCI Express System Error on Fatal Error.

SENFE

Enable or disable Root PCI Express System Error on Non-Fatal Error.

SECE

Enable or disable Root PCI Express System Error on Correctable Error.

PME SCI

Enable or disable PCI Express PME SCI.

Hot Plug

Enable or disable PCI Express Hot Plug.

Extra Bus Reserved

Extra Bus Reserved (0-7) for bridges behind this Root Bridge.

Reserved Memory

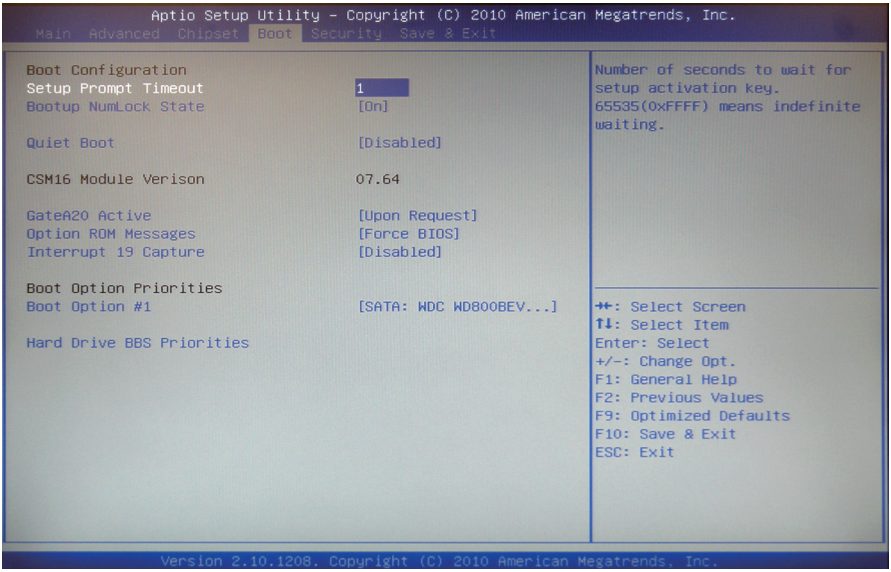
Reserved Memory and Prefetchable Memory (1-20MB) Range for this Root Bridge.

Reserved I/O

Reserved I/O (4k/8k/12k/16k/20k) Range for this Root Bridge.

3.4 Boot Settings

The Boot menu items allow you to change the system boot options.



Boot Configuration

Setup Prompt Timeout

Select the number of seconds to wait for the setup activation key.

Bootup NumLock State

This setting determines whether the Num Lock key should be activated at boot up.

Quiet Boot

This allows you to select the screen display when the system boots.

GateA20 Active

This item is to set the Gate A20 status.

Option ROM Messages

This item is to set display mode for Option ROM.

Interrupt 19 Capture

When enabled, it allows the optional ROM to trap interrupt 19.

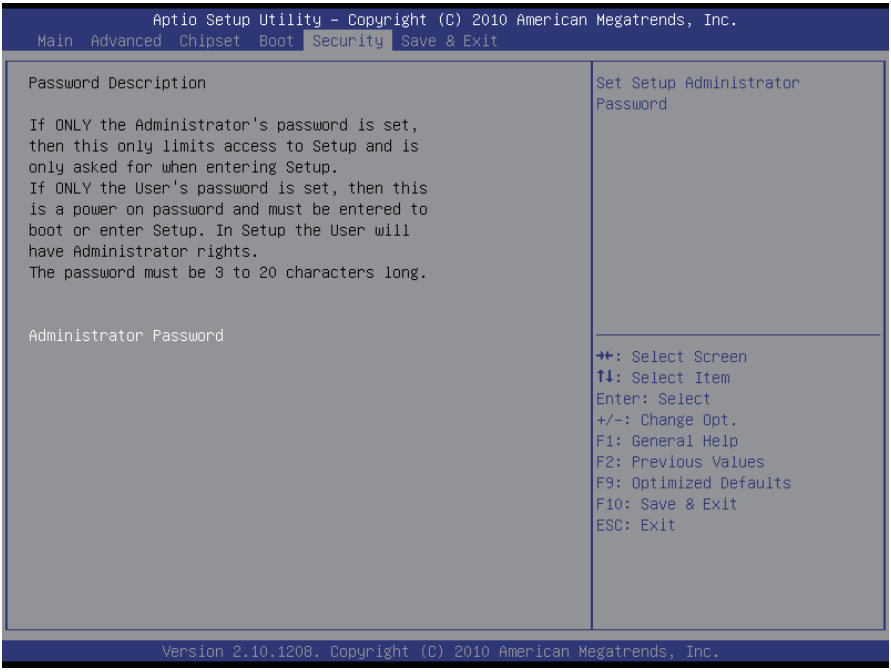
Boot Option Priorities

Select the boot sequence of the hard drives.

Hard Drive BBS Priorities

This allows you to set the hard drive boot priority. The BIOS will attempt to arrange the hard disk boot sequence automatically. You can also change the booting sequence. The number of device items that appears on the screen depends on the number of devices installed in the system.

3.5 Security



Administrator Password

Use the Administrator Password to set or change a administrator password.

ENTER PASSWORD

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <ESC> to abort the selection and not enter a password.

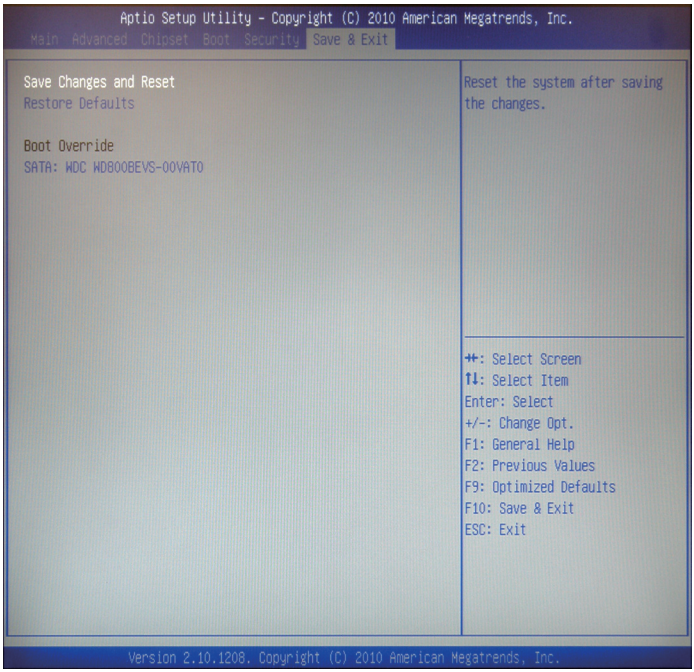
To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED
When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You can determine when the password is required within the BIOS Features Setup Menu and its Security option. If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If it’s set to “Setup”, prompting only occurs when trying to enter Setup.

3.6 Save & Exit



Save Changes and Reset

Pressing <Enter> on this item and it asks for confirmation:

Save configuration changes and exit setup?

Pressing <OK> stores the selection made in the menus in CMOS - a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

Restore Defaults

Restore system to factory default.
Pressing <Enter> on this item and it asks for confirmation prior to executing this command.

Boot Override

This group of functions includes a list of tokens, each of them corresponding to one device within the boot order. Select a drive to immediately boot that device regardless of the current boot order.

3.7 AMI BIOS Checkpoints

3.7.1 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

3.7.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed

0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.

0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available

0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)

0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable

0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found

0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

Appendix

Appendix A: I/O Port Address Map

Each peripheral device in the system is assigned with a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0x00000000-0x0000001F	Direct memory access controller
0x00000000-0x00000CF7	PCI bus
0x00000010-0x0000001F	Motherboard resources
0x00000020-0x00000021	Programmable interrupt controller
0x00000022-0x0000003F	Motherboard resources
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x0000002E-0x0000002F	Motherboard resources
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x00000040-0x00000043	System timer
0x00000044-0x0000005F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000050-0x00000053	System timer
0x00000060-0x00000060	Standard PS/2 Keyboard
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000064-0x00000064	Standard PS/2 Keyboard
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000070-0x00000077	System CMOS/real time clock
0x00000072-0x0000007F	Motherboard resources

0x00000080-0x00000080	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000081-0x00000091	Direct memory access controller
0x00000084-0x00000086	Motherboard resources
0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x00000093-0x0000009F	Direct memory access controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A2-0x000000BF	Motherboard resources
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B2-0x000000B3	Motherboard resources
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000000C0-0x000000DF	Direct memory access controller
0x000000E0-0x000000EF	Motherboard resources
0x000000F0-0x000000FF	Numeric data processor
0x00000290-0x0000029F	Motherboard resources
0x000002E0-0x000002E7	Communications 0x0000(COM6)
0x000002F0-0x000002F7	Communications 0x0000(COM5)
0x000003B0-0x000003BB	Standard VGA Graphics Adapter
0x000003C0-0x000003DF	Standard VGA Graphics Adapter
0x00000400-0x00000453	Motherboard resources
0x00000454-0x00000457	Motherboard resources
0x00000458-0x0000047F	Motherboard resources
0x000004D0-0x000004D1	Motherboard resources

0x000004D0-0x000004D1	Programmable interrupt controller
0x00000500-0x0000057F	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x00000A00-0x00000A1F	Motherboard resources
0x00000D00-0x0000FFFF	PCI bus
0x00001000-0x0000100F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x0000E000-0x0000E01F	Ethernet Controller
0x0000E000-0x0000EFFF	PCI Express standard Root Port
0x0000F000-0x0000F03F	Standard VGA Graphics Adapter
0x0000F040-0x0000F05F	SM Bus Controller
0x0000F060-0x0000F07F	Ethernet Controller
0x0000F080-0x0000F08F	Standard Dual Channel PCI IDE Controller
0x0000F090-0x0000F09F	Standard Dual Channel PCI IDE Controller
0x0000F0A0-0x0000F0A3	Standard Dual Channel PCI IDE Controller
0x0000F0B0-0x0000F0B7	Standard Dual Channel PCI IDE Controller
0x0000F0C0-0x0000F0C3	Standard Dual Channel PCI IDE Controller
0x0000F0D0-0x0000F0D7	Standard Dual Channel PCI IDE Controller
0x0000F0E0-0x0000F0EF	Standard Dual Channel PCI IDE Controller
0x0000F0F0-0x0000F0FF	Standard Dual Channel PCI IDE Controller
0x0000F100-0x0000F103	Standard Dual Channel PCI IDE Controller
0x0000F110-0x0000F117	Standard Dual Channel PCI IDE Controller
0x0000F120-0x0000F123	Standard Dual Channel PCI IDE Controller
0x0000F130-0x0000F137	Standard Dual Channel PCI IDE Controller
0x0000F140-0x0000F147	PCI Serial Port
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000F130-0x0000F137	Intel(R) 6 Series/C200 Series Chipset Family 4 port Serial ATA Storage Controller - 1C01
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources

Appendix B: BIOS Memory Map

Address	Device Description
000A0000-000BFFFF	PCI bus
000A0000-000BFFFF	Standard VGA Graphics Adapter
000D0000-000D3FFF	PCI bus
000D4000-000D7FFF	PCI bus
000D8000-000DBFFF	PCI bus
000DC000-000DFFFF	PCI bus
000E0000-000E3FFF	PCI bus
000E4000-000E7FFF	PCI bus
20000000-201FFFFF	System board
40000000-401FFFFF	System board
DFA00000-DFA00FFF	Motherboard resources
DFA00000-FEAFFFFF	PCI bus
E0000000-EFFFFFFF	Standard VGA Graphics Adapter
F7800000-F7BFFFFF	Standard VGA Graphics Adapter
F7C00000-F7CFFFFF	Ethernet Controller
F7C00000-F7DFFFFF	PCI Express standard Root Port
F7D40000-F7D5FFFF	Ethernet Controller
F7D60000-F7D63FFF	Ethernet Controller
F7E00000-F7E1FFFF	Ethernet Controller
F7E20000-F7E23FFF	High Definition Audio Controller
F7E25000-F7E250FF	SM Bus Controller
F7E26000-F7E263FF	Standard Enhanced PCI to USB Host Controller
F7E27000-F7E273FF	Standard Enhanced PCI to USB Host Controller
F7E28000-F7E28FFF	Ethernet Controller
F7E29000-F7E29FFF	PCI Serial Port
F7E2B000-F7E2B00F	PCI Simple Communications Controller
F8000000-FBFFFFFF	Motherboard resources
FED00000-FED003FF	High precision event timer
FED10000-FED17FFF	Motherboard resources

FED18000-FED18FFF	Motherboard resources
FED19000-FED19FFF	Motherboard resources
FED1C000-FED1FFFF	Motherboard resources
FED20000-FED3FFFF	Motherboard resources
FED40000-FED44FFF	System board
FED45000-FED8FFFF	Motherboard resources
FED90000-FED93FFF	Motherboard resources
FEE00000-FEEFFFFF	Motherboard resources
FF000000-FFFFFFFF	Intel(R) 82802 Firmware Hub Device
FF000000-FFFFFFFF	Motherboard resources

Appendix C: Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the required service. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 00	System timer
IRQ 01	Standard PS/2 Keyboard
IRQ 03	Ethernet Controller
IRQ 05	Communications Port (COM5)
IRQ 07	Communications Port (COM6)
IRQ 08	System CMOS/real time clock
IRQ 10	Ethernet Controller
IRQ 10	PCI Serial Port
IRQ 100	Microsoft ACPI-Compliant System
IRQ 101	Microsoft ACPI-Compliant System
IRQ 102	Microsoft ACPI-Compliant System
IRQ 103	Microsoft ACPI-Compliant System
IRQ 104	Microsoft ACPI-Compliant System
IRQ 105	Microsoft ACPI-Compliant System
IRQ 106	Microsoft ACPI-Compliant System
IRQ 107	Microsoft ACPI-Compliant System
IRQ 108	Microsoft ACPI-Compliant System
IRQ 109	Microsoft ACPI-Compliant System
IRQ 11	PCI Simple Communications Controller
IRQ 11	SM Bus Controller
IRQ 110	Microsoft ACPI-Compliant System
IRQ 111	Microsoft ACPI-Compliant System
IRQ 112	Microsoft ACPI-Compliant System
IRQ 113	Microsoft ACPI-Compliant System
IRQ 114	Microsoft ACPI-Compliant System
IRQ 115	Microsoft ACPI-Compliant System
IRQ 116	Microsoft ACPI-Compliant System

IRQ 117	Microsoft ACPI-Compliant System
IRQ 118	Microsoft ACPI-Compliant System
IRQ 119	Microsoft ACPI-Compliant System
IRQ 12	Microsoft PS/2 Mouse
IRQ 120	Microsoft ACPI-Compliant System
IRQ 121	Microsoft ACPI-Compliant System
IRQ 122	Microsoft ACPI-Compliant System
IRQ 123	Microsoft ACPI-Compliant System
IRQ 124	Microsoft ACPI-Compliant System
IRQ 125	Microsoft ACPI-Compliant System
IRQ 126	Microsoft ACPI-Compliant System
IRQ 127	Microsoft ACPI-Compliant System
IRQ 128	Microsoft ACPI-Compliant System
IRQ 129	Microsoft ACPI-Compliant System
IRQ 13	Numeric data processor
IRQ 130	Microsoft ACPI-Compliant System
IRQ 131	Microsoft ACPI-Compliant System
IRQ 131071	PCI Express standard Root Port
IRQ 131071	PCI Express standard Root Port
IRQ 131071	PCI Express standard Root Port
IRQ 131071	PCI Express standard Root Port
IRQ 132	Microsoft ACPI-Compliant System
IRQ 133	Microsoft ACPI-Compliant System
IRQ 134	Microsoft ACPI-Compliant System
IRQ 135	Microsoft ACPI-Compliant System
IRQ 136	Microsoft ACPI-Compliant System
IRQ 137	Microsoft ACPI-Compliant System
IRQ 138	Microsoft ACPI-Compliant System
IRQ 139	Microsoft ACPI-Compliant System
IRQ 140	Microsoft ACPI-Compliant System
IRQ 141	Microsoft ACPI-Compliant System

IRQ 142	Microsoft ACPI-Compliant System
IRQ 143	Microsoft ACPI-Compliant System
IRQ 144	Microsoft ACPI-Compliant System
IRQ 145	Microsoft ACPI-Compliant System
IRQ 146	Microsoft ACPI-Compliant System
IRQ 147	Microsoft ACPI-Compliant System
IRQ 148	Microsoft ACPI-Compliant System
IRQ 149	Microsoft ACPI-Compliant System
IRQ 150	Microsoft ACPI-Compliant System
IRQ 151	Microsoft ACPI-Compliant System
IRQ 152	Microsoft ACPI-Compliant System
IRQ 153	Microsoft ACPI-Compliant System
IRQ 154	Microsoft ACPI-Compliant System
IRQ 155	Microsoft ACPI-Compliant System
IRQ 156	Microsoft ACPI-Compliant System
IRQ 157	Microsoft ACPI-Compliant System
IRQ 158	Microsoft ACPI-Compliant System
IRQ 159	Microsoft ACPI-Compliant System
IRQ 16	Standard Enhanced PCI to USB Host Controller
IRQ 160	Microsoft ACPI-Compliant System
IRQ 161	Microsoft ACPI-Compliant System
IRQ 162	Microsoft ACPI-Compliant System
IRQ 163	Microsoft ACPI-Compliant System
IRQ 164	Microsoft ACPI-Compliant System
IRQ 165	Microsoft ACPI-Compliant System
IRQ 166	Microsoft ACPI-Compliant System
IRQ 167	Microsoft ACPI-Compliant System
IRQ 168	Microsoft ACPI-Compliant System
IRQ 169	Microsoft ACPI-Compliant System
IRQ 170	Microsoft ACPI-Compliant System
IRQ 171	Microsoft ACPI-Compliant System

IRQ 172	Microsoft ACPI-Compliant System
IRQ 173	Microsoft ACPI-Compliant System
IRQ 174	Microsoft ACPI-Compliant System
IRQ 175	Microsoft ACPI-Compliant System
IRQ 176	Microsoft ACPI-Compliant System
IRQ 177	Microsoft ACPI-Compliant System
IRQ 178	Microsoft ACPI-Compliant System
IRQ 179	Microsoft ACPI-Compliant System
IRQ 180	Microsoft ACPI-Compliant System
IRQ 181	Microsoft ACPI-Compliant System
IRQ 182	Microsoft ACPI-Compliant System
IRQ 183	Microsoft ACPI-Compliant System
IRQ 184	Microsoft ACPI-Compliant System
IRQ 185	Microsoft ACPI-Compliant System
IRQ 186	Microsoft ACPI-Compliant System
IRQ 187	Microsoft ACPI-Compliant System
IRQ 188	Microsoft ACPI-Compliant System
IRQ 189	Microsoft ACPI-Compliant System
IRQ 19	Standard Dual Channel PCI IDE Controller
IRQ 19	Standard Dual Channel PCI IDE Controller
IRQ 190	Microsoft ACPI-Compliant System
IRQ 22	High Definition Audio Controller
IRQ 23	Standard Enhanced PCI to USB Host Controller
IRQ 81	Microsoft ACPI-Compliant System
IRQ 82	Microsoft ACPI-Compliant System
IRQ 83	Microsoft ACPI-Compliant System
IRQ 84	Microsoft ACPI-Compliant System
IRQ 85	Microsoft ACPI-Compliant System
IRQ 86	Microsoft ACPI-Compliant System
IRQ 87	Microsoft ACPI-Compliant System
IRQ 88	Microsoft ACPI-Compliant System

IRQ 89	Microsoft ACPI-Compliant System
IRQ 90	Microsoft ACPI-Compliant System
IRQ 91	Microsoft ACPI-Compliant System
IRQ 92	Microsoft ACPI-Compliant System
IRQ 93	Microsoft ACPI-Compliant System
IRQ 94	Microsoft ACPI-Compliant System
IRQ 95	Microsoft ACPI-Compliant System
IRQ 96	Microsoft ACPI-Compliant System
IRQ 97	Microsoft ACPI-Compliant System
IRQ 98	Microsoft ACPI-Compliant System
IRQ 99	Microsoft ACPI-Compliant System

Appendix D: Digital I/O Setting

Below are the source codes written in C, please take them for Digital I/O application examples. The default I/O address is 6Eh.

C Language Code

```
//==== History ====//
//compile by TCPP 3.0
//R00     5/18/2010          1st modify

//#include "ring1726.h"
#include <stdio.h>
#include <dos.h>
#include <conio.h>

#define EC_CMD_Port                 0x6C
#define  EC_DATA_Port    0x68

unsigned long Process_686C_Command_Write(unsigned long m_ECCMD, un-
signed long m_ECDATA);
unsigned long Process_686C_Command_Read(unsigned long m_ECCMD );
unsigned long ECU_Write_686C_RAM_BYTE( unsigned long
ECUMemAddr,unsigned long ECUMemData );
unsigned long ECU_Read_686C_RAM_BYTE( unsigned long ECUMemAddr );
unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int REG_INDEX);
void SMB_Byte_WRITE(int SMPORT, int DeviceID, int REG_INDEX, int REG_
DATA);



char APName[]=       "\t\tMB-M671 DIO Testing Program\n"
                     "\t==========================================\n" ;

char APHelp[]=    "\n - Pass 'A' key for inver state of DIO GP1x"
                                "\n - Pass 'S' key for inver state of DIO GP2x"
                                "\n - Pass 'D' key for inver state of DIO GP3x"
                     "\n - Pass 'Esc' key for Exit"
                     "\n" ;

void main(void){
          char getkey = 0;
     //   char DIOSTS=0;
     //   char tempJ=0;
```

```
    //    char tempA=0;
          unsigned char GP2xVal,GP3xVal,GP1xVal;
          int SMB_PORT_AD  = 0xF040;
          //--int SMB_DEVICE_ADD = 0x9C;  /*75111R's Add=6eh */
          int SMB_DEVICE_ADD = 0x6E;       /*75111R's Add=6eh */

          clrscr();  //clear screen
          printf(APName);
          printf(APHelp);

          //pg DIO as output
          //0:input 1:Output
/*        Index 10, GPIO1x Output pin control          */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x10,0xff);
          delay(10);
/*        Index 20, GPIO2x Output pin control          */
//poweron defalult 0x00::::  SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_
ADD,0x20,0x00); //pg as Input
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x20,0xff);
/*        Index 40, GPIO3x Output pin control          */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x40,0x0f);
          delay(10);

          //pg DIO default LOW
/*        Index 11, GPIO1x Output Data value           */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,0x00);
          GP1xVal = 0;
          delay(10);

/*        Index 21, GPIO2x Output Data value           */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x21,0x00);
          GP2xVal = 0;
          delay(10);

/*        Index 41, GPIO3x Output Data value           */
          SMB_Byte_WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x41,0x00);
          GP3xVal = 0;

          gotoxy(1,9);
          //printf("DIO Status: Low \n");

          do{
                    if (getkey != 27){
                              while (!kbhit());
```

```
getkey = getch();
switch (getkey){
        case ‘D’:
        case ‘d’:
                if (GP3xVal == 0)
                {
                        GP3xVal = 1; //DIO
                        //pg DIO high
                        SMB_Byte_

                        gotoxy(1,10);
                        printf(“GP3x Status:

                }
                else
                {
                        GP3xVal = 0; //DIO
                        //pg DIO LOW
                        SMB_Byte_

                        gotoxy(1,10);
                        printf(“GP3x Status:
                }

                break;
        case ‘A’:
        case ‘a’:
                if (GP1xVal == 0)
                {
                        GP1xVal = 1; //DIO
                        //pg DIO high
                        SMB_Byte_

                        gotoxy(1,8);
                        printf(“GP1x Status:

                }
                else
                {
                        GP1xVal = 0; //DIO
                        //pg DIO LOW
                        SMB_Byte_

                        gotoxy(1,8);
```

all high

WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x41,0x0f);

LED OFF\n");

all low

WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x41,0x00);

LED ON \n");

all high

WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,0xff);

LED OFF\n");

all low

WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x11,0x00);

```
                                                    printf("GP1x Status:
                                                }
                                        break;
                                case 'S':
                                case 's':
                                                if (GP2xVal == 0)
                                                {
                                                        GP2xVal = 1; //DIO
                                                        //pg DIO high
                                                        SMB_Byte_

                                                        gotoxy(1,9);
                                                        printf("GP2x Status:

                                                }
                                                else
                                                {
                                                        GP2xVal = 0; //DIO
                                                        //pg DIO LOW
                                                        SMB_Byte_

                                                        gotoxy(1,9);
                                                        printf("GP2x Status:
                                                }
                                        break;
                                default:
                                        break;
                        };
                        //-printf( "Input: [%c]       ", getkey);  //DEBUG
                };
        }while (getkey != 27); //ESC ascii==27
        //pg all DIO as Input
}


unsigned long Process_686C_Command_Write(unsigned long m_ECCMD, un-
{
 //---------------------------------------------------------------------------
 int     i,temp;
 unsigned long m_OutBuf;
 //---------------------------------------------------------------------------
 m_OutBuf=inportb(0x6C);
 if ( ( m_OutBuf&0x00000003) > 0 )
   {
```

```
LED ON \n");




all high

WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x21,0xff);

LED OFF\n");



all low

WRITE(SMB_PORT_AD,SMB_DEVICE_ADD,0x21,0x00);

LED ON \n");









signed long m_ECDATA)
```

```
      // temp=inportb(0x68);
      return 0xFFFFFFFF;
     }

 outport(0x6C,m_ECCMD);
 for ( i=0; i<=4000; i++ )
 {
    m_OutBuf=inportb(0x6C);
    if ( ( m_OutBuf&0x00000002) == 0 )  break;
 }
  if ( i < 3999 )
     {
       outport(0x68,m_ECDATA);
        for ( i=0; i<=4000; i++ )
        {
          m_OutBuf=inportb(0x6C);
          if ( ( m_OutBuf&0x00000002) == 0 )
                {    return 0x00000000;  }
        }
     }

 if ( i > 3999 )   m_OutBuf=inportb(0x68);
 return 0xFFFFFFFF;
}
//---------------------------------------------------------------------------
unsigned long Process_686C_Command_Read(unsigned long m_ECCMD )
{
int i,temp;
 unsigned long m_OutBuf,m_InBuf;
 m_OutBuf=inportb(0x6C);
if ( ( m_OutBuf&0x00000003) > 0 )
    {
       temp=inportb(0x68);
       return 0xFFFFFFFF;

     }
 m_InBuf = m_ECCMD;
 outport(0x6C,m_InBuf);
 for ( i=0; i<=3500; i++ )
 {
    m_OutBuf=inportb(0x6C);
   if ( ( m_OutBuf&0x00000001) > 0 )
    {
      temp=inportb(0x68);
```

```
      temp= (temp & 0x000000FF ) ;
      return temp;
     // break;
    }
 }
 if ( i > 3499 )
    {
    temp=inportb(0x68);
    return 0xFFFFFFFF;
     }
 return 0xFFFFFFFF;
 }

//---------------------------------------------------------------------------
 unsigned long ECU_Read_686C_RAM_BYTE( unsigned long ECUMemAddr )
{
  unsigned long uDATA1,uDATA2,ECRamAddrH,ECRamAddrL;
  ECRamAddrL=ECUMemAddr%256;   ECRamAddrH=ECUMemAddr/256;
  //
  uDATA1=Process_686C_Command_Write(0x000000A3, ECRamAddrH );
  if ( uDATA1==0xFFFFFFFF ) { return 0xFFFFFFFF; }
  //
  uDATA1=Process_686C_Command_Write(0x000000A2, ECRamAddrL );
  if ( uDATA1==0xFFFFFFFF ) { return 0xFFFFFFFF; }
  //
  uDATA1=Process_686C_Command_Read( 0x000000A4 );
  if ( uDATA1 > 0x000000FF ) { return 0xFFFFFFFF; }
  uDATA2=Process_686C_Command_Read( 0x000000A4 );
  if ( uDATA2 > 0x000000FF ) { return 0xFFFFFFFF; }
  if (uDATA1==uDATA2) return uDATA1;
  else return  0xFFFFFFFF;
}
//---------------------------------------------------------------------------
 unsigned long ECU_Write_686C_RAM_BYTE( unsigned long
ECUMemAddr,unsigned long ECUMemData )
{
  unsigned long uDATA, RD_DATA, ECRamAddrH, ECRamAddrL;
  ECRamAddrL=ECUMemAddr%256;   ECRamAddrH=ECUMemAddr/256;
  //
  uDATA=Process_686C_Command_Write(0x000000A3, ECRamAddrH );
  if ( uDATA==0xFFFFFFFF ) { return 0xFFFFFFFF;}
  //
  uDATA=Process_686C_Command_Write(0x000000A2, ECRamAddrL );
  if ( uDATA==0xFFFFFFFF ) { return 0xFFFFFFFF;}
```

```
  //
  uDATA=Process_686C_Command_Write(0x000000A5, ECUMemData );
  if ( uDATA==0xFFFFFFFF ) { return 0xFFFFFFFF;}
  //
  return  0x00000000;
}
//---------------------------------------------------------------------------


unsigned char SMB_Byte_READ(int SMPORT, int DeviceID, int REG_INDEX)
{
        unsigned char SMB_R;
        outportb(SMPORT+02, 0x00);          /* clear */
        outportb(SMPORT+00, 0xff);          /* clear */
        delay(10);
        outportb(SMPORT+04, DeviceID+1);        /* clear */
        outportb(SMPORT+03, REG_INDEX);           /* clear */
        outportb(SMPORT+02, 0x48);          /* read_byte */
        delay(10);
        //printf(" %02x ",inportb(SMPORT+05));
        SMB_R= inportb(SMPORT+05);
        return SMB_R;
}

void SMB_Byte_WRITE(int SMPORT, int DeviceID, int REG_INDEX, int REG_
DATA)
{
        outportb(SMPORT+02, 0x00);          /* clear */
        outportb(SMPORT+00, 0xff);          /* clear */
        delay(10);
        outportb(SMPORT+04, DeviceID);                /* clear */
        outportb(SMPORT+03, REG_INDEX);           /* clear */
        outportb(SMPORT+05, REG_DATA);            /* read_byte */
        outportb(SMPORT+02, 0x48);          /* read_byte */
/*      delay(10);
        printf(" %02x ",inportb(SMPORT+05)); */
}
```

Digital IO Usage Table (Super IO Chipset F75111)

Pin	Description	Chipset Pin#	Chipset Pin Description
1	DIO0	10	GPIO10
2	DIO1	11	GPIO11
3	DIO2	12	GPIO12
4	DIO3	3	GPIO13
5	DIO4	9	GPIO14
6	DIO5	19	GPIO15
7	DIO6	4	GPIO16
8	DIO7	5	GPIO17
9	DIO8	6	GPIO20
10	DIO9	7	GPIO21
11	DIO10	8	GPIO22
12	DIO11	24	GPIO23
13	DIO12	23	GPIO24
14	DIO13	22	GPIO25
15	DIO14	21	GPIO26
16	DIO15	20	GPIO27

Appendix E: Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitor the activity of CPU. Application software depends on its own requirement to trigger WDT with adequate timer setting. Before WDT time-out, the functional normal system will reload the WDT. The WDT never times out for a normal system. Then, WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255-level watchdog timer by software programming. Below are the source codes written in C, please take them as WDT application example.

```
/*-----    Include Header Area -----*/
#include “math.h”
#include “stdio.h”
#include “dos.h”

/*-----    routing, sub-routing -----*/

void main()
{
        outportb(0x2e, 0x87);              /* initial IO port */
        outportb(0x2e, 0x87);          /* twice,  */

        outportb(0x2e, 0x07);          /* point to logical device */
        outportb(0x2e+1, 0x07);          /* select logical device 7 */
        outportb(0x2e, 0xf5);          /* select offset f5h */
        outportb(0x2e+1, 0x40);          /* set bit5 = 1 to clear bit5 */
        outportb(0x2e, 0xf0);          /* select offset f0h */
        outportb(0x2e+1, 0x81);          /* set bit7 =1 to enable WDTRST# */
        outportb(0x2e, 0xf6);          /* select offset f6h */
        outportb(0x2e+1, 0x05);          /* update offset f6h to 0ah :10sec */
        outportb(0x2e, 0xf5);          /* select offset f5h */
        outportb(0x2e+1, 0x20);          /* set bit5 = 1 enable watch dog time
*/

        outportb(0x2e, 0xAA);          /* stop program F71869E, Exit */
}
```

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