GENE-CV05

Intel® Atom™ D2550/N2800/N2600 Processor

With LVDS

10/100/1000Base-TXEthernet

1 Mini Card, LPC

6 USB2.0, 6 COM

2CH HD Audio + 2W Amplifier

GENE-CV05 Manual Rev. A 3rd Ed.
June 2012

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Acknowledgments

Packing List

Before you begin installing your card, please make sure that the following materials have been shipped:

- GENE-CV05 CPU Card with Active Cooler (Intel® Atom™ D2550 version) or Passive Heatsink (Intel® Atom™ N2800/N2600 version)
- DVD-ROM for manual (in PDF format) and drivers

If any of these items should be missing or damaged, please contact your distributor or sales representative immediately.

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1

General Information

1.1 Introduction

AAEON, a leading embedded boards manufacturer, is pleased to announce the debut of their new generation 3.5" SubCompact Board—GENE-CV05.

GENE-CV05 adopts Intel® Atom™ D2550/N2800/N2600 Processor. The system memory is deployed with 204-pin SODIMM DDR3 800/1066 up to 4 GB for Intel® Atom™ D2550 /N2800 processor and up to 2 GB for Intel® Atom™ N2600 Processor. In addition, Realtek RTL8111E supports two 10/100/1000Base-TX that allows a faster network connections.

The display of GENE-CV05 supports CRT/LCD, DVI/LCD simultaneous and dual view displays. This model applies one Mini Card and LPC bus for flexible expansions. Moreover, one SATA 3.0Gb/s and one CFast™ provide a better storage. Six USB2.0, six COM Ports (five RS-232, one RS-232/422/485) and 8-bit digital I/O are configured on the GENE-CV05 as well. Full functions make GENE-CV05 user friendly. This brand new SubCompact board is developed to cater to the requirements of Automation, Medical, ticket machine, transportation, gaming, KIOSK, and POS/POI applications.

1.2 Features

- Onboard Intel® Atom™ D2550/N2800/N2600 Processor
- Intel® NM10
- DDR3 800/1066 SODIMM , Max. 4 GB for Intel® Atom™ D2550/N2800 Processor, and Max. 2 GB for Intel® Atom™ N2600 Processor
- Gigabit Ethernet x 2
- CRT, 24-bit Single Channel LVDS LCD +18/24-bit Single Channel LVDS LCD for Intel® Atom™ D2550 Processor; 18-bit Single Channel LVDS LCD+ 18/24-bit Single Channel LVDS LCD for Intel® Atom™ N2800/N2600 Processor
- 2CH HD Audio + 2W Amplifier
- SATA 3.0Gb/s x 1, CFast™ x 1
- USB2.0 x 6, COM x 6 , 8-bit Digital I/O, Parallel x 1 (Optional)
- Onboard 4/5/8-wire Resistive Touch Screen Controller
- Mini Card x 1
- +12V Only Operation
- Onboard Trusted Platform Module (Optional)
- mSATA x 1 (Optional, if you choose mSATA, the functions of Mini Card & CFAST™ will be disabled.)

1.3 Specifications

System

Processor	Intel® Atom™ D2550/N2800/N2600 processor
System Memory	204-pin DDR3 SODIMM x 1, Max. 4 GB (DDR3 800/1066) for Intel® Atom™D2550/N2800; Max. 2 GB (DDR3 800/1066) for Intel® Atom™N2600
Chipset	Intel® NM10
I/O Chipset	ITE 8783
Ethernet	Realtek RTL8111E, 10/100/1000Base-TX, RJ-45 x 2
BIOS	AMI Plug & Play SPI BIOS – 32 MB Flash
Wake On LAN	Yes
Watchdog Timer	Generates a time-out system reset
H/W Status Monitoring	Supports power supply voltages and temperature monitoring
Expansion Interface	Mini Card x 1, LPC bus
Power Requirement	+12V, AT/ATX
Trusted Platform	Infineon SLB 9635 TT 1.2

Module (TPM)	(Optional)
● Battery	Lithium battery
● Board Size	5.75”(L) x 4”(W) (146mm x 101.6mm)
● Gross Weight	0.88 lb (0.4 Kg)
● Operating Temperature	32˚F~ 140˚F (0˚C ~ 60˚C)
● Storage Temperature	-40˚F~ 176˚F (-40˚C ~ 80˚C)
● Operating Humidity	0%~90% relative humidity, non-condensing

Display: Supports CRT/LCD, DVI/LCD, simultaneous and dual view displays

● Chipset	Intel® Atom™ D2550/N2800/N2600 integrated
● Memory	Shared system memory up to 256 MB
● LCD Interface	LCD Interface Dual LVDS LCDs: 24-bit Single Channel LVDS LCD + 18/24-bit Single channel LVDS LCD for Intel® Atom™D2550; 18-bit Single Channel LVDS LCD + 18/24-bit Single Channel LVDS LCD for Intel® Atom™N2800/N2600
● Resolution	Up to 1920 x 1200 for CRT;

Up to 1366 x 768 for LCD

I/O

- Storage: SATA 3.0Gb/s x 1, CFast™ x 1
- Serial Port: RS-232 x 5, RS-232/422/485 (auto flow) x 1
- Parallel Port: SPP/EPP/ECP x 1 (Optional)
- USB Port: USB2.0 x 6
- PS/2 Port: Keyboard x 1, Mouse x 1
- Digital I/O: Supports 8-bit (Programmable)
- Audio: MIC-in, Line-in, Line-out
- Touch Screen: Supports 4/5/8-wire resistive touch screen

Note: If you choose Parallel Port, the COM6 will be removed from the GENE-CV05.

Chapter

2

Quick Installation Guide

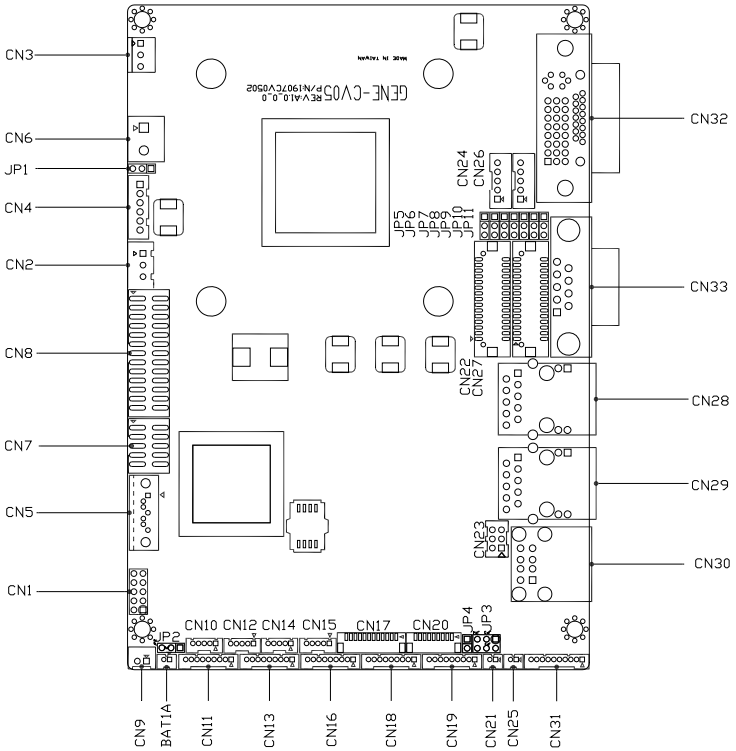
2.1 Safety Precautions

Always completely disconnect the power cord from your board whenever you are working on it. Do not make connections while the power is on, because a sudden rush of power can damage sensitive electronic components.

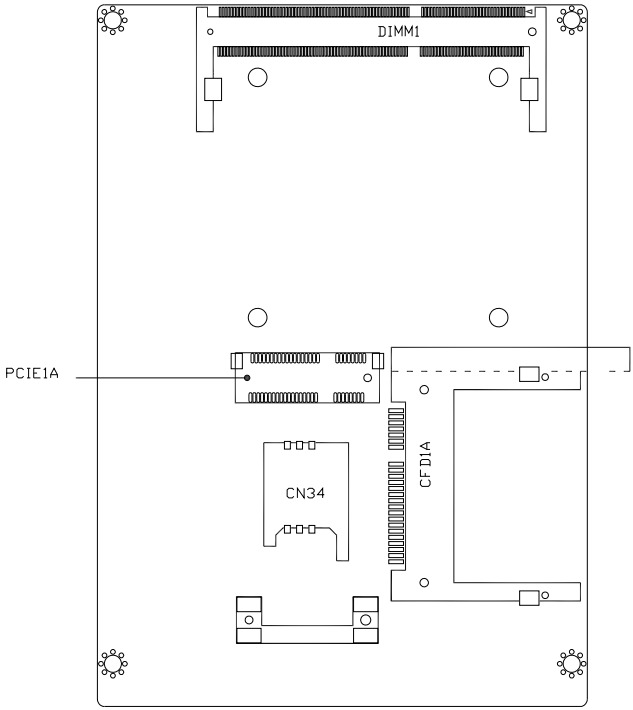
Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis

2.2 Location of Connectors and Jumpers

Component Side

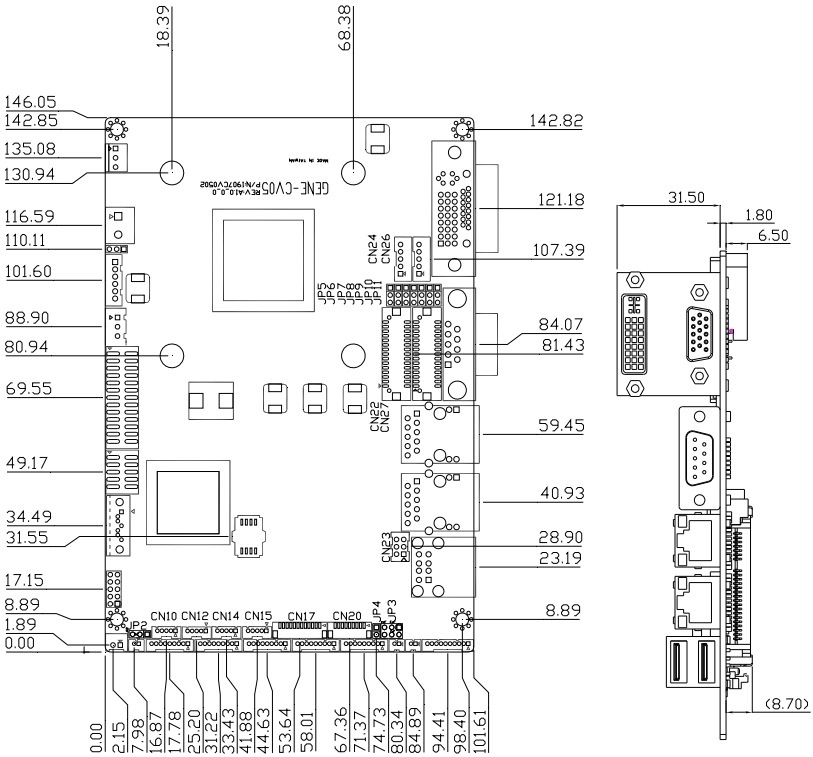


Solder Side

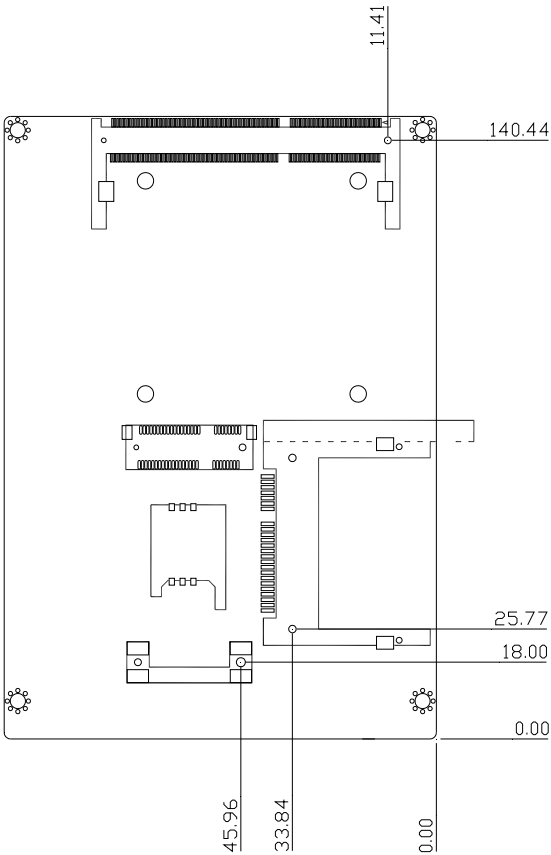


2.3 Mechanical Drawing

Component Side



Solder Side



2.4 List of Jumpers

The board has a number of jumpers that allow you to configure your system to suit your application.

The table below shows the function of each of the board's jumpers:

Label	Function
JP1	Auto Power Button Selection
JP2	Clear CMOS
JP3	COM2 RI/+5/+12V Selection
JP4	Touch Screen 4/5/8-wires Mode Selection
JP5	Brightness Control for 2nd LVDS
JP6	2nd LVDS Backlight Bias/PWM Mode Selection
JP7	2nd LVDS Operating Voltage Selection
JP8	2nd LVDS Inverter Voltage Selection
JP9	1st LVDS Inverter Voltage Selection
JP10	1st LVDS Backlight Bias/PWM Mode Selection
JP11	1st LVDS Operating Voltage Selection

2.5 List of Connectors

The board has a number of connectors that allow you to configure your system to suit your application. The table below shows the function of each board's connectors:

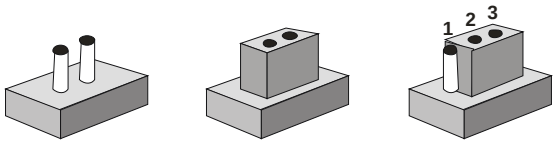
Label	Function
CN1	Front Panel
CN2	External +5VSB Input
CN3	CPU FAN
CN4	+5VSB Output w/ SMBus
CN5	SATA Port
CN6	External 12V Input
CN7	Digital I/O
CN8	Parallel Port
CN9	+5V Output for SATA HDD using
CN10	USB Port #6
CN11	COM Port #6
CN12	USB Port #5
CN13	COM Port #5
CN14	USB Port #4
CN15	USB Port #3
CN16	COM Port #4
CN17	LPC Expansion I/F
CN18	COM Port #3

CN19	COM Port #2
CN20	Touch Screen
CN21	Stereo-R Channel
CN22	2nd LVDS (Dual channel 18/24bit)
CN23	PS/2 Keyboard & Mouse
CN24	2nd LVDS Inverter
CN25	Stereo-L Channel
CN26	1st LVDS Inverter
CN27	1st LVDS (Single channel 18/24bit)
CN28	2nd RJ-45 Ethernet
CN29	1st RJ-45 Ethernet
CN30	USB Port #1 and #2
CN31	Audio Line In/Out and MIC
CN32	CRT/DVI (Configured by manufacturing)
CN33	COM Port #1
CN34	SIM Card Socket
CFD1	CFAST™
PCIE1	Mini Card/mSATA (Configured by manufacturing)
DIMM1	DDR3 SODIMM Slot

2.6 Setting Jumpers

You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip.

To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



Open Closed Closed 2-3

A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any change.

Generally, you simply need a standard cable to make most connections.

2.7 Auto Power Button Selection (JP1)

JP1	Function
1-2	Enable(Default)
2-3	Disable

2.8 Clear CMOS (JP2)

JP2	Function
1-2	Normal (Default)
2-3	Clear CMOS

2.9 COM2 RI/+5V/+12V Selection (JP3)

JP3	Function
1-2	+12V
3-4	RI (Default)
5-6	+5V

Note: Max. Current rating is 0.5A.

2.10 Touch Screen 4/5/8-wire Mode Selection (JP4)

JP4	Function
1-2	4/8-wire (Default)
Open	5-wire

2.11 Brightness Control for 2nd LVDS (JP5)

JP5	Function
1-2	Brightness Up
2-3	Brightness Down

Note: Controlled by triggering UP or DOWN.

2.12 2nd LVDS Backlight Bias/PWM Mode Selection (JP6)

JP6	Function
1-2	Bias (Default)
2-3	PWM Control

2.13 2nd LVDS Operating Voltage Selection (JP7)

JP7	Function
1-2	+5V
2-3	+3.3V (Default)

Note: Max. Current rating is 2A.

2.14 2nd LVDS Inverter Voltage Selection (JP8)

JP8	Function
1-2	+12V
2-3	+5V (Default)

Note: Max. Current rating is 1A.

2.15 1st LVDS Inverter Voltage Selection (JP9)

JP9	Function
1-2	+12V
2-3	+5V (Default)

Note: Max. Current rating is 1A.

2.16 1st LVDS Backlight Bias/PWM Mode Selection (JP10)

JP10	Function
1-2	Bias (Default)
2-3	PWM Control

2.17 1st LVDS Operating Voltage Selection (JP11)

JP11	Function
1-2	+5V
2-3	+3.3V (Default)

Note: Max. Current rating is 2A.

2.18 Front Panel (CN1)

Pin	Signal
(-) 1-2 (+)	ATX Power-on Button
(-) 3-4 (+)	HDD Active LED
(-) 5-6 (+)	External Speaker
(-) 7-8 (+)	Power LED
(-) 9-10 (+)	System Reset Button

2.19 External +5VSB Input (CN2)

Pin	Signal
1	PSON#
2	Ground
3	+5 Volt. Standby

Note: Max. Current rating is 2A.

2.20 CPU Fan Connector (CN3)

Pin	Signal
1	Ground
2	+12 Volt.
3	FAN Sense

2.21 +5VSB Output w/SMBUS (CN4)

Pin	Signal
1	SMBDATA
2	Ground
3	SMBCLK
4	Ground
5	PSON#
6	+5 Volt. Standby

2.22 SATA Port (CN5)

Pin	Signal
1	Ground
2	TX0+
3	TX0-
4	Ground
5	RX0-
6	RX0+
7	Ground

2.23 External 12V Input (CN6)

DC terminal

Pin	Signal
1	+12 Volt.
2	Ground

Note: Max. Current rating is 4A.

2.24 Digital I/O Connector (CN7)

I2C Address: 0x6Eh

Pin	Signal	Pin	Signal
1	Port 1	2	Port 2
3	Port 3	4	Port 4
5	Port 5	6	Port 6
7	Port 7	8	Port 8
9	+3.3 Volt.	10	Ground

BIOS Setting (I2C address)	Connector Definition	Address(Register)		F75111 GPIO Setting
		Output	Input	
Port 1 @6Eh	Pin 1	21h/Bit 0	22h/Bit 0	U44 Pin 6 (GPIO 20)
Port 2 @6Eh	Pin 2	21h/Bit 1	22h/Bit 1	U44 Pin 7 (GPIO 21)
Port 3 @6Eh	Pin 3	21h/Bit 2	22h/Bit 2	U44 Pin 8 (GPIO 22)
Port 4 @6Eh	Pin 4	21h/Bit 3	22h/Bit 3	U44 Pin 24(GPIO 23)
Port 5 @6Eh	Pin 5	21h/Bit 4	22h/Bit 4	U44 Pin 23(GPIO 24)
Port 6 @6Eh	Pin 6	21h/Bit 5	22h/Bit 5	U44 Pin 22(GPIO 25)
Port 7 @6Eh	Pin 7	21h/Bit 6	22h/Bit 6	U44 Pin 21(GPIO 26)
Port 8 @6Eh	Pin 8	21h/Bit 7	22h/Bit 7	U44 Pin 20(GPIO 27)

2.25 Parallel Port Connector (CN8) (Optional)

Pin	Signal	Pin	Signal
1	STB	2	AFD#
3	D0	4	ERROR#
5	D1	6	PINIT#
7	D2	8	SLIN#

9	D3	10	Ground
11	D4	12	Ground
13	D5	14	Ground
15	D6	16	Ground
17	D7	18	Ground
19	ACK#	20	Ground
21	BUSY	22	Ground
23	PE	24	Ground
25	SLCT	26	N/C

2.26 +5V Output for SATA HDD Usage (CN9)

Pin	Signal
1	+5 Volt.
2	Ground

Note: Max. Current rating is 1A.

2.27 USB Port #6 (CN10)

Pin	Signal
1	+5 Volt. Standby
2	Data5-
3	Data5+
4	Ground
5	Ground

2.28 COM Port #6 (CN11)

Pin	Signal	Pin	Signal
1	DCDF	2	DSRF
3	RXF	4	RTSF

5	TXF	6	CTSF
7	DTRF	8	RIF
9	Ground	10	N/C

2.29 USB Port #5 (CN12)

Pin	Signal
1	+5 Volt. Standby
2	Data4-
3	Data4+
4	Ground
5	Ground

2.30 COM Port #5 (CN13)

Pin	Signal	Pin	Signal
1	DCDE	2	DSRE
3	RXE	4	RTSE
5	TXE	6	CTSE
7	DTRE	8	RIE
9	Ground	10	N/C

2.31 USB Port #4 (CN14)

Pin	Signal
1	+5 Volt. Standby
2	Data3-
3	Data3+
4	Ground
5	Ground

2.32 USB Port #3 (CN15)

Pin	Signal
1	+5 Volt. Standby
2	Data2-
3	Data2+
4	Ground
5	Ground

2.33 COM Port #4 (CN16)

Pin	Signal	Pin	Signal
1	DCDD	2	DSRD
3	RXD	4	RTSD
5	TXD	6	CTSD
7	DTRD	8	RID
9	Ground	10	N/C

2.34 LPC Expansion I/F (CN17)

Pin	Signal
1	LAD0
2	LAD1
3	LAD2
4	LAD3
5	+3.3 Volt.
6	LFRAME#
7	LRESET#
8	Ground
9	LPC_CLK

10	LDRQ#0
11	LDRQ#1
12	SERIRQ

2.35 COM Port #3 (CN18)

Pin	Signal	Pin	Signal
1	DCDC	2	DSRC
3	RXC	4	RTSC
5	TXC	6	CTSC
7	DTRC	8	RIC
9	Ground	10	N/C

2.36 COM Port #2 (CN19)

RS-232 Mode

Pin	Signal	Pin	Signal
1	DCDB	2	DSRB
3	RXB	4	RTSB
5	TXB	6	CTSB
7	DTRB	8	RIB / +5 Volt. / (+12 Volt.)
9	Ground	10	N/C

RS-422 Mode

Pin	Signal	Pin	Signal
1	TXD-	2	N/C
3	RXD+	4	N/C
5	TXD+	6	N/C
7	RXD-	8	N/C / +5 Volt. / (+12 Volt.)
9	Ground	10	N/C

RS-485 Mode

Pin	Signal	Pin	Signal
1	TXD-	2	N/C
3	N/C	4	N/C
5	TXD+	6	N/C
7	N/C	8	N/C / +5 Volt. / (+12 Volt.)
9	Ground	10	N/C

2.37 Touch Screen (CN20)

Pin	8-wire Signal	4-wire Signal	5-wire Signal
1	Ground	Ground	Ground
2	Top Excite	Top	UL(Y)
3	Bottom Excite	Bottom	UR(H)
4	Left Excite	Left	LL(L)
5	Right Excite	Right	LR(X)
6	Top Sense	N/C	SENSE
7	Bottom Sense	N/C	N/C
8	Left Sense	N/C	N/C
9	Right Sense	N/C	N/C

2.38 Stereo-R Channel (CN21)

Pin	Signal
1	R+
2	R-

2.39 2nd LVDS Output Single Channel 18/24-bit (CN22)

Pin	Signal	Pin	Signal
1	2nd Back-Light Enable	2	2nd Back-Light Control

3	2nd LCD Volt.	4	Ground
5	LB_CLK#	6	LB_CLK
7	2nd LCD Volt.	8	Ground
9	LB_DATA#_0	10	LB_DATA_0
11	LB_DATA#_1	12	LB_DATA_1
13	LB_DATA#_2	14	LB_DATA_2
15	LB_DATA#_3	16	LB_DATA_3
17	2nd LVD_DDCDAT	18	2nd LVD_DDCCLK
19	LC_DATA#_0	20	LC_DATA_0
21	LC_DATA#_1	22	LC_DATA_1
23	LC_DATA#_2	24	LC_DATA_2
25	LC_DATA#_3	26	LC_DATA_3
27	2nd LCD Volt.	28	Ground
29	LC_CLK#	30	LC_CLK

2.40 PS/2 Keyboard and Mouse Connector (CN23)

Pin	Signal	Pin	Signal
1	Keyboard Data	2	Keyboard Clock
3	Ground	4	+5 Volt.
5	Mouse Data	6	Mouse Clock

2.41 2nd LVDS Inverter (CN24)

Pin	Signal
1	+5 Volt. / +12 Volt.
2	2nd Brightness Control (Controlled by CH7511B)
3	Ground
4	Ground
5	2nd Backlight Enable (Controlled by CH7511B)

Note: Max. Current rating is 1A.

2.42 Stereo-L Channel Inverter (CN25)

Pin	Signal
1	L+
2	L-

2.43 1st LVDS Inverter (CN26)

Pin	Signal
1	+5 Volt. / +12 Volt.
2	1st Brightness Control (Controlled by Cedarview)
3	Ground
4	Ground
5	1st Backlight Enable (Controlled by Cedarview)

Note: Max. Current rating is 1A.

2.44 1st LVDS Output-Single Channel 18/24-bit (CN27)

Pin	Signal	Pin	Signal
1	1st Back-Light Enable	2	1st Back-Light Control
3	1st LCD Volt.	4	Ground
5	LA_CLK#	6	LA_CLK
7	1st LCD Volt.	8	Ground
9	LA_DATA#_0	10	LA_DATA_0
11	LA_DATA#_1	12	LA_DATA_1
13	LA_DATA#_2	14	LA_DATA_2
15	LA_DATA#_3	16	LA_DATA_3
17	1st LVD_DDCDAT	18	1st LVD_DDCCLK
19	N/C	20	N/C
21	N/C	22	N/C
23	N/C	24	N/C

25	N/C	26	N/C
27	1st LCD Volt.	28	Ground
29	N/C	30	N/C

2.45 2nd RJ-45 Ethernet Connector (CN28)

Pin	Signal	Pin	Signal
R1	LAN2_MDIO0+	R2	LAN2_MDIO0-
R3	LAN2_MDIO1+	R4	LAN2_MDIO1-
R5	LAN2_TCD0	R6	LAN2_TCD1
R7	LAN2_MDIO2+	R8	LAN2_MDIO2-
R9	LAN2_MDIO3+	R10	LAN2_MDIO3-
L1	LAN2_SPD100_LED	L2	LAN2_SPD1K_LED
L3	LAN2_ACT_LED	L4	+3.3 Volt.

2.46 1st RJ-45 Ethernet Connector (CN29)

Pin	Signal	Pin	Signal
R1	LAN1_MDIO0+	R2	LAN1_MDIO0-
R3	LAN1_MDIO1+	R4	LAN1_MDIO1-
R5	LAN1_TCD0	R6	LAN1_TCD1
R7	LAN1_MDIO2+	R8	LAN1_MDIO2-
R9	LAN1_MDIO3+	R10	LAN1_MDIO3-
L1	LAN1_SPD100_LED	L2	LAN1_SPD1K_LED
L3	LAN1_ACT_LED	L4	+3.3 Volt.

2.47 USB Port #1 and #2 (CN30)

Pin	Signal	Pin	Signal
1	+5 Volt. Standby	5	+5 Volt. Standby
2	Data0-	6	Data1-

3	Data0+	7	Data1+
4	Ground	8	Ground

2.48 Audio Line In/Out and MIC (CN31)

Pin	Signal
1	MIC_L
2	MIC_R
3	Ground
4	Line IN_L
5	Line IN_R
6	Ground
7	Line OUT_L
8	Ground
9	Line OUT_R
10	+5 Volt.

2.49 DVI/CRT Display Connector (CN32) Configured by manufacturing

DVI

Pin	Signal	Pin	Signal
C1	RED	C2	GREEN
C3	BLUE	C4	HSYNC
C5	Ground	C6	N/C
1	DVI_TDC2#	2	DVI_TDC2
3	Ground	4	DDCCLK
5	DDCDATA	6	DVI_CLK
7	DVI_DATA	8	VSYNC
9	DVI_TDC1#	10	DVI_TDC1

11	Ground	12	N/C
13	N/C	14	+5 Volt.
15	Ground	16	DVI_DET
17	DVI_TDC0#	18	DVI_TDC0
19	Ground	20	N/C
21	N/C	22	Ground
23	DVI_TLC	24	DVI_TLC#
25	Ground	26	Ground
27	N/C	28	N/C

CRT Display

Pin	Signal	Pin	Signal
29	DDCCLK	30	N/C
31	+5 Volt.	32	HSYNC
33	GREEN	34	Ground
35	N/C	36	Ground
37	Ground	38	VSYNC
39	BLUE	40	Ground
41	DDCDATA	42	RED
43	CRT_PLUG#		

2.50 COM Port #1 (CN32)

Pin	Signal	Pin	Signal
1	DCDA	2	RXA
3	TXA	4	DTRA
5	Ground	6	DSRA
7	RTSA	8	CTSA
9	RIA		

2.51 SIM Card Socket (CN34)

Pin	Signal	Pin	Signal
1	UIM_PWR	2	UIM_RST
3	UIM_CLK	4	Ground
5	UIM_VPP	6	UIM_DATA

2.52 CFast™ Disk (CFD1)

Pin	Signal
S1	Ground
S2	SATA_TX+
S3	SATA_TX-
S4	Ground
S5	SATA_RX-
S6	SATA_RX+
S7	Ground
P1	N/C
P2	Ground
P3	N/C
P4	N/C
P5	N/C
P6	N/C
P7	Ground
P8	CFD_LED#
P9	N/C
P10	N/C
P11	N/C
P12	N/C

P13	+3.3 Volt.
P14	+3.3 Volt.
P15	Ground
P16	Ground
P17	N/C

2.53 Mini Card/ mSATA (PCIE1)

Pin	Signal	Pin	Signal
1	PCIE_WAKE#	2	+3.3 Volt. Standby/+3.3 Volt.
3	N/C	4	Ground
5	N/C	6	+1.5 Volt.
7	CLKREQ#	8	UIM_PWR
9	Ground	10	UIM_DATA
11	MCARD_CLK#	12	UIM_CLK
13	MCARD_CLK	14	UIM_RESET
15	Ground	16	UIM_VPP
17	N/C	18	Ground
19	N/C	20	W_DISABLE#
21	Ground	22	PCIE_RST#
23	PCIE_RXN/mSATA_RX+	24	+3.3 Volt. Standby/+3.3 Volt.
25	PCIE_RXP/mSATA_RX-	26	Ground
27	Ground	28	+1.5 Volt.
29	Ground	30	SMBCLK
31	PCIE_TXN/mSATA_TX-	32	SMBDATA
33	PCIE_TXP/mSATA_TX+	34	Ground
35	Ground	36	USB_Data7-
37	Ground	38	USB_Data7+

39	+3.3 Volt. Standby/+3.3 Volt.	40	Ground
41	+3.3 Volt. Standby/+3.3 Volt.	42	N/C
43	Ground	44	N/C
45	N/C	46	N/C
47	N/C	48	+1.5 Volt.
49	N/C	50	Ground
51	N/C	52	+3.3 Volt. Standby/+3.3 Volt.

2.54 DDR3 SODIMM Slot (DIMM1)

Standard Specification

Below Table for China RoHS Requirements
产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 **SJ/T 11363-2006** 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 **SJ/T 11363-2006** 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

Chapter

3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration against the values stored in the CMOS memory. If they do not match, the program outputs an error message. You will then need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The CMOS memory has lost power and the configuration information has been erased.

The GENE-CV05 CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del> or <F2> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Advanced BIOS Features Setup including TPM, ACPI, etc.

Chipset

Host bridge parameters.

Boot

Enables/disable quiet boot option.

Security

Set setup administrator password.

Save&Exit

Exit system setup after saving the changes.

Note:

1. If the "**Control LVDS2 (CH7511)**" has been set "**Disable**," and then, the screen cannot be switched to LVDS2 under the OS.

2. If the "**Control LVDS2 (CH7511)**" has been set "**Enable,**" and then, the screen can be switched to LVDS2 under the OS.

3. This model does not support LVDS2 output under DOS mode. So if it is a dual LVDS application, users have to enable "**Onboard LVDS 2**" on the LVDS1 panel under BIOS interface, and then, enter to the OS.

4. For LVDS1 + LVDS2 application, this model does not support scaling after entering the OS, users have to set the fixed resolution on their LCD Panel under BIOS interface, and then, enter to the OS.

Chapter

4

Driver Installation

The GENE-CV05 comes with a DVD-ROM that contains all drivers and utilities that meet your needs.

Follow the sequence below to install the drivers:

Step 1 – Install Chipset Driver

Step 2 – Install VGA Driver

Step 3 – Install LAN Driver

Step 4 – Install Audio Driver

Step 5 – Install AHCI Driver

Step 6 – Install TPM Driver

Step 7 – Install Touch Driver

4.1 Installation:

Insert the GENE-CV05 DVD-ROM into the DVD-ROM Drive. And install the drivers from Step 1 to Step 7 in order.

Step 1 – Install Chipset Driver

1. Click on the ***STEP1-CHIPSET*** folder and double click on the ***Setup.exe*** file
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

Step 2 – Install VGA Driver

1. Click on the ***STEP2-VGA*** folder and double click on the ***Setup.exe*** file
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

Step 3 – Install LAN Driver

1. Click on the ***STEP3-LAN*** folder and select the OS folder your system is
2. Double click on the ***setup.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 4 – Install Audio Driver

1. Click on the ***STEP4-AUDIO*** folder and select the OS folder your system is

2. Double click on the ***Setup.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 5 – Install AHCI Driver

Please refer to the Appendix D AHCI Setting

Step 6 – Install TPM Driver

1. Click on the ***STEP6-TPM*** folder and select the OS folder your system is
2. Double click on the ***Setup.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 7 – Install Touch Driver

1. Click on the ***STEP7-Touch*** folder and select the OS folder your system is
2. Double click on the ***Setup.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Appendix

A

Programming the Watchdog Timer

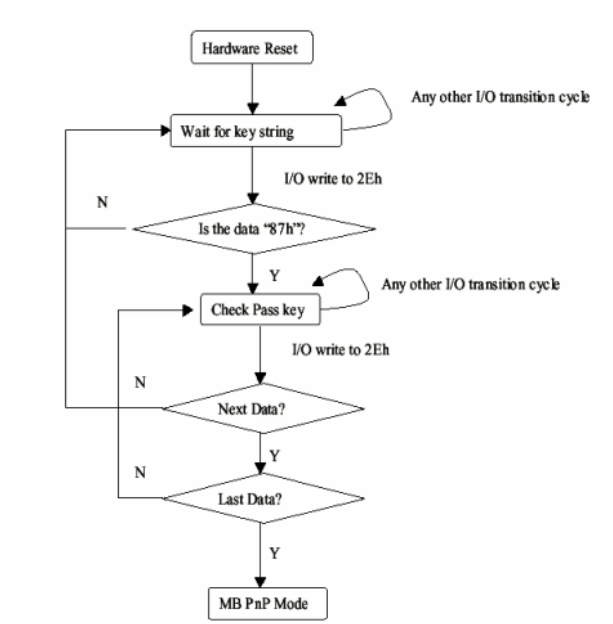
A.1 Programming

GENE-CV05 utilizes ITE 8783 chipset as its watchdog timer controller. Below are the procedures to complete its configuration and the AAEON initial watchdog timer program is also attached based on which you can develop customized program to fit your application.

Configuring Sequence Description

After the hardware reset or power-on reset, the ITE 8783 enters the

normal mode with all logical devices disabled except KBC. The initial state (enable bit) of this logical device (KBC) is determined by the state of pin 121 (DTR1#) at the falling edge of the system reset during power-on reset.



There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, four special I/O write operations are to be performed during Wait for Key state. To ensure the initial state of the key-check logic, it is necessary to perform four write opera-tions to the Special Address port (2EH). Two different enter keys are provided to select configuration ports (2Eh/2Fh) of the next step.

	Address Port	Data Port
87h, 01h, 55h, 55h:	2Eh	2Fh

(2) Modify the Data of the Registers

All configuration registers can be accessed after entering the MB PnP Mode. Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global registers.

(3) Exit the MB PnP Mode

Set bit 1 of the configure control register (Index=02h) to 1 to exit the MB PnP Mode.

WatchDog Timer Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
All	02h	W	NA	Configure Control

07h	71h	R/W	00h	Watch Dog Timer Control Register
07h	72h	R/W	001s0000b	Watch Dog Timer Configuration Register
07h	73h	R/W	38h	Watch Dog Timer Time-out Value (LSB) Register
07h	74h	R/W	00h	Watch Dog Timer Time-out Value (MSB) Register

Configure Control (Index=02h)

This register is write only. Its values are not sticky; that is to say, a hardware reset will automatically clear the bits, and does not require the software to clear them.

Bit	Description
7-2	**Reserved**
1	Returns to the "Wait for Key" state. This bit is used when the configuration sequence is completed.
0	Resets all logical devices and restores configuration registers to their power-on states.

Watch Dog Timer 1, 2, 3 Control Register (Index=71h,81h,91h Default=00h)

Bit	Description
7	**WDT Timeout Enable(WTE)** 1: Disable. 0: Enable.
6	**WDT Reset upon Mouse Interrupt(WRKMI)** 0: Disable. 1: Enable.
5	**WDT Reset upon Keyboard Interrupt(WRKBI)** 0: Disable. 1: Enable.
4	**Reserved**
3-2	**Reserved**
1	**Force Time-out(FTO)** This bit is self-clearing.
0	**WDT Status(WS)** 1: WDT value reaches 0. 0: WDT value is not 0.

Watch Dog Timer 1, 2, 3 Configuration Register (Index=72h, 82h, 92h Default=001s0000b)

Bit	Description
7	**WDT Time-out Value Select 1 (WTVS)** 1: Second 0: Minute
6	**WDT Output through KRST (Pulse) Enable(WOKE)** 1: Enable 0: Disable
5	**WDT Time-out value Extra select(WTVES)** 1: 64ms x WDT Timer-out value (default = 4s) 0: Determined by WDT Time-out value select 1 (bit 7 of this register)
4	**WDT Output through PWROK (Pulse) Enable(WOPE)** 1: Enable 0: Disable During LRESET#, this bit is selected by JP7 power-on strapping option
3-0	**Select interrupt level [Note1] for WDT(SIL)**

Watch Dog Timer 1,2,3 Time-Out Value (LSB) Register (Index=73h,83h,93h, Default=38h)

Bit	Description
7-0	**WDT Time-out Value 7-0(WTV)**

Watch Dog Timer 1,2,3 Time-Out Value (MSB) Register (Index=74h,84h,94h Default=00h)

Bit	Description
7-0	**WDT Time-out Value 15-8(WTV)**

A.2 ITE8783 Watchdog Timer Initial Program

```
.MODEL SMALL
.CODE
Main:
CALL Enter_Configuration_mode
CALL Check_Chip
mov cl, 7
call Set_Logic_Device
;time setting
mov cl, 10 ; 10 Sec
dec al
Watch_Dog_Setting:
;Timer setting
mov al, cl
mov cl, 73h
call Superio_Set_Reg
;Clear by keyboard or mouse interrupt
mov al, 0f0h
mov cl, 71h
call Superio_Set_Reg
;unit is second.
mov al, 0C0H
mov cl, 72h
```

```
call Superio_Set_Reg
; game port enable
mov cl, 9
call Set_Logic_Device

Initial_OK:
CALL Exit_Configuration_mode
MOV AH,4Ch
INT 21h

Enter_Configuration_Mode PROC NEAR
MOV SI,WORD PTR CS:[Offset Cfg_Port]

MOV DX,02Eh
MOV CX,04h
Init_1:
MOV AL,BYTE PTR CS:[SI]
OUT DX,AL
INC SI
LOOP Init_1
RET
Enter_Configuration_Mode ENDP

Exit_Configuration_Mode PROC NEAR
MOV AX,0202h
```

```
CALL Write_Configuration_Data
RET
Exit_Configuration_Mode ENDP

Check_Chip PROC NEAR

MOV AL,20h
CALL Read_Configuration_Data
CMP AL,87h
JNE Not_Initial

MOV AL,21h
CALL Read_Configuration_Data
CMP AL,81h
JNE Not_Initial

Need_Initial:
STC
RET
Not_Initial:
CLC
RET
Check_Chip ENDP
Read_Configuration_Data PROC NEAR
MOV DX,WORD PTR CS:[Cfg_Port+04h]
```

```
OUT DX,AL
MOV DX,WORD PTR CS:[Cfg_Port+06h]
IN AL,DX
RET
Read_Configuration_Data ENDP

Write_Configuration_Data PROC NEAR
MOV DX,WORD PTR CS:[Cfg_Port+04h]
OUT DX,AL
XCHG AL,AH
MOV DX,WORD PTR CS:[Cfg_Port+06h]
OUT DX,AL
RET
Write_Configuration_Data ENDP

Superio_Set_Reg proc near
push ax
MOV DX,WORD PTR CS:[Cfg_Port+04h]
mov al,cl
out dx,al
pop ax
inc dx
out dx,al
ret
Superio_Set_Reg endp.Set_Logic_Device proc near
```

```
Set_Logic_Device      proc      near
push ax
push cx
xchg al,cl
mov cl,07h
call Superio_Set_Reg
pop cx
pop ax
ret
Set_Logic_Device endp

;Select 02Eh->Index Port, 02Fh->Data Port
Cfg_Port DB 087h,001h,055h,055h
DW 02Eh,02Fh
```

END Main

Note: Interrupt level mapping

0Fh-Dh: not valid

0Ch: IRQ12

.

.

03h: IRQ3

02h: not valid

01h: IRQ1

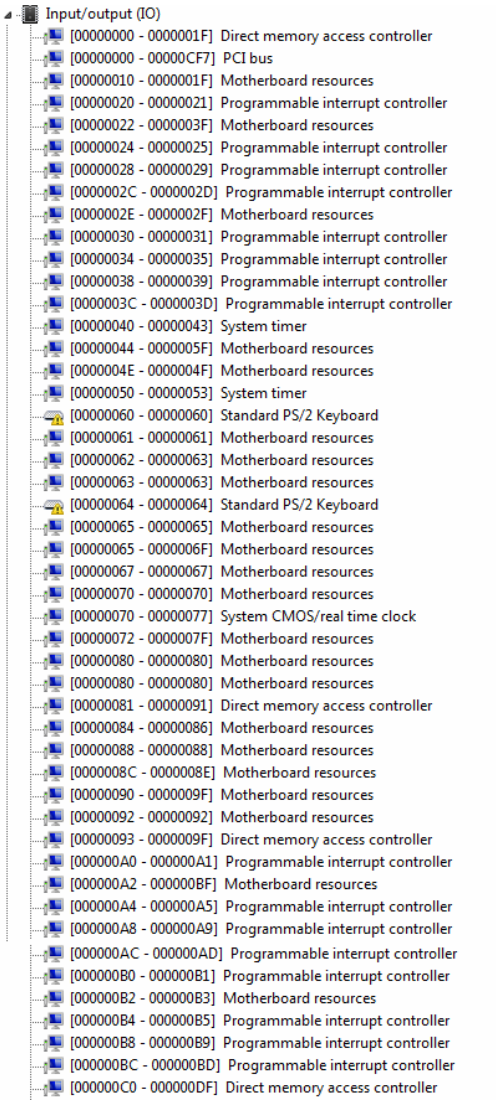
00h: no interrupt selected

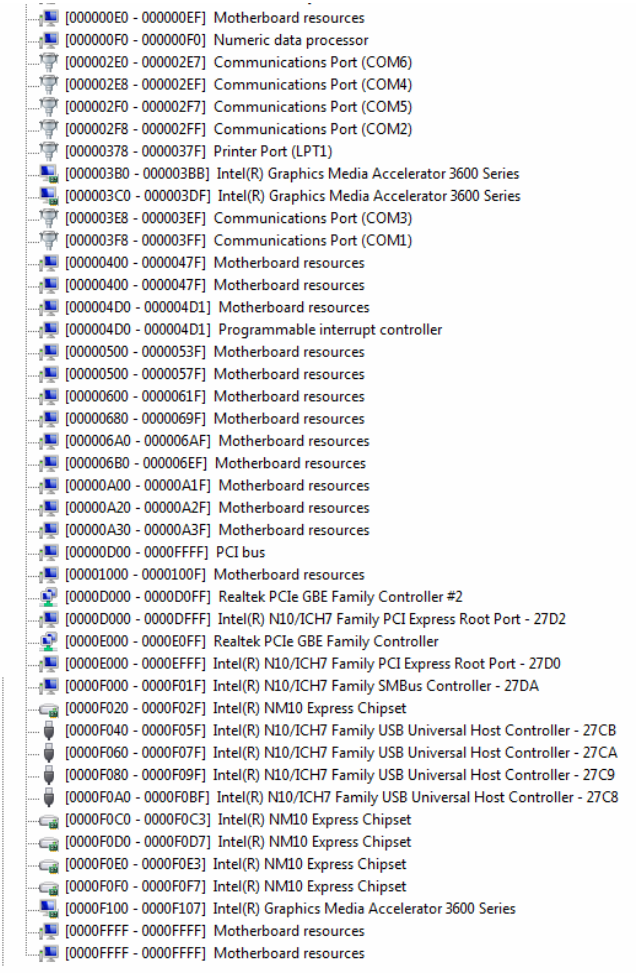
Appendix

B

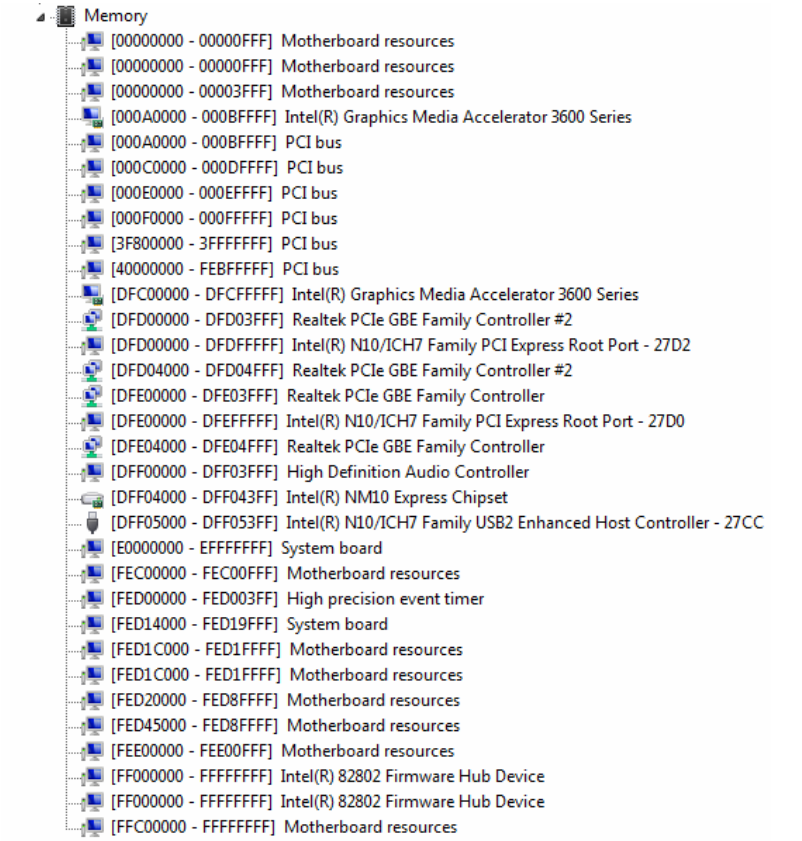
I/O Information

B.1 I/O Address Map

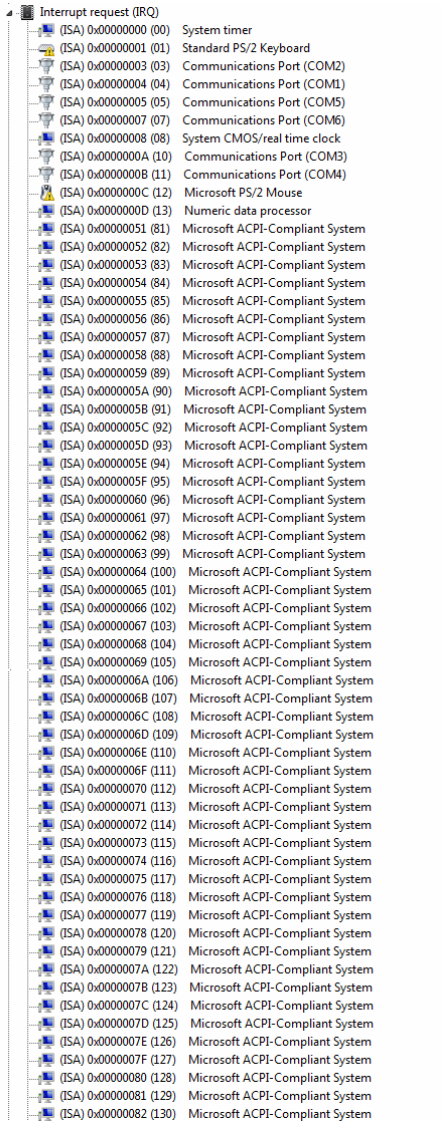


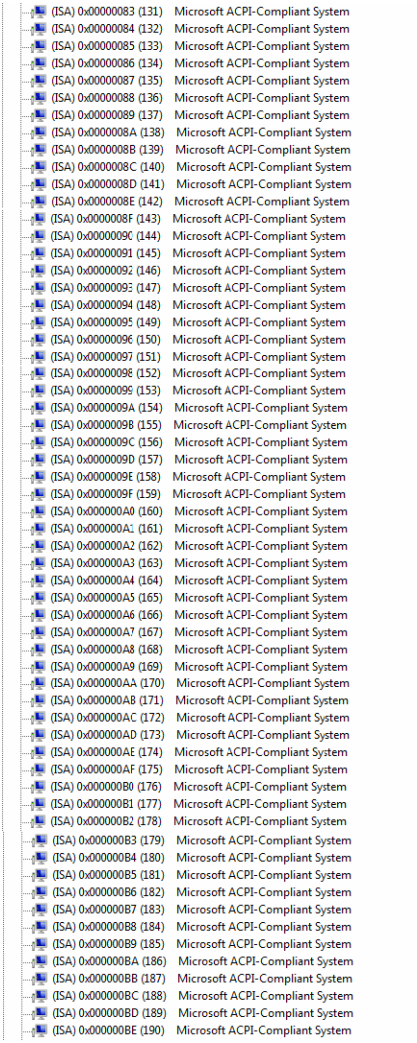

[000000E0 - 000000EF] Motherboard resources
[000000F0 - 000000F0] Numeric data processor
[000002E0 - 000002E7] Communications Port (COM6)
[000002E8 - 000002EF] Communications Port (COM4)
[000002F0 - 000002F7] Communications Port (COM5)
[000002F8 - 000002FF] Communications Port (COM2)
[00000378 - 0000037F] Printer Port (LPT1)
[000003B0 - 000003BB] Intel(R) Graphics Media Accelerator 3600 Series
[000003C0 - 000003DF] Intel(R) Graphics Media Accelerator 3600 Series
[000003E8 - 000003EF] Communications Port (COM3)
[000003F8 - 000003FF] Communications Port (COM1)
[00000400 - 0000047F] Motherboard resources
[00000400 - 0000047F] Motherboard resources
[000004D0 - 000004D1] Motherboard resources
[000004D0 - 000004D1] Programmable interrupt controller
[00000500 - 0000053F] Motherboard resources
[00000500 - 0000057F] Motherboard resources
[00000600 - 0000061F] Motherboard resources
[00000680 - 0000069F] Motherboard resources
[000006A0 - 000006AF] Motherboard resources
[000006B0 - 000006EF] Motherboard resources
[00000A00 - 00000A1F] Motherboard resources
[00000A20 - 00000A2F] Motherboard resources
[00000A30 - 00000A3F] Motherboard resources
[00000D00 - 0000FFFF] PCI bus
[00001000 - 0000100F] Motherboard resources
[0000D000 - 0000D0FF] Realtek PCIe GBE Family Controller #2
[0000D000 - 0000DFFF] Intel(R) N10/ICH7 Family PCI Express Root Port - 27D2
[0000E000 - 0000E0FF] Realtek PCIe GBE Family Controller
[0000E000 - 0000EFFF] Intel(R) N10/ICH7 Family PCI Express Root Port - 27D0
[0000F000 - 0000F01F] Intel(R) N10/ICH7 Family SMBus Controller - 27DA
[0000F020 - 0000F02F] Intel(R) NM10 Express Chipset
[0000F040 - 0000F05F] Intel(R) N10/ICH7 Family USB Universal Host Controller - 27CB
[0000F060 - 0000F07F] Intel(R) N10/ICH7 Family USB Universal Host Controller - 27CA
[0000F080 - 0000F09F] Intel(R) N10/ICH7 Family USB Universal Host Controller - 27C9
[0000F0A0 - 0000F0BF] Intel(R) N10/ICH7 Family USB Universal Host Controller - 27C8
[0000F0C0 - 0000F0C3] Intel(R) NM10 Express Chipset
[0000F0D0 - 0000F0D7] Intel(R) NM10 Express Chipset
[0000F0E0 - 0000F0E3] Intel(R) NM10 Express Chipset
[0000F0F0 - 0000F0F7] Intel(R) NM10 Express Chipset
[0000F100 - 0000F107] Intel(R) Graphics Media Accelerator 3600 Series
[0000FFFF - 0000FFFF] Motherboard resources
[0000FFFF - 0000FFFF] Motherboard resources

B.2 1st MB Memory Address Map

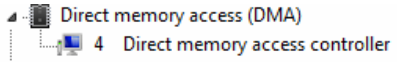


B.3 IRQ Mapping Chart





B.4 DMA Channel Assignments



Appendix

C

Mating Connector

C.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN2	External +5VSB Power Input and PS_ON#	JST	XHP-3	ATX Cable	170220020B
CN3	CPU Fan Connector	Molex	22-01-2035	N/A	N/A
CN4	+5VSB Output w/ SMBus	JST	PHR-6	ATX External 5VSB Cable	External AUX Power and PS_ON#
CN5	SATA	Molex	887505318	SATA Cable	1709070500
CN6	External 12V Input	Molex	19211-0003	Power Cable	1702002010
CN7	Digital I/O	Molex	51110-1050	N/A	N/A
CN8	Parallel Port	Molex	51110-2650	Parallel Cable	1701260200
CN9	+5V Output for SATA HDD using	JST	PHR-2	2 Pins For SATA Power	1702150155
CN10	USB Port #6	Molex	51021-0500	USB Wafer Cable	1700050207
CN11	COM Port #6	Molex	51021-0900	UART Wafer Cable	1701090150
CN12	USB Port #5	Molex	51021-0500	USB Wafer Cable	1700050207
CN13	COM Port #5	Molex	51021-0900	UART Wafer Cable	1701090150
CN14	USB Port #4	Molex	51021-0500	USB Wafer Cable	1700050207
CN15	USB Port #3	Molex	51021-0500	USB Wafer Cable	1700050207
CN16	COM Port #4	Molex	51021-0900	UART Wafer	1701090150

				Cable	
CN17	LPC Expansion I/F	JST	SHR-12V-S-B	AAEON LPC Cable	1703120130
CN18	COM Port #3	Molex	51021-0900	UART Wafer Cable	1701090150
CN19	COM Port #2	Molex	51021-0900	UART Wafer Cable	1701090150
CN20	Touch Screen	JST	SHR-9V-S-B	N/A	N/A
CN21	Stereo-R Channel	Molex	51021-0200	N/A	N/A
CN22	2nd LVDS (Dual channel 18/24bit)	HIROSE	DF13-30DS-1.25C	N/A	N/A
CN23	PS/2 Keyboard & Mouse	JST	PHDR-06VS	KB/MS Cable	1700060152
CN24	2nd LVDS Inverter	JST	PHR-5	Invertor Cable	1705050153
CN25	Stereo-L Channel	Molex	51021-0200	N/A	N/A
CN26	1st LVDS Inverter	JST	PHR-5	Invertor Cable	1705050153
CN27	1st LVDS (Single channel 18/24bit)	HIROSE	DF13-30DS-1.25C	N/A	N/A
CN28	2nd RJ-45 Ethernet	Molex	90075-0141	N/A	N/A
CN29	1st RJ-45 Ethernet	Molex	90075-0141	N/A	N/A
CN31	Audio Line In/Out and MIC Connector	Molex	51021-1000	Audio Cable	1709100254
BAT1	External RTC Connector	Molex	51021-0200	Battery Cable	175011901C

Appendix

D

AHCI Setting

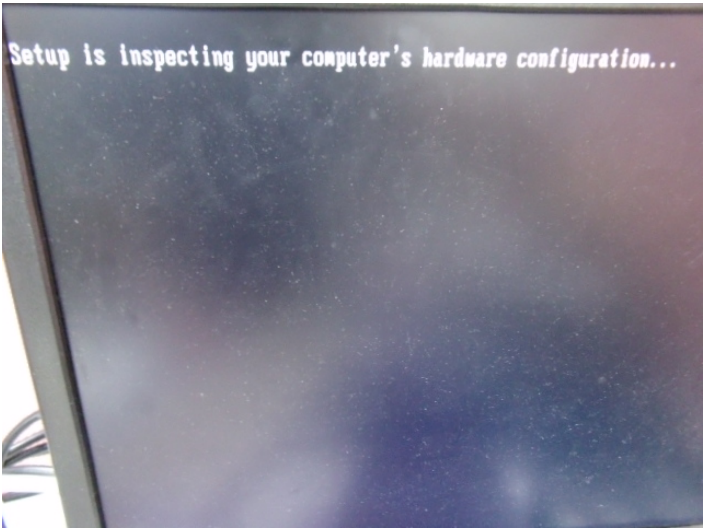
D.1 Setting AHCI

OS installation to setup AHCI Mode.

Step 1: Copy the files below from “Driver CD -> STEP5-AHCI\WIN7_32\F6 Install Floppy Create for 32 and 64 bit Windows” to Disk

Step 2: Connect the USB Floppy to the board

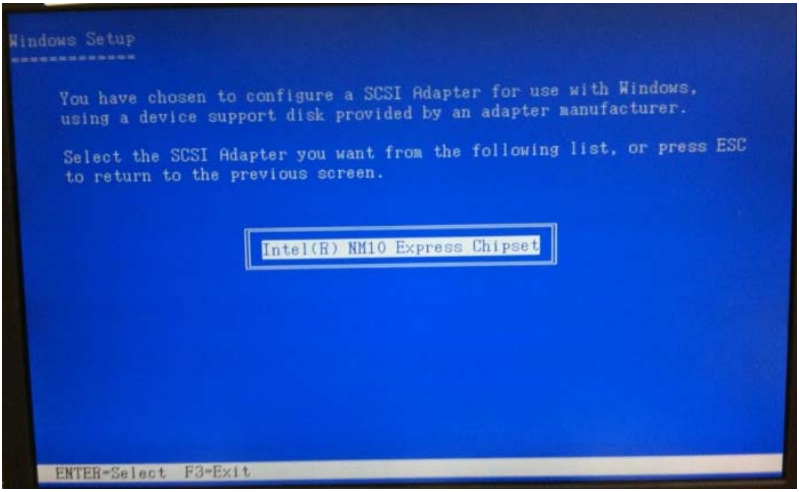
Step 3: Setup OS



Step 4: Press "**F6**"

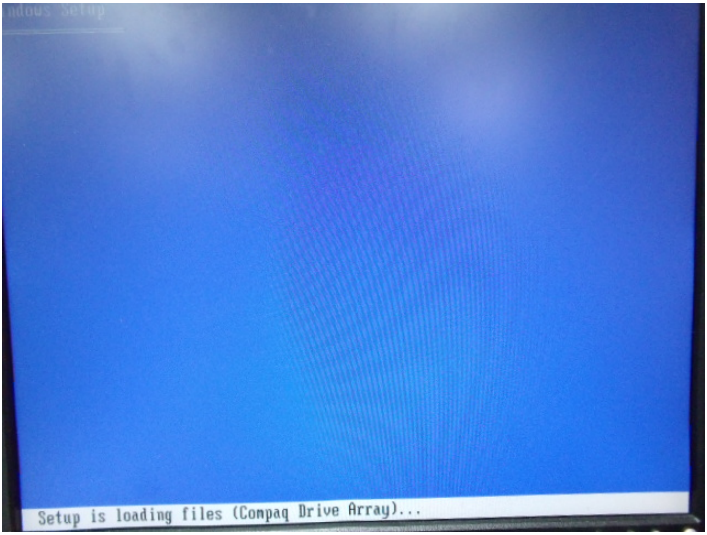
Step 5: Choose "**S**"

Step 6: Choose "**Intel(R) NM10 Express Chipset**"



Step 7: It will show the model number you select and then press “**ENTER**

Step 8: Setup is loading files



Appendix

E

Digital I/O

E.1 Digital I/O

The F75111 provides one serial access interface, I2C Bus, to read/write internal registers. The address of Serial Bus is 0x6E (0110_1110)

The related register for configuring DIO is list as follows:

Configuration and Control Register-Index 01h

Power-on default [7:0]=0000_1000b

Bit	Name	R/W	PWR	Description
7	INIT	R/W	VSB3V	Software reset for all registers including Test Mode registers. Users use only.
6	Reserved	R/W	VSB3V	
5	EN_WDT10	R/W	VSB3V	Enable Reset Out. If set to 1, enable WDTOUT10# output. Default is disable.
4	Reserved	R/W	VSB3V	
3	Reserved	R/W	VSB3V	
2	Reserved	R/W	VSB3V	
1	SMART_POWR_MAGEMENT	R/W	VSB3V	Set this bit to 1 will enable auto power down mode, when all function are idle then 20ms the chip will auto power down, it will wakeup when GPIO state change or read write register
0	SOFT_POWR_DOWN	R/W	VSB3V	Set this bit to 1 will power down all of the analog block and stop internal clock, write 0 to clear this bit or when GPIO state change will auto clear this bit to 0.

GPIO2x Output Control Register-Index 20h

Power-on default [7:0]=0000_0000b

Bit	Name	R/W	PWR	Description
7	GP27_OCTRL	R/W	VSB3V	GPIO 27 output control. Set to 1 for output function. Set to 0 for input function (default).
6	GP26_OCTRL	R/W	VSB3V	GPIO 26 output control. Set to 1 for output function. Set to 0 for input function (default).
5	GP25_OCTRL	R/W	VSB3V	GPIO 25 output control. Set to 1 for output function. Set to 0 for input function (default).
4	GP24_OCTRL	R/W	VSB3V	GPIO 24 output control. Set to 1 for output function. Set to 0 for input function (default).
3	GP23_OCTRL	R/W	VSB3V	GPIO 23 output control. Set to 1 for output function. Set to 0 for input function (default).
2	GP22_OCTRL	R/W	VSB3V	GPIO 22 output control. Set to 1 for output function. Set to 0 for input function (default).
1	GP21_OCTRL	R/W	VSB3V	GPIO 21 output control. Set to 1 for output function. Set to 0 for input function (default).
0	GP20_OCTRL	R/W	VSB3V	GPIO 20 output control. Set to 1 for output function. Set to 0 for input function (default).

GPIO2x Output Data Register-Index 21h

Power-on default [7:0]=0000_0000b

Bit	Name	R/W	PWR	Description
7	GP27_ODATA	R/W	VSB3V	GPIO 27 output data.
6	GP26_ODATA	R/W	VSB3V	GPIO 26 output data.
5	GP25_ODATA	R/W	VSB3V	GPIO 25 output data.

4	GP24_ODATA	R/W	VSB3V	GPIO 24 output data.
3	GP23_ODATA	R/W	VSB3V	GPIO 23 output data.
2	GP22_ODATA	R/W	VSB3V	GPIO 22 output data.
1	GP21_ODATA	R/W	VSB3V	GPIO 21 output data.
0	GP20_ODATA	R/W	VSB3V	GPIO 20 output data.

GPIO2x Input Status Register-Index 22h

Power-on default [7:0]=xxxx_xxxxb

Bit	Name	R/W	PWR	Description
7	GP27_PSTS	RO	VSB3V	Read the GPIO27 data on the pin.
6	GP26_PSTS	RO	VSB3V	Read the GPIO26 data on the pin.
5	GP25_PSTS	RO	VSB3V	Read the GPIO25 data on the pin.
4	GP24_PSTS	RO	VSB3V	Read the GPIO24 data on the pin.
3	GP23_PSTS	RO	VSB3V	Read the GPIO23 data on the pin.
2	GP22_PSTS	RO	VSB3V	Read the GPIO22 data on the pin.
1	GP21_PSTS	RO	VSB3V	Read the GPIO21 data on the pin.
0	GP20_PSTS	RO	VSB3V	Read the GPIO20 data on the pin.

The following is a sample code for 8 input

```
.MODEL          SMALL
.CODE
```

```
begin:
                mov    cl,01h
                mov    al,80h
                call   CT_I2CWriteByte
                call   Delay5ms

            mov al,00h
                mov    cl,20h
                call   CT_I2CWriteByte

                mov    cl,22h
                call   CT_I2CReadByte

;Input  : CL - register index
;              CH - device ID
;Output : AL - Value read

Ct_I2CReadByte      Proc    Near
                mov    ch,06eh
                mov        dx, 0f000h + 00h ; Host Control Register
              mov        al, 0ffh                        ; Clear previous
commands
              out        dx, al
```

```
        call    Delay5ms

        mov     dx, 0f000h + 04h        ; Transmit Slave Address
Register
        inc     ch                      ; Set the slave address and
        mov     al, ch                  ; prepare for a READ command
        out     dx, al

        mov     dx, 0f000h + 03h        ; Host Command Register
        mov     al, cl                  ; offset to read
        out     dx, al

        mov     dx, 0f000h + 05h
      xor       al, al                  ; Clear old data
      out       dx, al

        mov     dx, 0f000h + 02h ; Host Control Reegister
        mov     al, 48h     ; Start a byte access
        out     dx, al

        call    CT_Chk_SMBus_Ready
        mov     dx, 0f000h + 05h
        in      al, dx

        ret
```

```
Ct_I2CReadByte      Endp

;Input : CL - register index
;           CH - device ID
;           AL - Value to write
;Output: none

Ct_I2CWriteByte     Proc    Near
                    mov     ch,06eh
                    xchg    ah, al
                    mov         dx, 0f000h + 00h ; Host Control Register
                  mov         al, 0ffh                        ; Clear previous
commands
                  out         dx, al

                    call      Delay5ms

                    mov         dx, 0f000h + 04h          ; Transmit Slave Address
Register
                    mov     al, ch                  ; Set the slave address and
                    out         dx, al                          ; prepare for a WRITE
command

                    mov         dx, 0f000h + 03h          ; Host Command Register
                    mov         al, cl                          ; offset to write
```

```
                out     dx, al

                mov     dx, 0f000h + 05h
                mov     al, ah
              out       dx, al

                mov       dx, 0f000h + 00h ; Host Control Register
                mov       al, 48h      ; Start a byte access
                out       dx, al

                call    CT_Chk_SMBus_Ready
                ret
Ct_I2CWriteByte     Endp

; Wait until the busy bit clears, indicating that the SMBUS
; activity has concluded.

CT_Chk_SMBus_Ready    Proc    Near
                mov     dx,0f000h+ 0;status port
                clc
                mov     cx,0800h
Chk_I2c_OK:
                in      al,dx           ;get status
                call    Delay5ms
```

```
                out     dx,al           ;clear status
                call    Delay5ms

                test    al, 02H                 ;termination of command ?
                jnz     short Clear_final

                and     al, NOT 40H  ;mask INUSE bit
                or      al,al           ;status OK ?
                jz      short Clear_final

                test    al,04h          ;device error
                jnz     short SMBus_Err

                loop    short Chk_I2c_OK
        ;SMbus error due to timeout
SMBus_Err:

                stc
                ret
Clear_final:
                clc
                ret
CT_Chk_SMBus_Ready    Endp

END    begin
```