GENE-BSW5

3.5″ Subcompact Board

User's Manual 1st Ed

Last Updated: November 30, 2015

Copyright Notice

Acknowledgement

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● GENE-BSW5 subcompact board	1
● Product DVD with User's Manual (in pdf) and drivers	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	×	O	O	O	O	O
外部信号 连接器及线材	×	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在
SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出
SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	X	O	O	O	O	O
Wires & Connectors for External Connections	X	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	3.5"
Processor	Intel® Pentium® N3150 SoC
System Memory	204-pin DDR3L 1600 SODIMM x 1, up to 8 GB
Chipset	Intel® Pentium® N3150 SoC
I/O Chipset	Fintek F81866D-I
Ethernet	Realtek RTL-8111E, 10/100/1000Base, RJ-45 x 2
BIOS	UEFI
Wake On LAN	Yes
Watchdog Timer	255 levels
H/W Status Monitoring	Fintek F81866D-I
Expansion Interface	MiniCard slot x 2 (half-sized mSATA x 1, full sized MiniCard x 1 by default)
Power Requirement	DC 12 V, AT or ATX
Board Size	146 x 101.7 mm (5.75 x 4")
Gross Weight	0.4 kg (0.88 lb)
Operating Temperature	0 ~ 60°C (32 ~ 140°F)
Storage Temperature	-40 ~ 81°C (-40 ~ 176°F)

● Operation Humidity	0 ~ 90% relative humidity, non condensing
● Certification	CE/FCC

Display

● Chipset	Intel® Pentium® N3150 SoC
● Resolution	HDMI Up to 2560 x 1600 @60 Hz, 3840 x 2160 @30Hz LVDS up to 1920 x 1200@ 60 Hz VGA up to 2560 x 1600 @ 60 Hz
● Video Output	LVDS x 2 + VGA (HDMI is optional, shared with LVDS2)
● Backlight Inverter Supply	PWM 5V/12V for LVDS x 2

I/O

● Storage	SATA 6.0 Gb/s x 1
● USB	USB 3.0 x 2 USB 2.0 x 3
● Serial Port	RS-232 x 4 RS-232/422/485 x 2 (Ring/ +5V/ +12V), RS-485 with auto flow
● Parallel Port	SPP/EPP/ECP x 1 (optional, shared with DI/O)
● DI/O	8-bit digital I/O (programmable)
● SIM Card Slot	SIM card slot x 1
● PS/2 Port	Keyboard x 1, mouse x 1
● Audio	Realtek ALC892

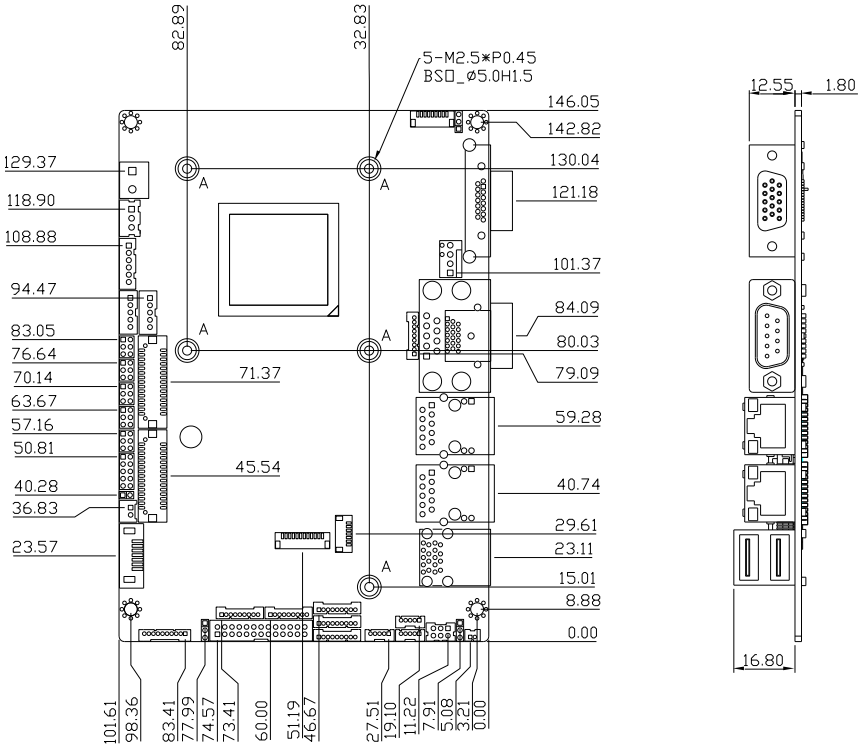
- **Touchscreen** 4/5/8-wire resistive touchscreen (USB interface)

Chapter 2

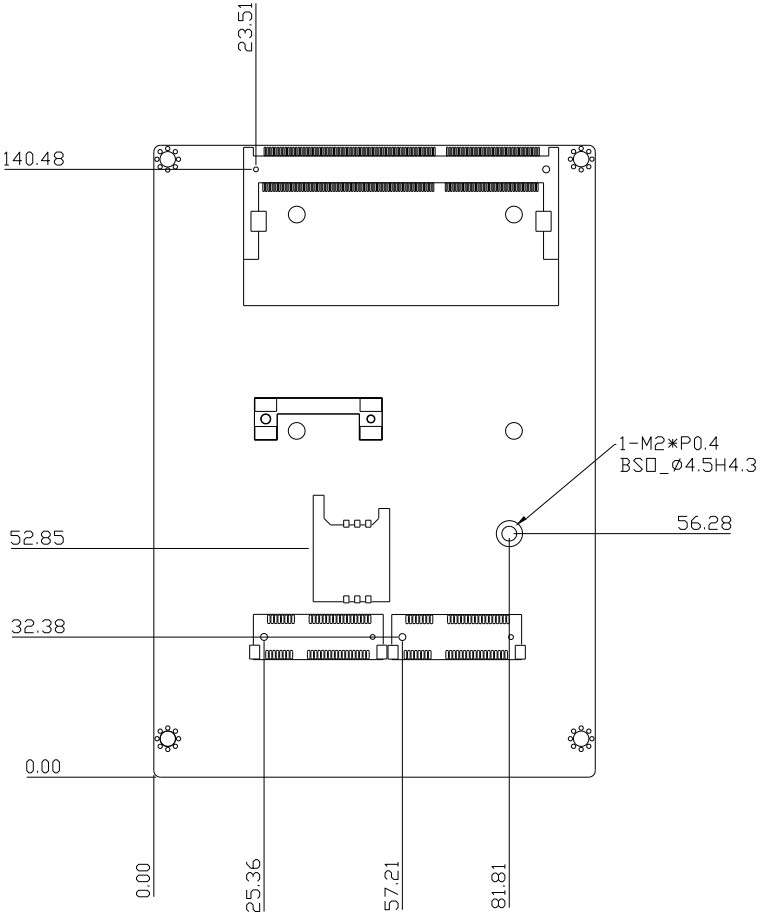
Hardware Information

2.1 Dimensions

Component Side

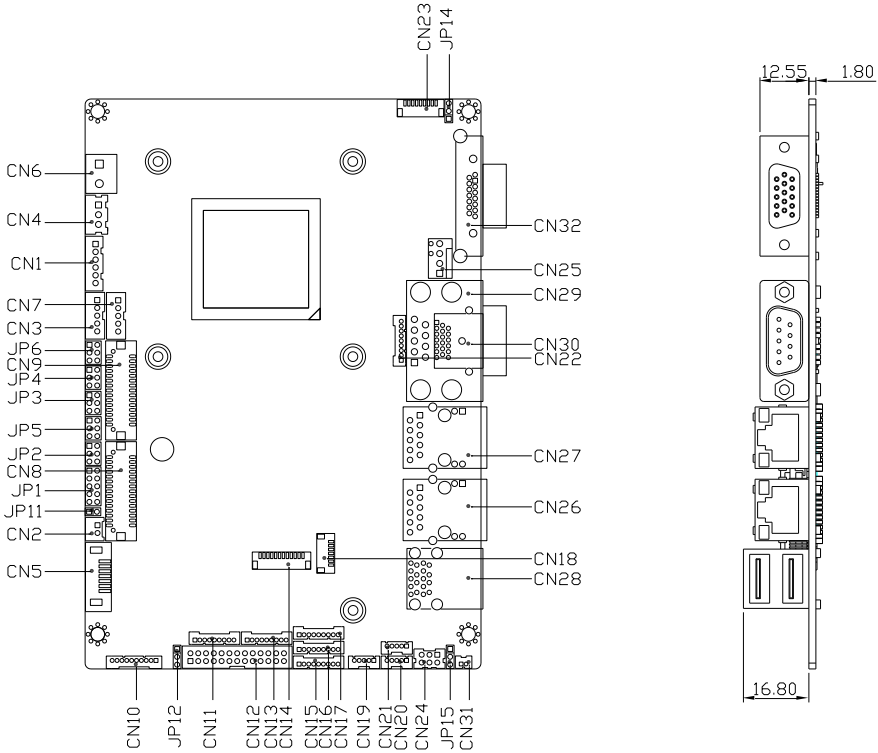


Solder Side

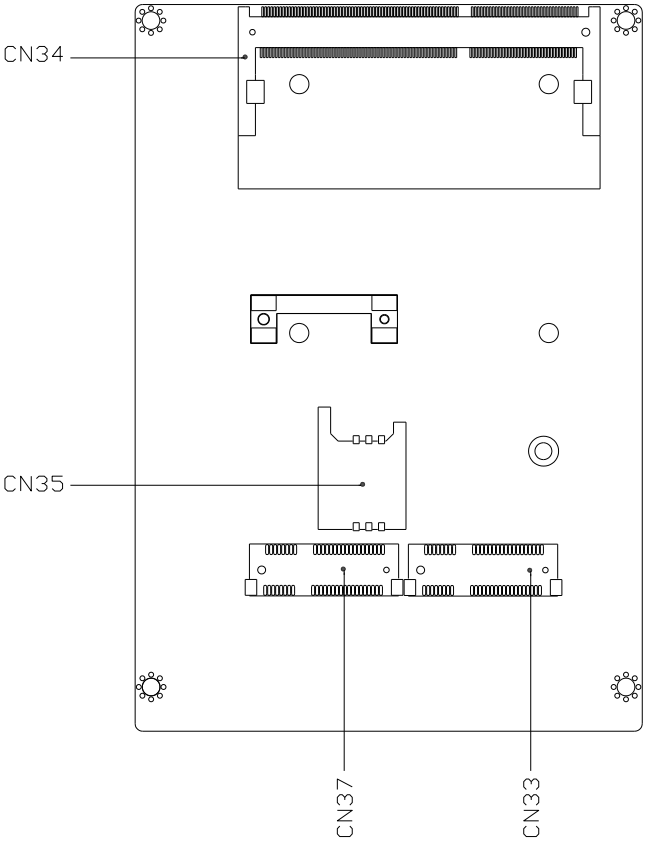

23.51
140.48
1-M2*P0.4
BS□_Ø4.5H4.3
56.28
52.85
32.38
0.00
0.00
25.36
57.21
81.81

2.2 Jumpers and Connectors

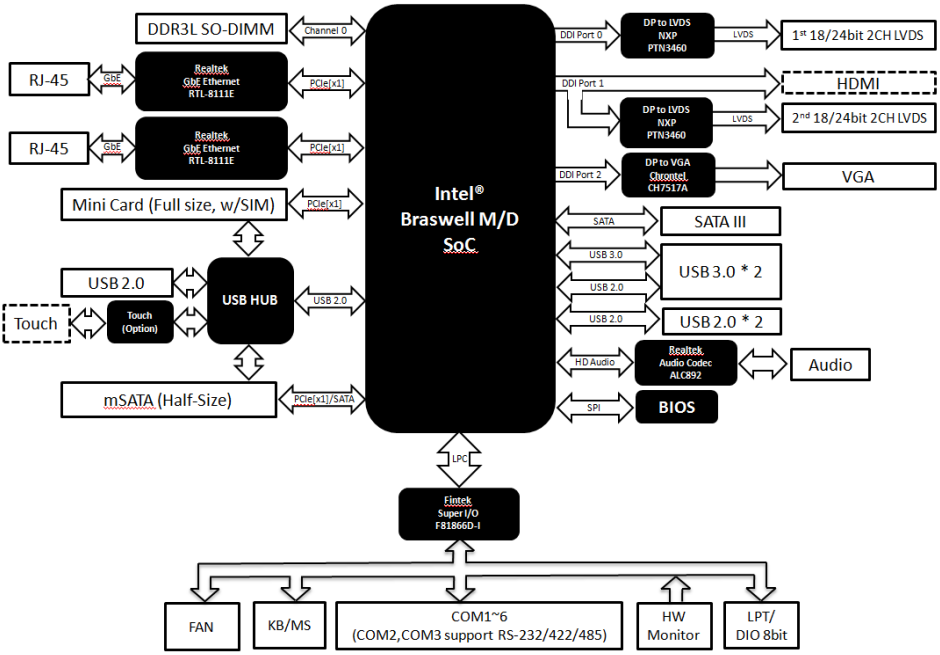
Component Side



Solder Side



2.3 Block Diagram

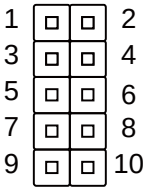


2.4 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application

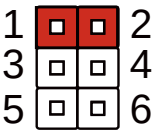
Label	Function
JP1	Front Panel Connector
JP2	COM3 Pin8 Function Selection
JP3	LVDS Port Backlight Inverter VCC Selection
JP4	LVDS Port Operating VDD Selection
JP5	COM2 Pin8 Function Selection
JP6	LVDS Port Backlight Lightness Control Mode Selection
JP11	Flash Descriptor Security
JP12	Auto Power Button Enable/Disable Selection
JP14	Touch Screen 4/5/8-wire Mode Selection
JP15	Clear CMOS Jumper

2.4.1 Front Panel Connector (JP1)

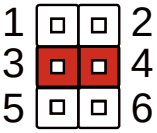


Pin	Pin Name	Pin	Pin Name
1	PWR_BTN-	2	PWR_BTN+
3	HDD_LED-	4	HDD_LED+
5	SPEAKER-	6	SPEAKER+
7	PWR_LED-	8	PWR_LED+
9	H/W RESET-	10	H/W RESET+

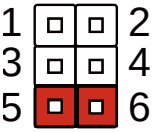
2.4.2 COM3 Function Selection (JP2)



+12V



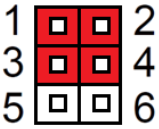
Ring(Default)



+5V

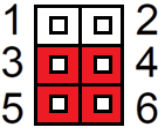
2.4.3 LVDS Port Backlight Inverter VCC Selection (JP3)

+12V



LVDS (2-4)
LVDS2 (1-3)

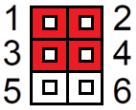
+5V



LVDS (4-6)
LVDS2 (3-5)

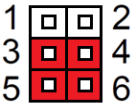
2.4.4 LVDS Port Operating VDD Selection (JP4)

+5V



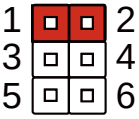
LVDS (2-4)
LVDS2 (1-3)

+3.3V

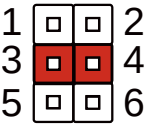


LVDS (4-6)
LVDS2 (3-5)

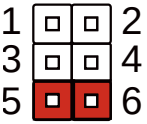
2.4.5 COM2 Function Selection (JP5)



+12V



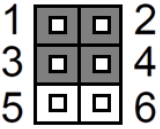
Ring(Default)



+5V

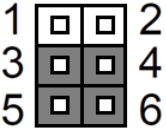
2.4.6 LVDS Port Backlight Lightness Control Selection (JP6)

LVDS_BKLCTL_CON



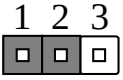
LVDS (2-4)
LVDS2 (1-3)

BKLT_CTRL_VR

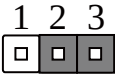


LVDS (4-6)
LVDS2 (3-5)

2.4.7 Auto Power Button Enable/Disable Selection (JP12)

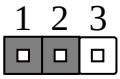


ATX Mode

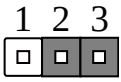


AT Mode (Default)

2.4.8 Touchscreen 4/5/8-wire Selection (JP14)

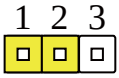


4/8 Wires Mode (Default)

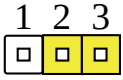


5 Wires Mode

2.4.9 Clear CMOS Jumper (JP15)



Normal (Default)



Clear CMOS

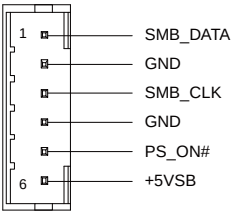
2.5 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	+5VSB Output w/SMBus
CN2	+5V Output for SATA HDD
CN3	LVDS Port Inverter / Backlight Connector
CN4	PSON# Port
CN5	3.0 SATA Port
CN6	External +12V Input
CN7	LVDS2 Port Inverter / Backlight Connector
CN8	LVDS2 Port
CN9	LVDS Port
CN10	Audio I/O Port
CN11	COM Port 2
CN12	LPT Port / 8bit DIO
CN13	COM Port 3
CN14	LPC Port
CN15	COM Port 6
CN16	COM Port 5
CN17	COM Port 4
CN18	SPI Debug Port
CN19	USB 2.0 Port 3
CN20	USB 2.0 Port 2
CN21	USB 2.0 Port 4
CN22	COM Port 1
CN23	Touch Screen Connector

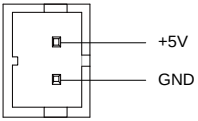
CN24	PS/2 Keyboard/Mouse Combo Port
CN25	CPU FAN (Optional)
CN26	LAN (RJ-45) Port1
CN27	LAN (RJ-45) Port2
CN28	USB Ports 0 and 1
CN29	COM Port 1 (D-SUB 9)
CN30	HDMI Port
CN31	Battery
CN32	VGA Port
CN33	MiniCard Slot (Half-MiniCard)
CN34	DDR3L SO-DIMM Slot
CN35	UIM Card Socket
CN37	MiniCard Slot (Full-MiniCard)

2.5.1 +5 VSB Output w/SMBus (CN1)



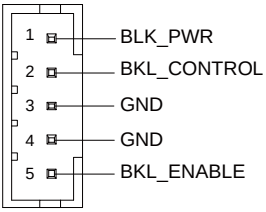
Pin	Pin Name	Signal Type	Signal level
1	SMB_DATA	I/O	+3.3V
2	GND	GND	
3	SMB_CLK	I/O	+3.3V
4	GND	GND	
5	PS_ON#	OUT	+3.3V
6	+5VSB	PWR	+5V

2.5.2 +5V Output for SATA HDD (CN2)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	GND	GND	

2.5.3 LVDS Port Inverter / Backlight Connector (CN3)

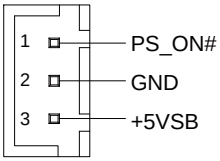


Pin	Pin Name	Signal Type	Signal Level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_CONTROL	OUT	
3	GND	GND	
4	GND	GND	
5	BKL_ENABLE	OUT	+3.3V

* LVDS BKL_PWR can be set to +5V or +12V by JP6.

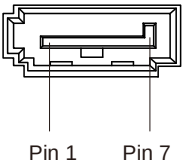
* LVDS BKL_CONTROL can be set by JP6.

2.5.4 External +5VSB Inout (CN4)



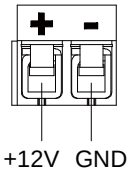
Pin	Pin Name	Signal Type	Signal Level
1	PS_ON#	OUT	+3.3V
2	GND	GND	
3	+5VSB	PWR	+5V

2.5.5 SATA Port 1 (CN5)



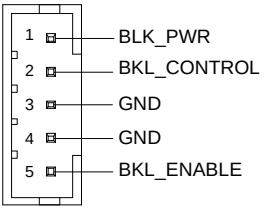
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.5.6 External +12V Input (CN6)



Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	

2.5.7 LVDS2 Port Inverter / Backlight Connector (CN7)

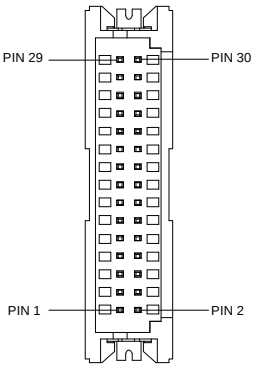


Pin	Pin Name	Signal Type	Signal Level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_CONTROL	OUT	
3	GND	GND	
4	GND	GND	
5	BKL_ENABLE	OUT	+3.3V

* LVDS BKL_PWR can be set to +5V or +12V by JP6.

* LVDS BKL_CONTROL can be set by JP6.

2.5.8 LVDS2 Port (CN8)

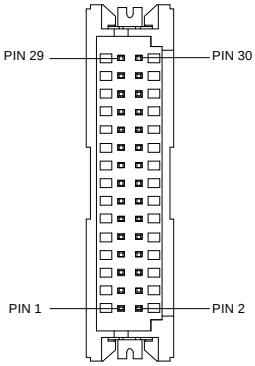


* LVDS LCD_PWR can be set to +3.3V or +5V by JP3.

Pin	Pin Name	Signal Type	Signal level
1	BKL_ENABLE	OUT	
2	BKL_CONTROL	OUT	

3	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	
5	LVDS_A_CLK-	DIFF	
6	LVDS_A_CLK+	DIFF	
7	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	
9	LVDS_DA0-	DIFF	
10	LVDS_DA0+	DIFF	
11	LVDS_DA1-	DIFF	
12	LVDS_DA1+	DIFF	
13	LVDS_DA2-	DIFF	
14	LVDS_DA2+	DIFF	
15	LVDS_DA3-	DIFF	
16	LVDS_DA3+	DIFF	
17	DDC_DATA	I/O	+3.3V
18	DDC_CLK	I/O	+3.3V
19	LVDS_DB0-	DIFF	
20	LVDS_DB0+	DIFF	
21	LVDS_DB1-	DIFF	
22	LVDS_DB1+	DIFF	
23	LVDS_DB2-	DIFF	
24	LVDS_DB2+	DIFF	
25	LVDS_DB3-	DIFF	
26	LVDS_DB3+	DIFF	
27	LCD_PWR	PWR	+3.3V/+5V
28	GND	GND	
29	LVDS_B_CLK-	DIFF	
30	LVDS_B_CLK+	DIFF	

2.5.9 LVDS Port (CN9)

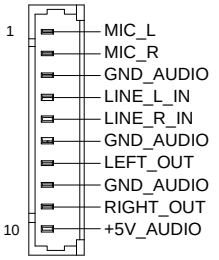


* LVDS LCD_PWR can be set to +3.3V or +5V by JP3.

Pin	Pin Name	Signal Type	Signal level
1	BKL_ENABLE	OUT	
2	BKL_CONTROL	OUT	
3	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	
5	LVDS_A_CLK-	DIFF	
6	LVDS_A_CLK+	DIFF	
7	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	
9	LVDS_DA0-	DIFF	
10	LVDS_DA0+	DIFF	
11	LVDS_DA1-	DIFF	
12	LVDS_DA1+	DIFF	
13	LVDS_DA2-	DIFF	
14	LVDS_DA2+	DIFF	
15	LVDS_DA3-	DIFF	
16	LVDS_DA3+	DIFF	
17	DDC_DATA	I/O	+3.3V

Pin	Pin Name	Signal Type	Signal level
18	DDC_CLK	I/O	+3.3V
19	LVDS_DB0-	DIFF	
20	LVDS_DB0+	DIFF	
21	LVDS_DB1-	DIFF	
22	LVDS_DB1+	DIFF	
23	LVDS_DB2-	DIFF	
24	LVDS_DB2+	DIFF	
25	LVDS_DB3-	DIFF	
26	LVDS_DB3+	DIFF	
27	LCD_PWR	PWR	+3.3V/+5V
28	GND	GND	
29	LVDS_B_CLK-	DIFF	
30	LVDS_B_CLK+	DIFF	

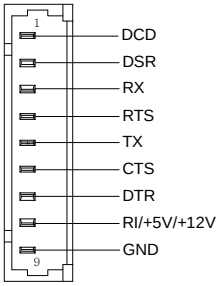
2.5.10 Audio I/O Port (CN10)



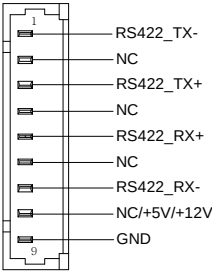
Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	IN	
2	MIC_R	IN	
3	GND_AUDIO	GND	
4	LINE_L_IN	IN	
5	LINE_R_IN	IN	

6	GND_AUDIO	GND	
7	LEFT_OUT	OUT	
8	GND_AUDIO	GND	
9	RIGHT_OUT	OUT	
10	+5V_AUDIO	PWR	+5V

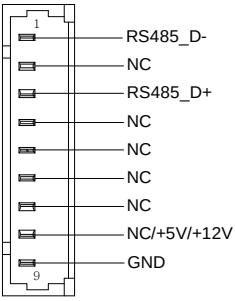
2.5.11 COM Port 2 (CN11)



RS-232			
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±5V
5	TX	OUT	±5V
6	CTS	IN	
7	DTR	OUT	±5V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	



RS-422			
Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	



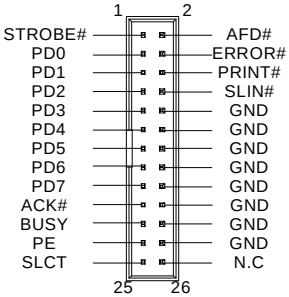
RS-485			
Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		

3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

* COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

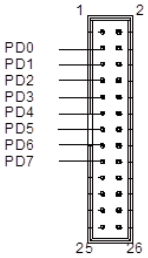
* Pin 8 function can be set by JP5.

2.5.12 LPT Port / 8 bit DIO (CN12)



LPT Port			
Pin	Pin Name	Signal Type	Signal Level
1	STROBE#	IN	
2	AFD#	I/O	
3	PD0	I/O	
4	ERROR#	IN	
5	PD1	I/O	
6	PRINT#	I/O	
7	PD2	I/O	
8	SLIN#	I/O	

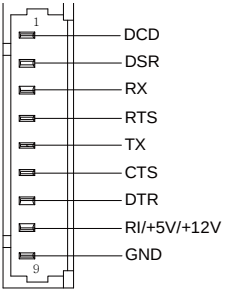
9	PD3	I/O
10	GND	GND
11	PD4	I/O
12	GND	GND
13	PD5	I/O
14	GND	GND
15	PD6	I/O
16	GND	GND
17	PD7	I/O
18	GND	GND
19	ACK#	IN
20	GND	GND
21	BUSY	IN
22	GND	GND
23	PD8	IN
24	GND	GND
25	SLCT	IN
26	NC	



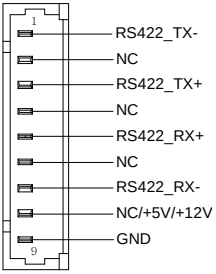
8-bit DI/O			
Pin	Pin Name	Signal Type	Signal Level
3	GPIO0	I/O	

5	GPIO1	I/O
7	GPIO2	I/O
9	GPIO3	I/O
11	GPIO4	I/O
13	GPIO5	I/O
15	GPIO6	I/O
17	GPIO7	I/O

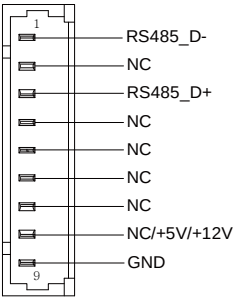
2.5.13 COM Port 3 (CN13)



RS-232			
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±5V
5	TX	OUT	±5V
6	CTS	IN	
7	DTR	OUT	±5V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	



RS-422			
Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	



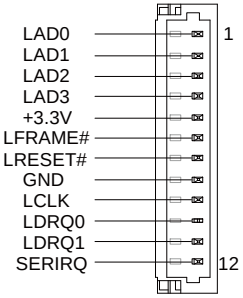
RS-485			
Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		

3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

* COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

* Pin 8 function can be set by JP5.

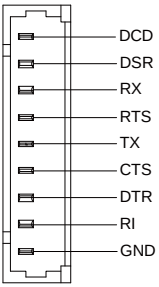
2.5.14 LPC Port (CN14)



Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	

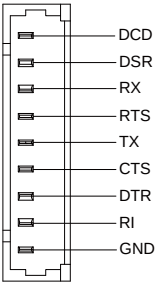
10	LDRQ0	IN	
11	LDRQ1	IN	
12	SERIRQ	I/O	+3.3V

2.5.15 COM Port 6 (CN15)



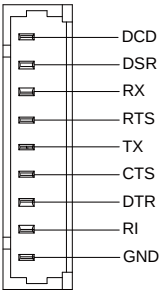
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±9V
5	TX	OUT	±9V
6	CTS	IN	
7	DTR	OUT	±9V
8	RI	IN	
9	GND	GND	

2.5.16 COM Port 5 (CN16)



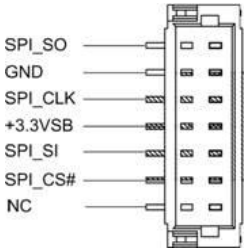
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±9V
5	TX	OUT	±9V
6	CTS	IN	
7	DTR	OUT	±9V
8	RI	IN	
9	GND	GND	

2.5.17 COM Port 4 (CN17)



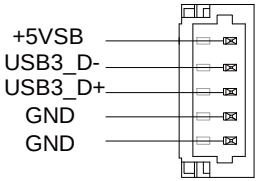
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±9V
5	TX	OUT	±9V
6	CTS	IN	
7	DTR	OUT	±9V
8	RI	IN	
9	GND	GND	

2.5.18 BIOS Debug Port (CN18)



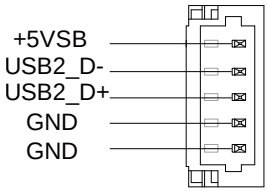
Pin	Pin Name	Signal Type	Signal Level
1	SPI_SO	OUT	
2	GND	GND	
3	SPI_CLK	IN	
4	+3.3VSB	PWR	+3.3V
5	SPI_SI	IN	
6	SPI_CS#	IN	
7	NC		

2.5.19 USB 2.0 Port 3 (CN19)



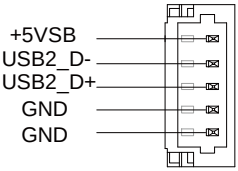
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB3_D-	DIFF	
3	USB3_D+	DIFF	
4	GND	GND	
5	GND	GND	

2.5.20 USB 2.0 Port 2 (CN20)



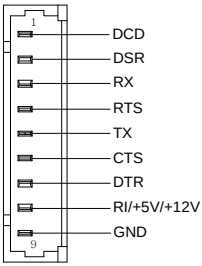
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB2_D-	DIFF	
3	USB2_D+	DIFF	
4	GND	GND	
5	GND	GND	

2.5.21 USB 2.0 Port 4 (CN21)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB4_D-	DIFF	
3	USB4_D+	DIFF	
4	GND	GND	
5	G ND	GND	

2.5.22 COM Port 1 (CN22)



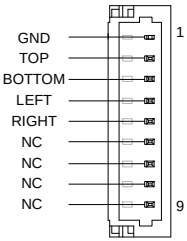
RS-232			
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±5V
5	TX	OUT	±5V
6	CTS	IN	

7	DTR	OUT	±5V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	

* COM1 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

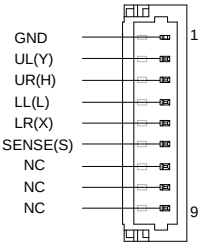
2.5.23 Touchscreen Connector (CN23)

4 Wires



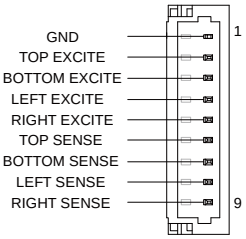
4 Wire			
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP	IN	
3	BOTTOM	IN	
4	LEFT	IN	
5	RIGHT	IN	
6	NC		
7	NC		
8	NC		
9	NC		

5 Wires



5 Wire			
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	UL(Y)	IN	
3	UR(H)	IN	
4	LL(L)	IN	
5	LR(X)	IN	
6	SENSE(S)	IN	
7	NC		
8	NC		
9	NC		

8 Wires

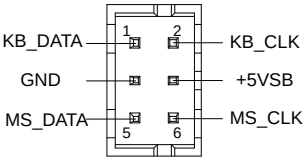


8 Wire			
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	

2	TOP EXCITE	IN
3	BOTTOM EXCITE	IN
4	LEFT EXCITE	IN
5	RIGHT EXCITE	IN
6	TOP SENSE	IN
7	BOTTOM SENSE	IN
8	LEFT SENSE	IN
9	RIGHT SENSE	IN

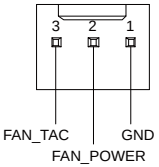
* Touch mode can be set by JP14

2.5.24 PS/2 Keyboard/Mouse Combo Port (CN24)



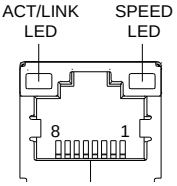
Pin	Pin Name	Signal Type	Signal Level
1	KB_ DATA	I/O	+5V
2	KB_CLK	I/O	+5V
3	GND	GND	
4	+5VSB	PWR	+5V
5	MS_DATA	I/O	+5V
6	MS_CLK	I/O	+5V

2.5.25 CPU Fan (CN25)



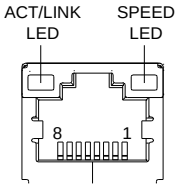
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	FAN_POWER	PWR	+12V
3	FAN_TAC	IN	

2.5.26 LAN (RJ-45) Port1 (CN26)



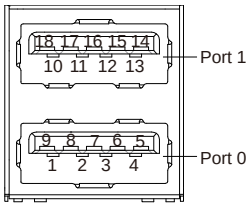
Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.5.27 LAN (RJ-45) Port2 (CN27)



Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

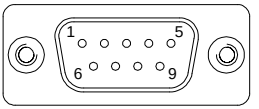
2.5.28 USB Ports 0 and 1 (CN28)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USB0_SSRX–	DIFF	

6	USB0_SSRX+	DIFF	
7	GND	GND	
8	USB0_SSTX–	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	
14	USB1_SSRX–		
15	USB1_SSRX+		
16	GND	GND	
17	USB1_SSTX–		
18	USB1_SSTX+		

2.5.29 COM Port 1 (D-SUB 9) (CN29)

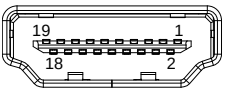


* COM port1 can be selected for D-SUB9 or Wafer BOX connector (CN22)

Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	RX	IN	
3	TX	OUT	±9V
4	DTR	OUT	±9V
5	GND	GND	
6	DSR	IN	
7	RTS	OUT	±9V

8	CTS	IN
9	RI	IN

2.5.30 HDMI Port (CN30)

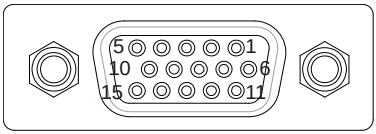


Pin	Pin Name	Signal Type	Signal Level
1	TMDS_DAT2+	DIFF	
2	GND	GND	
3	TMDS_DAT2-	DIFF	
4	TMDS_DAT1+	DIFF	
5	GND	GND	
6	TMDS_DAT1-	DIFF	
7	TMDS_DAT0+	DIFF	
8	GND	GND	
9	TMDS_DAT0-	DIFF	
10	TMDS_CLK+	DIFF	
11	GND	GND	
12	TMDS_CLK-	DIFF	
13	NC		
14	NC		
15	DDC_CLK	I/O	+5V
16	DDC_DATA	I/O	+5V
17	GND	GND	
18	+5V	I/O	+5V
19	HPLG_DETECT	IN	

2.5.31 Battery (CN31)

Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	3.3V
2	GND	GND	

2.5.32 VGA Port (CN32)



Pin	Pin Name	Signal Type	Signal Level
1	RED	OUT	
2	GREEN	OUT	
3	BLUE	OUT	
4	NC		
5	GND	GND	
6	RED_GND_RTN	GND	
7	GREEN_GND_RTN	GND	
8	BLUE_GND_RTN	GND	
9	+5V	PWR	+5V
10	CRT_PLUG#		
11	NC		
12	DDC_DATA	I/O	+5V
13	HSYNC	OUT	
14	VSYNC	OUT	
15	DDC_CLK	I/O	+5V

2.5.33 MiniCard Slot (Half-MiniCard) (CN33)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	NC	PWR	
9	GND	GND	
10	NC	I/O	
11	PCIE_REF_CLK-	DIFF	
12	NC	IN	
13	PCIE_REF_CLK+	DIFF	
14	NC		
15	GND	GND	
16	NC	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V

25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		

52	+3.3VSB	PWR	+3.3V

2.5.34 DDR3L SO-DIMM (CN34)

Standard Specification

2.5.35 UIM Card Socket (CN35)

Pin	Pin Name	Signal Type	Signal Level
1	UIM_PWR	PWR	
2	UIM_RST	IN	
3	UIM_CLK	IN	
4	GND	GND	
5	UIM_VPP	PWR	
6	UIM_DATA	I/O	

2.5.36 MiniCard Slot (Full-MiniCard) (CN36)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	UIM_PWR	PWR	
9	GND	GND	

10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	

37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The board uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

Chipset – For hosting bridge parameters

Boot – Enable/ Disable quiet Boot Option

Security – The setup administrator password can be set here

Save & Exit –Save your changes and exit the program

3.3 Setup submenu: Main

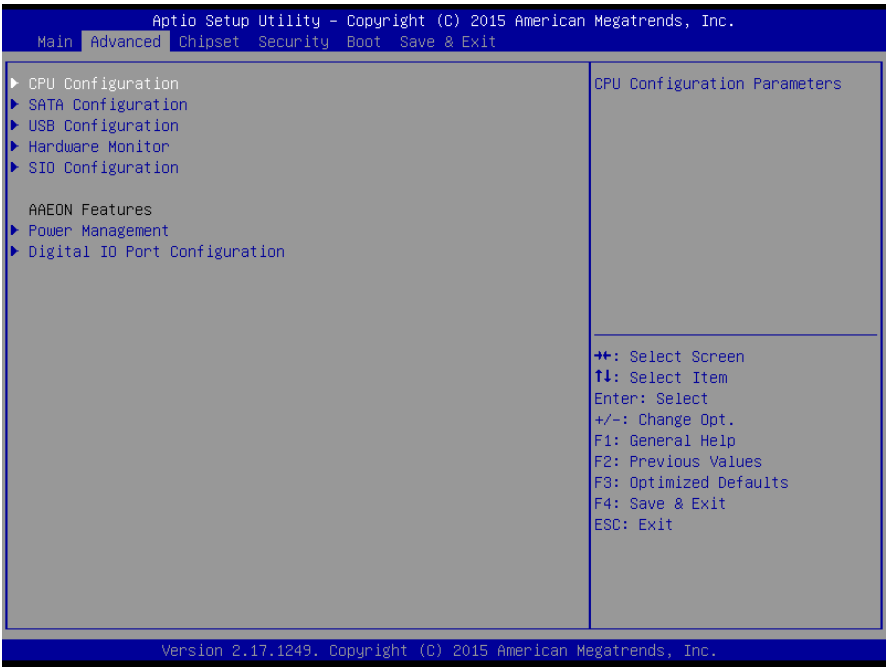
Press '*Delete*' Key to enter Setup

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Main  Advanced  Chipset  Security  Boot  Save & Exit

BIOS Information                          Set the Date. Use Tab to
    GENE-BSW5 Rx.y (GBW5AMxy) (MM/DD/YYYY)  switch between Date elements.

BIOS Vendor                American Megatrends
Compliancy                 UEFI 2.4; PI 1.3

System Date                [Day MM/DD/YYYY]
System Time                [hh:mm:ss]

Access Level               Administrator

                                          →←: Select Screen
                                          ↑↓: Select Item
                                          Enter: Select
                                          +/-: Change Opt.
                                          F1: General Help
                                          F2: Previous Values
                                          F3: Optimized Defaults
                                          F4: Save & Exit
                                          ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

System Date	Day MM:DD:YYYY	
Change the month, year and century. The 'Day' is changed automatically.		
System Time	HH : MM : SS	
Change the clock of the system.		

3.4 Setup submenu: Advanced



Options summary: (**default setting**)

CPU Configuration		
CPU Configuration Parameters		
SATA Configuration		
SATA Device Options Settings		
USB Configuration		
USB Configuration Parameters		
Hardware Monitor		
Monitor hardware status		
SIO Configuration		
Super IO Configuration Parameters		

Power Management		
System ACPI/Power Mode/Wake Event Configuration		
Digital IO Port Configuration		
DIO configuration		

3.4.1 Advanced: Power Management

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Main

Power Management                                  Select system power mode.

Power Mode                        [ATX Type]
Power Saving(ERP) Control         [Disabled]
Restore AC Power Loss             [Always Off]

Wake Events
RI Wake Event                     [Enabled]
RTC wake system from S5           [Disabled]

                                  →←: Select Screen
                                  ↑↓: Select Item
                                  Enter: Select
                                  +/-: Change Opt.
                                  F1: General Help
                                  F2: Previous Values
                                  F3: Optimized Defaults
                                  F4: Save & Exit
                                  ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

Power Mode	**ATX Type**	
	AT Type	
Select system power mode		
Power Saving (ERP) Control	Enabled	
	Disabled	
Enabled or disabled ERP feature for power saving in S5 state.		
Restore AC Power Loss	**Power Off**	
	Power on	
	Late State	
Select AC power state when power is re-applied after a power failure		

RI Wake Event	**Enabled**	
	Disabled	
Enabled or disabled wake on ring function.		
RTC wake system from S5	**Disabled**	
	Fixed Time	
	Dynamic Time	
Enable system to wake from S5 using RTC alarm.		
Wake up day	0-31	
Select 0 for daily system wake up 1-31 for which day of the month that you would like the system to wake up		
Wake up hour	0-23	
Wake up minute	0-59	
Wake up second	0-59	
Wake up minute increase	1-5	

3.4.2 Advanced: CPU Configuration

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Main

CPU Configuration                                   Enable/Disable Intel SpeedStep

Intel(R) Atom(TM) CPU Modelname
CPU Signature                    xxxxx
Microcode Patch                  xxx
Max CPU Speed                    xxxx MHz
Min CPU Speed                    xxx MHz
Processor Cores                  x
64-bit                           Supported
Intel HT Technology              Not Supported
Intel VT-x Technology            Supported

L1 Data Cache                    24 kB x 4
L1 Code Cache                    32 kB x 4                 →←: Select Screen
L2 Cache                         1024 kB x 2               ↑↓: Select Item
L3 Cache                         Not Present               Enter: Select
                                                           +/-: Change Opt.
EIST                             [Enabled]                 F1: General Help
Turbo Mode                       [Enabled]                 F2: Previous Values
Intel Virtualization Technology  [Enabled]                 F3: Optimized Defaults
                                                           F4: Save & Exit
                                                           ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

EIST	**Enabled**	
	Disabled	
Enable/Disable Intel SpeedStep feature.		
Turbo Mode	**Enabled**	
	Disabled	
En/Disable Turbo mode.		
Intel Virtualization Technology	**Enabled**	
	Disabled	
When enabled, a VMM can utilize the additional hardware capabilities provide by Vanderpool Technology		

3.4.3 Advanced: SATA Configuration

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Main

SATA Configuration                                  Select SATA Interface Speed,
                                                    CHV A1 always with Gen1 Speed.
SATA Mode Selection              [AHCI]
SATA Interface Speed             [Gen3]

SATA Port0
Drive Modelname
Hot Plug                         [Disabled]

mSATA Port
Drive Modelname

                                                    →←: Select Screen
                                                    ↑↓: Select Item
                                                    Enter: Select
                                                    +/-: Change Opt.
                                                    F1: General Help
                                                    F2: Previous Values
                                                    F3: Optimized Defaults
                                                    F4: Save & Exit
                                                    ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

SATA Speed Support	**Gen3**	
	Gen2	
	Gen1	
SATA Speed Support Gen3, Gen2 or Gen1		
SATA Mode	**AHCI Mode**	
Only AHCI mode support on this platform		
SATA Port0/Port1 HotPlug	**Enabled**	
	Disabled	
Enabled/Disabled SATA Port0/Port1 HotPlug function		

3.4.4 Advanced: USB Configuration

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Main

USB Configuration                                  Mode of operation of xHCI
                                                   controller
USB Devices:
      Device list

XHCI Mode                          [Enabled]
Legacy USB Support                 [Enabled]

                                                   →←: Select Screen
                                                   ↑↓: Select Item
                                                   Enter: Select
                                                   +/-: Change Opt.
                                                   F1: General Help
                                                   F2: Previous Values
                                                   F3: Optimized Defaults
                                                   F4: Save & Exit
                                                   ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

XHCI Mode	**Enabled**	
	Disabled	
Enable/Disable for xHCI controller:		
USB 2.0(EHCI) Support	Enabled	
	Disabled	
Control the USB EHCI (USB 2.0) functions. This item active when xHCI controller disabled because all ports are routed to xHCI controller when xHCI enabled.		
Legacy USB Support	**Enabled**	
	Disabled	

	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI application		

3.4.5 Advanced: SIO Configuration

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Advanced

AMI SIO Driver Version :   A5.05.03

Super IO Chip Logical Device(s) Configuration
▶ [*Active*]  Serial Port  1
▶ [*Active*]  Serial Port  2
▶ [*Active*]  Serial Port  3
▶ [*Active*]  Serial Port  4
▶ [*Active*]  Serial Port  5
▶ [*Active*]  Serial Port  6
▶ [Disabled]  Parallel Port

WARNING: Logical Devices state on the left side of the

View and Set Basic properties
of the SIO Logical device.
Like IO Base, IRQ Range, DMA
Channel and Device Mode.

→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

Parallel Port/Serial Port 1/2/3/4/5/6 Configuration		
Set Parameters of Serial Port 1/2/3/4/5/6 and Parallel Port		

3.4.5.1 SIO Configuration: Serial Port 1-6 Configuration

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Advanced

Serial Port  x Configuration                    Enable or Disable this Logical
                                                Devcie.
Use This Device                    [Enabled]

Logical Device Settings:
Current :     IO=xxxh; IRQ=x;

Possible:                          [Auto]
Mode    :                          [RS232]

WARNING: disabling SIO Logical Devices may have unwanted
side effects.
PROCEED WITH CAUTION.                           →←: Select Screen
                                                ↑↓: Select Item
                                                Enter: Select
                                                +/-: Change Opt.
                                                F1: General Help
                                                F2: Previous Values
                                                F3: Optimized Defaults
                                                F4: Save & Exit
                                                ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

Mode	**RS232**	
	RS422	
	RS485 Driver Half Duplex	
	RS485 Receiver Half Duplex	
Configure COM operated as RS232, RS422 or RS485. Only COM2 and COM3 support this function.		

3.4.5.2 SIO Configuration: Parallel Port Configuration

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Advanced

Parallel Port  Configuration                    Enable or Disable this Logical
                                                Device.
Use This Device                    [Disabled]

WARNING: Disabling SIO Logical Devices may have unwanted
side effects.
PROCEED WITH CAUTION.

                                                →←: Select Screen
                                                ↑↓: Select Item
                                                Enter: Select
                                                +/-: Change Opt.
                                                F1: General Help
                                                F2: Previous Values
                                                F3: Optimized Defaults
                                                F4: Save & Exit
                                                ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

Use This Device		**Disabled**	
		Enabled	
En/Disable specified this Logical Device Note: LPT and DIO feature share the same interface on the board. When LPT disabled, the interface works in DIO mode and vice versa.			
Possible		**Use Automatic Settings**	
	STD Printer	IO=378h; IRQ=5;	
	SPP	IO=378h; IRQ=5,6,7,9,10,11,12;	
	EPP and SPP	IO=278h; IRQ=5,6,7,9,10,11,12;	
		IO=3BCh; IRQ=5,6,7,9,10,11,12;	

	ECP	IO=378h; IO=778h; IRQ=5; DMA=3;	
	ECP and EPP	IO=378h; IO=778h; IRQ=5,6,7,9,10,11,12; DMA=1,3;	
		IO=278h; IO=678h; IRQ=5,6,7,9,10,11,12; DMA=1,3;	
		IO=3BCh; IO=7BCh; IRQ=5,6,7,9,10,11,12; DMA=1,3;	
Select a resource setting for Super IO device.			
Mode		**STD Print Mode**	
		SPP Mode	
		EPP-1.9 and SPP Mode	
		EPP-1.7 and SPP Mode	
		ECP Mode	
		ECP and EPP 1.9 Mode	
		ECP and EPP 1.7 Mode	
Change Parallel Port mode.			

3.4.6 Advanced: Hardware Monitor

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Main

CPU Temperature                    :     %                  Enable or Disable Smart Fan
CPU(external) Temperature          :     %
System Temperature                 :     %
CPU Fan Speed                      :
VCORE                              :        V
VMEM                               :        V
+12V                               :        V
+5V                                :        V
+5VSB                              :        V
+3.3V                              :        V
VBAT                               :        V

Smart Fan                          [Enabled]            →←: Select Screen
▶ Smart Fan Configuration                                ↑↓: Select Item
                                                         Enter: Select
                                                         +/-: Change Opt.
                                                         F1: General Help
                                                         F2: Previous Values
                                                         F3: Optimized Defaults
                                                         F4: Save & Exit
                                                         ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

Smart Fan	Disabled	
	Enabled	
En/Disable specified Smart Fan.		

3.4.6.1 Hardware Monitor: Smart Fan Configuration

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Main

Smart Fan Mode Configuration                    Smart Fan  Mode Select

Fan Mode                          [Auto Duty]
Temperature Source                [CPU(external)]
Duty Cycle 1                      85
Temperature 1                     60
Duty Cycle 2                      70
Temperature 2                     50
Duty Cycle 3                      60
Temperature 3                     40
Duty Cycle 4                      50
Temperature 4                     30
Duty Cycle 5                      40

                                  →←: Select Screen
                                  ↑↓: Select Item
                                  Enter: Select
                                  +/-: Change Opt.
                                  F1: General Help
                                  F2: Previous Values
                                  F3: Optimized Defaults
                                  F4: Save & Exit
                                  ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

Fan Mode	Manual Duty	
	Auto Duty	
Smart Fan Mode Select		
Manual Duty Mode	**60**	
Manual mode fan control, user can write expected duty cycle (PWM fan type) 1 – 100		
Temperature Source	**CPU(external)**	
Select the monitored temperature source for this fan. Only supports CPU(external) support for this board.		
Duty Cycle 1	**85**	
Duty Cycle 2	**70**	

Duty Cycle 3	60	
Duty Cycle 4	50	
Duty Cycle 5	40	
Fan speed control for each temperature region. User can write expected duty cycle (PWM fan type) 1 – 100		
Temperature 1	60	
Temperature 2	50	
Temperature 3	40	
Temperature 4	30	
Definition of temperature region. User can write expected temperature boundary 1 – 100		

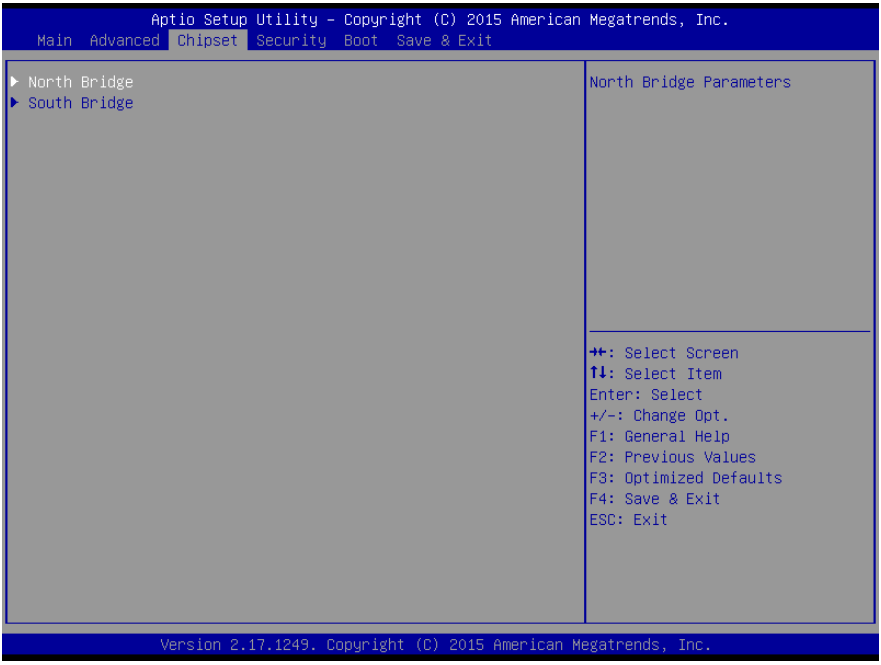
3.4.7 Advanced: Digital IO Port Configuration

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Advanced

Digital IO Port Configuration                    Set DIO as Input or Output

DIO Port1                          [Output]
  Output Level                     [High  ]
DIO Port2                          [Output]
  Output Level                     [High  ]
DIO Port3                          [Output]
  Output Level                     [High  ]
DIO Port4                          [Output]
  Output Level                     [High  ]
DIO Port5                          [Input ]
DIO Port6                          [Input ]
DIO Port7                          [Input ]
DIO Port8                          [Input ]

                                   →←: Select Screen
                                   ↑↓: Select Item
                                   Enter: Select
                                   +/-: Change Opt.
                                   F1: General Help
                                   F2: Previous Values
                                   F3: Optimized Defaults
                                   F4: Save & Exit
                                   ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

DIO Port1/2/3/4	Input	
	Output	
Set DIO Port1/2/3/4 as Input or Output		
DIO Port5/6/7/8	**Input**	
	Output	
Set GPIO3/GPIO4 as Input or Output		
Output Level	Hi	
	Low	
Set GPIO Level when used as Output		

3.5 Setup submenu: Chipset



Options summary: (**default setting**)

North Bridge Configuration		
North Bridge Parameters.		
South Bridge		
South Bridge Parameters		

3.5.1 Chipset: North Bridge Configuration

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Chipset

North Bridge                                   Select the Video Device which
                                               will be activated during POST.
Memory Information                             This has no effect if external
Total Memory                    xxxx MB        graphics present.
Primary IGFX Boot Display       [Auto]         Secondary boot display
                                               selection will appear based on
DVMT Pre-Allocated              [32M]          your selection.
DVMT Total Gfx Mem              [256MB]        VGA modes will be supported
                                               only on primary display
▶ LVDS Panel Configuration

                                               →←: Select Screen
                                               ↑↓: Select Item
                                               Enter: Select
                                               +/-: Change Opt.
                                               F1: General Help
                                               F2: Previous Values
                                               F3: Optimized Defaults
                                               F4: Save & Exit
                                               ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

Primary Boot Display	**Auto**	
	CRT	
	LVDS1	
	LVDS2/HDMI	
Select Primary boot display device		
Secondary Boot Display	**Disabled**	
	CRT	
	LVDS1	
	LVDS2/HDMI	
Select Primary boot display device		

DVMT Pre-Allocated	**32MB**	
	32MB~512MB	
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.		
DVMT Total Gfx Mem	128MB	
	256MB	
	Max	
Select DVMT 5.0 Total Graphic Memory size used by the IGD.		
LVDS Panel Configuration		
Config LVDS panel parameters.		

3.5.1.1 North Bridge: LVDS Panel Configuration

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Main

LVDS Panel Configuration                    Enable/Disabled this panel

LVDS                          [Enabled]
  Panel Type                  [1024x768@60Hz]
  Color Depth                 [18-Bit]
  Backlight Type              [Normal]
  Backlight Level             [ 80%]

LVDS2                         [Enabled]
  Panel Type                  [1024x768@60Hz]
  Color Depth                 [18-Bit]
  Backlight Type              [Normal]
  Backlight Level             [ 80%]

                                          →←: Select Screen
                                          ↑↓: Select Item
                                          Enter: Select
                                          +/-: Change Opt.
                                          F1: General Help
                                          F2: Previous Values
                                          F3: Optimized Defaults
                                          F4: Save & Exit
                                          ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

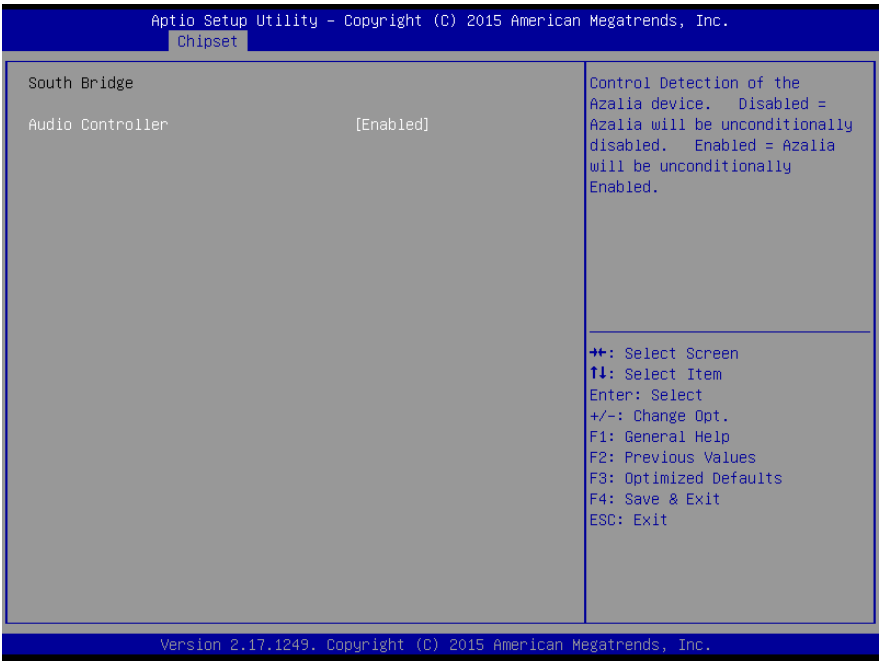
Options summary: (**default setting**)

LVDS	Disabled	
	Enabled	
LVDS2	Disabled	
	Enabled	
Enable or Disable LVDS interface		
Panel Type	640x480	
	800x480	
	800x600	
	1024x600	
	1024x768	

	1280x768	
	1280x1024	
	1366x768	
	1440x900	
	1600x1200	
	1920x1080	
	1920x1200	
Select panel resolution.		
Color Depth	**18-Bit**	
	24-Bit	
	36-Bit	
	48-Bit	
Select color depth of the panel		
Backlight Type	Inverted	
	Normal	
Select Backlight control type. Inverted: Brightest for low PWM duty cycle and low voltage. Normal: Brightest for high PWM duty cycle and high voltage.		
Backlight Level	100%	
	90%	
	80%	
	70%	
	60%	
	50%	
	40%	
	30%	
	20%	

	10%	
	0%	
Select Backlight Level		

3.5.2 Chipset: South Bridge



Options summary: (**default setting**)

Audio Controller	Disabled	
	Enabled	
Enable or disabled Azalia device for audio function.		

3.6 Setup submenu: Security

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
 Main  Advanced  Chipset  Security  Boot  Save & Exit

 Password Description                          Set Administrator Password

 If ONLY the Administrator's password is set,
 then this only limits access to Setup and is
 only asked for when entering Setup.
 If ONLY the User's password is set, then this
 is a power on password and must be entered to
 boot or enter Setup. In Setup the User will
 have Administrator rights.
 The password length must be
 in the following range:
 Minimum length                    3
 Maximum length                    20

                                                 →←: Select Screen
 Administrator Password                          ↑↓: Select Item
 User Password                                   Enter: Select
                                                 +/-: Change Opt.
                                                 F1: General Help
                                                 F2: Previous Values
                                                 F3: Optimized Defaults
                                                 F4: Save & Exit
                                                 ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (*default setting*)

Administrator Password/	*Not set*	
User Password		

Change User/Administrator Password

If an Administrator Password is set, it will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

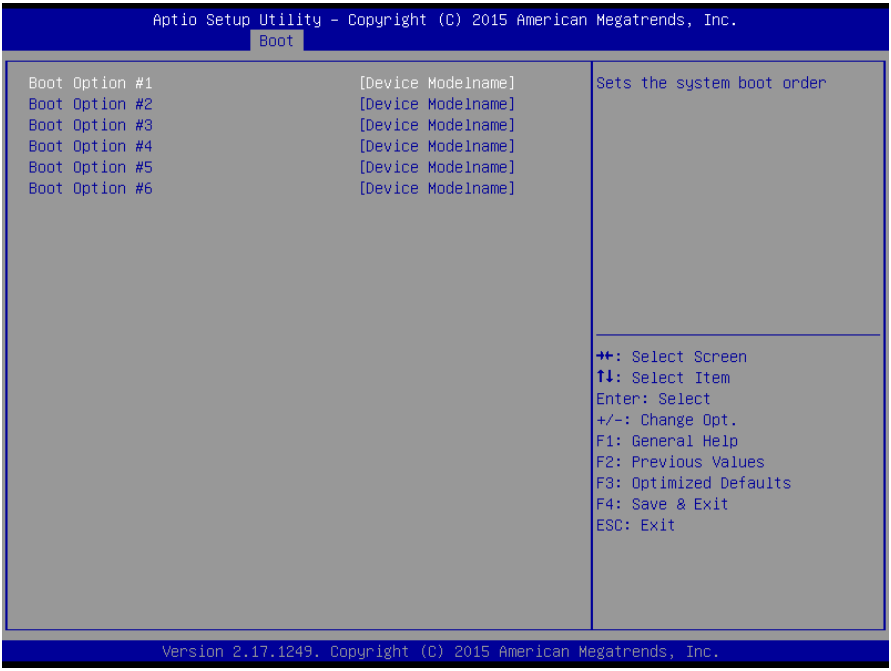
3.7 Setup submenu: Boot

```
Aptio Setup Utility – Copyright (C) 2015 American Megatrends, Inc.
Main  Advanced  Chipset  Security  Boot  Save & Exit

Boot Configuration                                   Enables or disables Quiet Boot
                                                     option
Quiet Boot                          [Enabled]
Launch PXE ROM                      [Disabled]

Boot Option Priorities
Boot Option #1                      [Device Modelname]
Boot Option #2                      [Device Modelname]
Boot Option #3                      [Device Modelname]
Boot Option #4                      [Device Modelname]
Boot Option #5                      [Device Modelname]

CD/DVD ROM Drive BBS Priorities
Hard Drive BBS Priorities                            →←: Select Screen
Floppy Drive BBS Priorities                          ↑↓: Select Item
Network Device BBS Priorities                        Enter: Select
                                                     +/-: Change Opt.
                                                     F1: General Help
                                                     F2: Previous Values
                                                     F3: Optimized Defaults
                                                     F4: Save & Exit
                                                     ESC: Exit

Version 2.17.1249. Copyright (C) 2015 American Megatrends, Inc.
```

Options summary: (**default setting**)

Quiet Boot	Disabled	
	Enabled	
En/Disable showing boot logo.		
Launch PXE OpROM	**Disabled**	
	Enabled	
En/Disable network OpROM for legacy PXE boot		
Boot Option #X/ XXXX Drive BBS Priorities		
The order of boot priorities.		

3.7.1 Boot: BBS Priorities



Options summary: (**default setting**)

Boot Option #x	Disabled	
	Device name	
Sets the system boot order		

3.8 Setup submenu: Save & Exit

Options summary: (**default setting**)

Save Changes and Reset		
Reset the system after saving the changes		
Discard Changes and Exit		
Reset system setup without saving any changes		
Restore Defaults		
Restore/Load Default values for all the setup options.		

Chapter 4

Drivers Installation

4.1 Product CD/DVD

The GENE-BSW5 comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Drivers

1. Open the **Step1 - Chipset** folder and select your OS
2. Open the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install Graphics Drivers

1. Open the **Step2 - VGA** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Note: After the drivers are installed, LVDS1, not VGA, will be automatically set as the default video output. Users may change this by disabling LVDS1/LVDS2 in BIOS (if they are not used) to make VGA as the default output. Desktop display modes can be changed using the hotkey "Windows key + P".

Note 2: There is a known issue in Windows® 8.1 whereby running Direct3D graphic tools such as BurnIn Test will cause the system to freeze. Microsoft has provided the KB2979265 hotfix (included in the disk) to address this issue. In order to apply this hotfix without dependency issues, it is advised that users install it via Windows® Update.

Step 3 – Install Audio Drivers

1. Click on the **Step3 - Audio** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install LAN Drivers

1. Open the **Step4 - LAN** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install Touch Panel Driver

1. Open the **Step5 - TOUCHPANEL** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 6 – Install TXE Driver

1. Open the **Step6 - TXE** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 7 – Install USB 3.0 Driver (Windows 7/8.1 only)

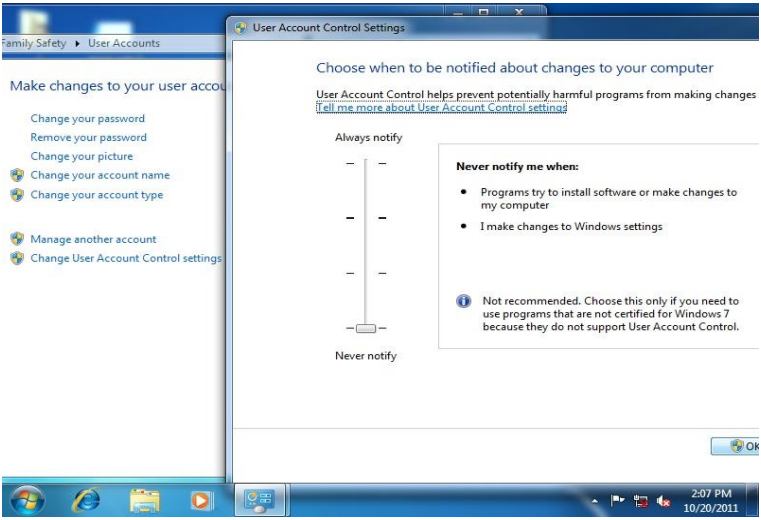
1. Open the **Step7 - USB3.0** folder and select your OS
2. Open the**.exe** file in the folder
3. Follow the instructions

4. Drivers will be installed automatically

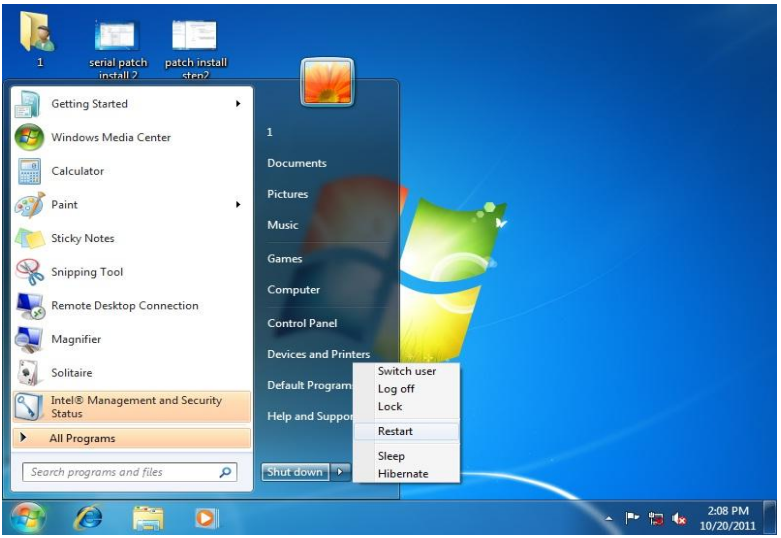
Step 8 – Install Serial Port Drivers

For Windows 7:

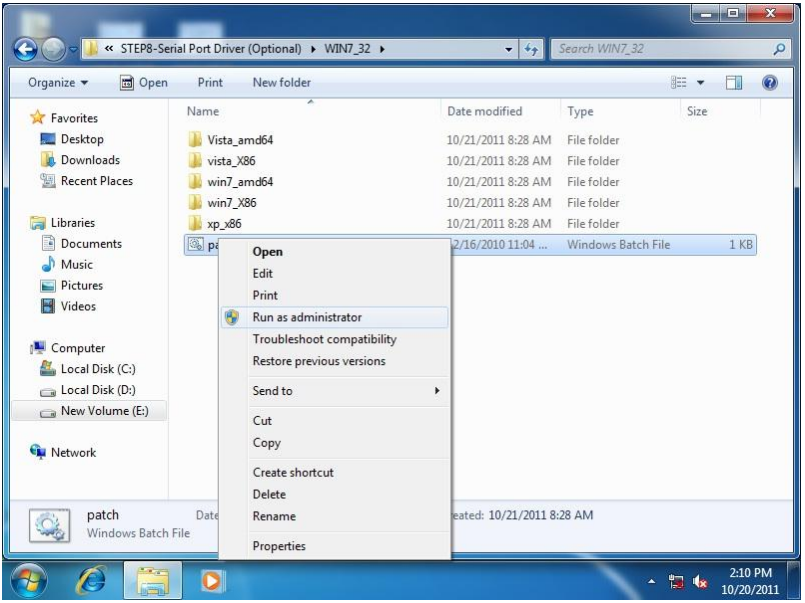
1. Change User Account Control settings to **Never notify**



2. Reboot and log in as administrator

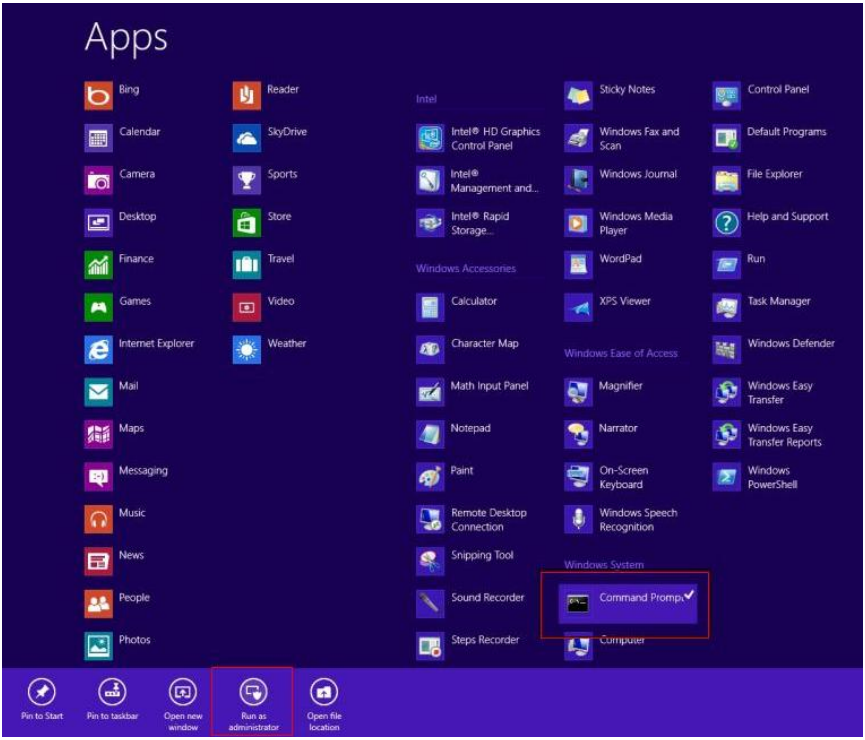


3. Run patch.bat as administrator



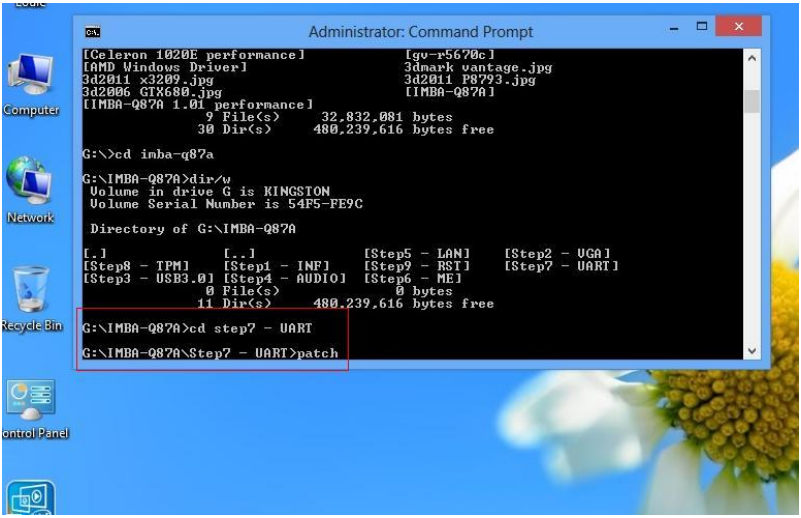
For Windows 8:

1. Open the Apps Screen, right click on the **Command Prompt** tile and select **Run as Administrator**



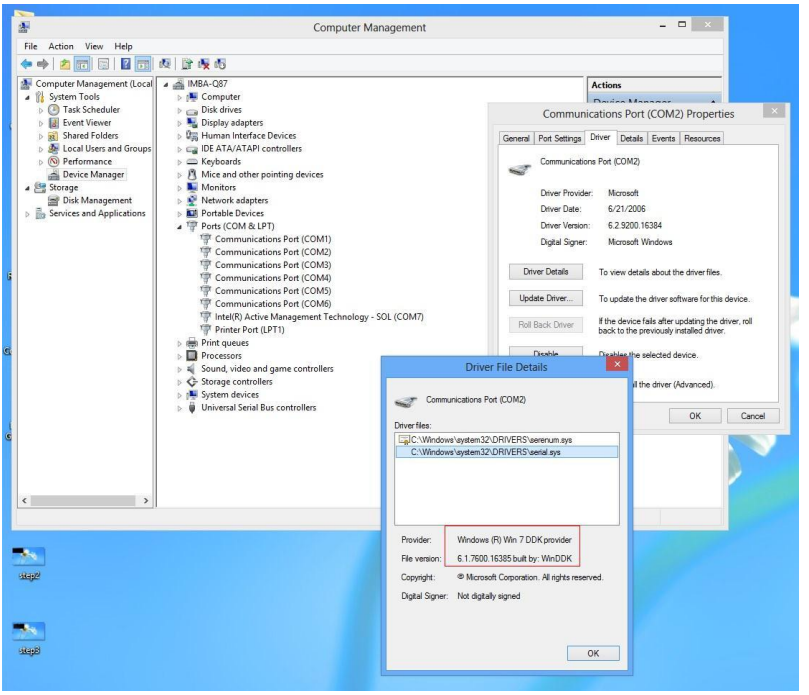
2. To install the driver (patch.bat), you will first have to locate the file in command prompt. To do that, go to the folder in which the file resides by entering **cd (file path)** eg: if the file is in a folder named abc in c drive, enter cd c:\abc (screenshot for reference only)

3. You are now at the folder where the file is located. Enter the **patch.bat** to open and install the drivers.



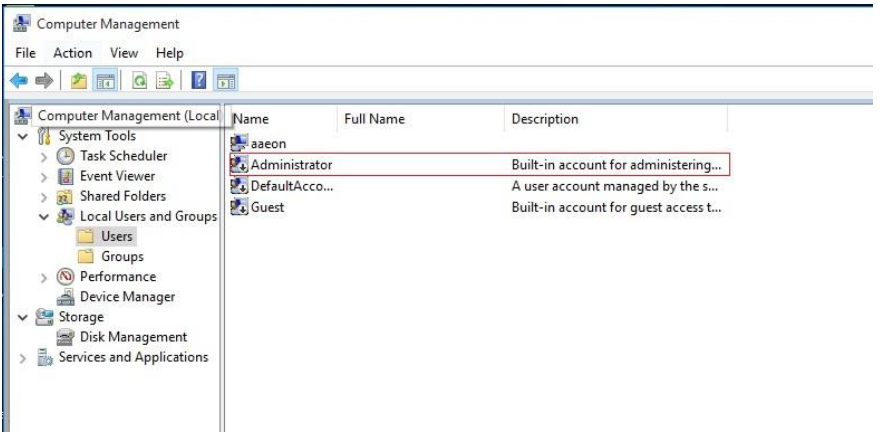
4. Reboot after installation completes.

5. To confirm the installation, go to Device Manager, expand the Ports (COM & LPT) tree and double click on any of the COM ports to open its properties. Go to the Driver tab, select Driver Details and click on serial.sys, you should see its provider as Windows (R) Win 7 DDK Provider.

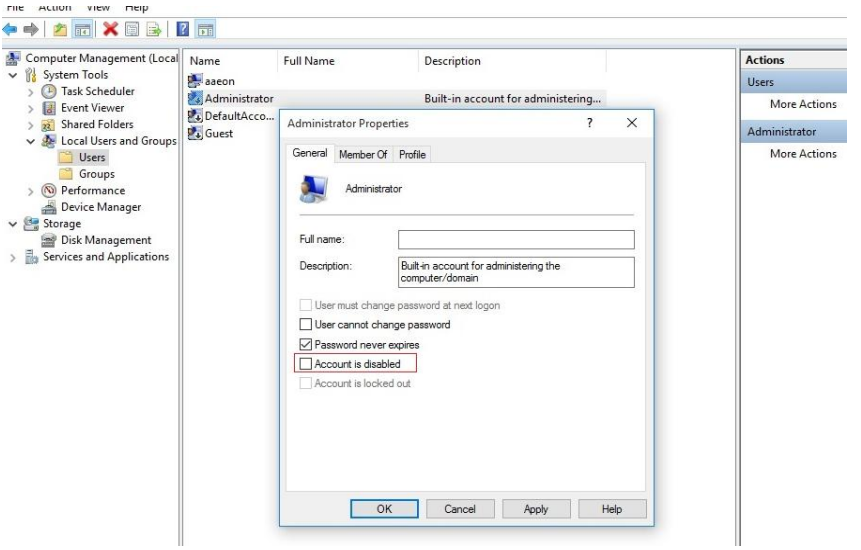

Computer Management
File Action View Help
Computer Management (Local
System Tools
Task Scheduler
Event Viewer
Shared Folders
Local Users and Groups
Performance
Device Manager
Storage
Disk Management
Services and Applications
IMBA-Q87
Computer
Disk drives
Display adapters
Human Interface Devices
IDE ATA/ATAPI controllers
Keyboards
Mice and other pointing devices
Monitors
Network adapters
Portable Devices
Ports (COM & LPT)
Communications Port (COM1)
Communications Port (COM2)
Communications Port (COM3)
Communications Port (COM4)
Communications Port (COM5)
Communications Port (COM6)
Intel(R) Active Management Technology - SOL (COM7)
Printer Port (LPT1)
Print queues
Processors
Sound, video and game controllers
Storage controllers
System devices
Universal Serial Bus controllers
Actions
Communications Port (COM2) Properties
General Port Settings Driver Details Events Resources
Communications Port (COM2)
Driver Provider: Microsoft
Driver Date: 6/21/2006
Driver Version: 6.2.9200.16384
Digital Signer: Microsoft Windows
Driver Details
To view details about the driver files.
Update Driver...
To update the driver software for this device.
Roll Back Driver
If the device fails after updating the driver, roll back to the previously installed driver.
OK
Cancel
Driver File Details
Communications Port (COM2)
Driver files:
C:\Windows\system32\DRIVERS\serenum.sys
C:\Windows\system32\DRIVERS\serial.sys
Provider: Windows (R) Win 7 DDK provider
File version: 6.1.7600.16385 built by: WinDDK
Copyright: © Microsoft Corporation. All rights reserved.
Digital Signer: Not digitally signed
OK

For Windows 10:

1. You will need administrator rights to install the drivers. To get it, first go to **Computer Management** in **Control Panel** and double-click on **Administrator**

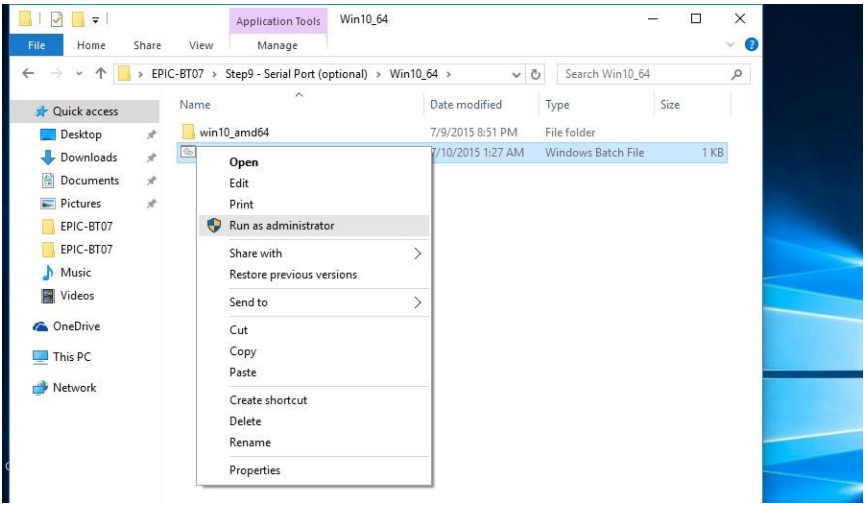


2. In the dialog box, **uncheck** the **Account is disabled** option to enable administrator account.



3. Restart and sign in as the administrator (not password-protected by default)

4. Go back to the Windows 10 Serial Port drivers directory and **run patch.bat as administrator.**



Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address		
	Default Value	Note
I/O Base Address	0xA10	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7, register 0x60-0x61.

Table 2 : Watchdog relative register table				
Register	Offset	BitNum	Value	Note
Watchdog WDTRST# Enable	0x00	7	1	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s *Pulse width is must longer then 16ms.*
Signal Polarity	0x05	2	0	0: low active 1: high active *Must set this bit to 0*
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse *Must set this bit to 1*
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

A.2 Watchdog Sample Program

```
*****************************************************************************
// WDT I/O operation relative definition (Please reference to Table 1)
#define   WDTAddr        0x510   // WDT I/O base address
Void   WDTWriteByte(byte Register, byte Value);
byte   WDTReadByte(byte Register);
Void   WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define   DevReg          0x00   // Device configuration register
      #define   WDTRstBit   0x80   // Watchdog WDTRST# (Bit7)
      #define   WDTRstVal   0x80   // Enabled WDTRST#
#define   TimerReg       0x05   // Timer register
      #define   PSWidthBit     0x00     // WDTRST# Pulse width (Bit0:1)
      #define   PSWidthVal     0x01     // 25ms for WDTRST# pulse
      #define   PolarityBit   0x02     // WDTRST# Signal polarity (Bit2)
      #define   PolarityVal   0x00     // Low active for WDTRST#
      #define   UnitBit          0x03     // Unit for timer (Bit3)
      #define   ModeBit          0x04     // WDTRST# mode (Bit4)
      #define   ModeVal          0x01     // 0:level 1: pulse
      #define   EnableBit       0x05     // WDT timer enable (Bit5)
      #define   EnableVal       0x01     // 1: enable
      #define   StatusBit       0x06     // WDT timer status (Bit6)
#define   CounterReg   0x06   // Timer counter register
*****************************************************************************

*****************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig(Counter, Unit);

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*****************************************************************************

*****************************************************************************
// Procedure : AaeonWDTEnable
```

```
VOID    AaeonWDTEnable (){
        WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (byte Counter, BOOLEAN Unit){
        // Disable WDT counting
        WDTEnableDisable(0);
        // Clear Watchdog Timeout Status
        WDTClearTimeoutStatus();
        // WDT relative parameter setting
        WDTParameterSetting(Timer, Unit);
}

VOID    WDTEnableDisable(byte Value){
        If (Value == 1)
            WDTSetBit(TimerReg, EnableBit, 1);
        else
            WDTSetBit(TimerReg, EnableBit, 0);
}

VOID    WDTParameterSetting(byte Counter, BOOLEAN Unit){
        // Watchdog Timer counter setting
        WDTWriteByte(CounterReg, Counter);
        // WDT counting unit setting
        WDTSetBit(TimerReg, UnitBit, Unit);
        // WDT output mode set to pulse
        WDTSetBit(TimerReg, ModeBit, ModeVal);
        // WDT output mode set to active low
        WDTSetBit(TimerReg, PolarityBit, PolarityVal);
        // WDT output pulse width is 25ms
        WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
        // Watchdog WDTRST# Enable
        WDTSetBit(DevReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
        WDTSetBit(TimerReg, StatusBit, 1);
}
*****************************************************************************

*****************************************************************************
```

```
VOID   WDTWriteByte(byte Register, byte Value){
        IOWriteByte(WDTAddr+Register, Value);
}

byte   WDTReadByte(byte Register){
        return IOReadByte(WDTAddr+Register);
}

VOID   WDTSetBit(byte Register, byte Bit, byte Val){
        byte TmpValue;

        TmpValue = WDTReadByte(Register);
        TmpValue &= ~(1 << Bit);
        TmpValue |= Val << Bit;
        WDTWriteByte(Register, TmpValue);
}

*******************************************************************************
```

Appendix B

I/O Information

B.1 I/O Address Map

Input/output (IO)

```
[0000000000000000 - 000000000000006F] PCI Express Root Complex
[0000000000000020 - 0000000000000021] Programmable interrupt controller
[0000000000000024 - 0000000000000025] Programmable interrupt controller
[0000000000000028 - 0000000000000029] Programmable interrupt controller
[000000000000002C - 000000000000002D] Programmable interrupt controller
[000000000000002E - 000000000000002F] Motherboard resources
[0000000000000030 - 0000000000000031] Programmable interrupt controller
[0000000000000034 - 0000000000000035] Programmable interrupt controller
[0000000000000038 - 0000000000000039] Programmable interrupt controller
[000000000000003C - 000000000000003D] Programmable interrupt controller
[0000000000000040 - 0000000000000043] System timer
[000000000000004E - 000000000000004F] Motherboard resources
[0000000000000050 - 0000000000000053] System timer
[0000000000000061 - 0000000000000061] Motherboard resources
[0000000000000063 - 0000000000000063] Motherboard resources
[0000000000000065 - 0000000000000065] Motherboard resources
[0000000000000067 - 0000000000000067] Motherboard resources
[0000000000000070 - 0000000000000070] Motherboard resources
[0000000000000070 - 0000000000000077] System CMOS/real time clock
[0000000000000078 - 0000000000000CF7] PCI Express Root Complex
[0000000000000080 - 000000000000008F] Motherboard resources
[0000000000000092 - 0000000000000092] Motherboard resources
[00000000000000A0 - 00000000000000A1] Programmable interrupt controller
[00000000000000A4 - 00000000000000A5] Programmable interrupt controller
[00000000000000A8 - 00000000000000A9] Programmable interrupt controller
[00000000000000AC - 00000000000000AD] Programmable interrupt controller
[00000000000000B0 - 00000000000000B1] Programmable interrupt controller
[00000000000000B2 - 00000000000000B3] Motherboard resources
[00000000000000B4 - 00000000000000B5] Programmable interrupt controller
[00000000000000B8 - 00000000000000B9] Programmable interrupt controller
[00000000000000BC - 00000000000000BD] Programmable interrupt controller
[00000000000002C0 - 00000000000002C7] Communications Port (COM6)
[00000000000002D0 - 00000000000002D7] Communications Port (COM5)
[00000000000002E8 - 00000000000002EF] Communications Port (COM4)
[00000000000002F8 - 00000000000002FF] Communications Port (COM2)
[00000000000003B0 - 00000000000003BB] Intel(R) HD Graphics
[00000000000003C0 - 00000000000003DF] Intel(R) HD Graphics
[00000000000003E8 - 00000000000003EF] Communications Port (COM3)
[00000000000003F8 - 00000000000003FF] Communications Port (COM1)
[0000000000000400 - 000000000000047F] Motherboard resources
[00000000000004D0 - 00000000000004D1] Programmable interrupt controller
[0000000000000500 - 00000000000005FE] Motherboard resources
[0000000000000680 - 000000000000069F] Motherboard resources
[0000000000000A00 - 0000000000000A0F] Motherboard resources
[0000000000000A00 - 0000000000000A3F] Motherboard resources
[0000000000000A10 - 0000000000000A1F] Motherboard resources
[0000000000000A20 - 0000000000000A2F] Motherboard resources
[0000000000000D00 - 000000000000FFFF] PCI Express Root Complex
[000000000000D000 - 000000000000D0FF] Realtek PCIe GBE Family Controller
[000000000000D000 - 000000000000DFFF] PCI Express standard Root Port
[000000000000E000 - 000000000000E0FF] Realtek PCIe GBE Family Controller #2
[000000000000E000 - 000000000000EFFF] PCI Express standard Root Port
[000000000000F000 - 000000000000F03F] Intel(R) HD Graphics
[000000000000F040 - 000000000000F05F] Intel(R) Celeron(R)/Pentium(R) SM Bus Controller - 2292
[000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller
[000000000000E070 - 000000000000E077] Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor AHCI
[000000000000E080 - 000000000000E087] Intel(R) HD Graphics
```

B.2 Memory Address Map

Memory
- [00000000000A0000 - 00000000000BFFFF] Intel(R) HD Graphics
- [00000000000A0000 - 00000000000BFFFF] PCI Express Root Complex
- [00000000000C0000 - 00000000000DFFFF] PCI Express Root Complex
- [00000000000E0000 - 00000000000FFFFF] PCI Express Root Complex
- [0000000080000000 - 0000000080FFFFFF] Intel(R) HD Graphics
- [0000000080000000 - 00000000DFFFFFFF] PCI Express Root Complex
- [0000000081000000 - 00000000810FFFFF] Intel(R) Trusted Execution Engine Interface
- [0000000081100000 - 00000000811FFFFF] Intel(R) Trusted Execution Engine Interface
- [0000000081200000 - 000000008120FFFF] Intel(R) USB 3.0 eXtensible Host Controller - 0100 (Microsoft)
- [0000000081210000 - 0000000081213FFF] High Definition Audio Controller
- [0000000081214000 - 00000000812140 1F] Intel(R) Celeron(R)/Pentium(R) SM Bus Controller - 2292
- [0000000081215000 - 000000008121 57FF] Standard SATA AHCI Controller
- [0000000090000000 - 000000009FFFFFFF] Intel(R) HD Graphics
- [00000000A0000000 - 00000000A0003FFF] Realtek PCIe GBE Family Controller
- [00000000A0000000 - 00000000A00FFFFF] PCI Express standard Root Port
- [00000000A0004000 - 00000000A0004FFF] Realtek PCIe GBE Family Controller
- [00000000A0100000 - 00000000A0103FFF] Realtek PCIe GBE Family Controller #2
- [00000000A0100000 - 00000000A01FFFFF] PCI Express standard Root Port
- [00000000A0104000 - 00000000A0104FFF] Realtek PCIe GBE Family Controller #2
- [00000000E0000000 - 00000000EFFFFFFF] Motherboard resources
- [00000000FEA00000 - 00000000FEAFFFFF] Motherboard resources
- [00000000FED01000 - 00000000FED01FFF] Motherboard resources
- [00000000FED03000 - 00000000FED03FFF] Motherboard resources
- [00000000FED06000 - 00000000FED06FFF] Motherboard resources
- [00000000FED08000 - 00000000FED09FFF] Motherboard resources
- [00000000FED1C000 - 00000000FED1CFFF] Motherboard resources
- [00000000FED80000 - 00000000FEDBFFFF] Motherboard resources
- [00000000FEE00000 - 00000000FEEFFFFF] Motherboard resources
- [00000000FF000000 - 00000000FFFFFFFF] Intel(R) 82802 Firmware Hub Device

B.3 IRQ Mapping Chart

Interrupt request (IRQ)

(ISA) 0x00000000 (00)	System timer
(ISA) 0x00000001 (01)	Standard PS/2 Keyboard
(ISA) 0x00000003 (03)	Communications Port (COM2)
(ISA) 0x00000004 (04)	Communications Port (COM1)
(ISA) 0x0000000B (11)	Communications Port (COM3)
(ISA) 0x0000000B (11)	Communications Port (COM4)
(ISA) 0x0000000B (11)	Communications Port (COM5)
(ISA) 0x0000000B (11)	Communications Port (COM6)
(ISA) 0x0000000C (12)	PS/2 Compatible Mouse
(PCI) 0x00000007 (07)	Intel(R) Celeron(R)/Pentium(R) SM Bus Controller - 2292
(PCI) 0x00000013 (19)	Standard SATA AHCI Controller
(PCI) 0x00000016 (22)	High Definition Audio Controller
(PCI) 0xFFFFFFF8 (-8)	Intel(R) Trusted Execution Engine Interface
(PCI) 0xFFFFFFF9 (-7)	Realtek PCIe GBE Family Controller
(PCI) 0xFFFFFFFA (-6)	Realtek PCIe GBE Family Controller #2
(PCI) 0xFFFFFFFB (-5)	Intel(R) USB 3.0 eXtensible Host Controller - 0100 (Microsoft)
(PCI) 0xFFFFFFFC (-4)	Intel(R) HD Graphics
(PCI) 0xFFFFFFFD (-3)	PCI Express standard Root Port
(PCI) 0xFFFFFFFE (-2)	PCI Express standard Root Port

Appendix C

Digital I/O Ports

C.1 Electrical Specifications for Digital I/O Ports

Table 1 : Digital Input/Output Pin Electrical Specification						
Pin	Type	Input Threshold Voltage		Output Voltage		Note
		Low	High	Low	High	
DIO0	I/O	0.8	2.0	0	5	
DIO1	I/O	0.8	2.0	0	5	
DIO2	I/O	0.8	2.0	0	5	
DIO3	I/O	0.8	2.0	0	5	
DIO4	I/O	0.8	2.0	0	5	
DIO5	I/O	0.8	2.0	0	5	
DIO6	I/O	0.8	2.0	0	5	
DIO7	I/O	0.8	2.0	0	5	

Note: All DIO pins are 5V tolerant in input mode.

C.2 DI/O Programming

GENE-BSW5 utilizes FINTEK F81801U chipset as its Digital I/O controller. Below are the procedures to complete its configuration and the AAEON initial DI/O program is also attached, based on which you can develop customized program to fit your application.

There are three steps to complete the configuration setup:

(1) Enter the MB PnP Mode

(2) Modify the data of configuration registers

(3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

C.3 Digital I/O Register

Table 2 : SuperIO relative register table		
	Default Value	Note
Index	0x2E	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 3 : Digital Input/Output relative register table				
	LDN	Register	Bit	Note
GPIO0 Direction	0x06	0x88	0	0:input, 1: output
GPIO1 Direction	0x06	0x88	1	
GPIO2 Direction	0x06	0x88	2	
GPIO3 Direction	0x06	0x88	3	
GPIO4 Direction	0x06	0x88	4	
GPIO5 Direction	0x06	0x88	5	
GPIO6 Direction	0x06	0x88	6	
GPIO7 Direction	0x06	0x88	7	
GPIO0 Output Level	0x06	0x89	0	0:low, 1: high
GPIO1 Output Level	0x06	0x89	1	
GPIO2 Output Level	0x06	0x89	2	
GPIO3 Output Level	0x06	0x89	3	
GPIO4 Output Level	0x06	0x89	4	
GPIO5 Output Level	0x06	0x89	5	
GPIO6 Output Level	0x06	0x89	6	
GPIO7 Output Level	0x06	0x89	7	
GPIO0 Status	0x06	0x8A	0	0:low, 1: high
GPIO1 Status	0x06	0x8A	1	
GPIO2 Status	0x06	0x8A	2	
GPIO3 Status	0x06	0x8A	3	
GPIO4 Status	0x06	0x8A	4	
GPIO5 Status	0x06	0x8A	5	
GPIO6 Status	0x06	0x8A	6	
GPIO7 Status	0x06	0x8A	7	

C.4 Digital I/O Sample Program

```
*****************************************************************************
// SuperIO relative definition (Please reference to Table 2)
#define   SIOIndex   0x2E
#define   SIOData    0x2F
#define   DIOLDN     0x06
IOWriteByte(byte IOPort, byte Value);
IOReadByte(byte IOPort);
// DIO relative definition (Please reference to Table 3)
#define   DirReg_L        0x88        // 0:input, 1: output
#define   DirReg_H        0x80        // 0:input, 1: output
      #define   InputPin        0x00
      #define   OutputPin       0x01
#define   OutputReg_L     0x89        // 0:low, 1: high
#define   OutputReg_H     0x81        // 0:low, 1: high
#define   StatusReg_L     0x8A        // 0:low, 1: high
#define   StatusReg_H     0x82        // 0:low, 1: high
      #define   PinLow          0x00
      #define   PinHigh         0x01
#define   Pin0Bit         0x00
#define   Pin1Bit         0x01
#define   Pin2Bit         0x02
#define   Pin3Bit         0x03
#define   Pin4Bit         0x04
#define   Pin5Bit         0x05
#define   Pin6Bit         0x06
#define   Pin7Bit         0x07

*****************************************************************************

*****************************************************************************
VOID   Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //      Example, Read Digital I/O Pin 3 status
         // Output :
         //     InputStatus :
         //             0: Digital I/O Pin level is low
         //             1: Digital I/O Pin level is High
```

```
        PinStatus = AaeonReadPinStatus(Pin3Bit);

        // Procedure : AaeonSetOutputLevel
        // Input :
        //      Example, Set Digital I/O Pin 2 to high level
        AaeonSetOutputLevel(Pin2Bit, PinHigh);
}
*****************************************************************************

*****************************************************************************
Boolean   AaeonReadPinStatus(byte PinBit){
        Boolean PinStatus ;
        PinStatus = SIOBitRead(DIOLDN, StatusReg_L, PinBit);
        Return PinStatus ;
}
VOID   AaeonSetOutputLevel(byte PinBit, byte Value){
        ConfigDioMode(PinBit, OutputPin);
        SIOBitSet(DIOLDN, OutputReg_L, PinBit, Value);
}
*******************************************************************************

*******************************************************************************VOID
SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
         IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
```

```
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
         IOWriteByte(SIOData, Value);
         SIOExitMBPnPMode();
}
*******************************************************************************

*******************************************************************************
Boolean   SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, Register);
         TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID   ConfigDioMode(byte PinBit, byte Mode){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(DIOLDN);
        IOWriteByte(SIOIndex, DirReg_L);
        TmpValue = IOReadByte(SIOData);
        TmpValue |= (Mode << PinBit);
        IOWriteByte(SIOData, DirReg_L);
         SIOExitMBPnPMode();
}
*************************************************************************
```