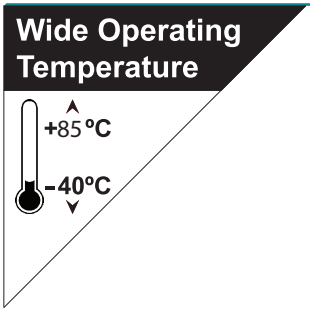

EmModule-7413

Wide Range Temperature
ETX-PC/104-Plus Complex

User's Manual

Version 1.0

2011.02

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Table of Content

Chapter 1

Introduction

1.1 Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.
Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

1.2 Declaration of Conformity

CE Class A

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in which case the user will be required to correct the interference at his own expense.

1.3 About This User's Manual

This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this User's Manual, please consult your vendor before further handling.

1.4 Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that came with the Single Board Computer, whenever components are separated from the system.

1.5 Replacing the lithium battery

Incorrect replacement of the lithium battery may lead to a risk of explosion. The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.
Do not throw lithium batteries into the trashcan. It must be disposed of in accordance with local regulations concerning special waste.

1.6 Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor.com.tw
E-mail:info@arbor.com.tw

1.7 Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.
Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantibility and fitness for particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

1.8 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

EmModule-7413 PC/104 plus module kit:
1 x ETX-742E ETX CPU Module
1 x PBE-1100-RG R3.x ETX 3.0 Carrier Board

1 x Driver CD

1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

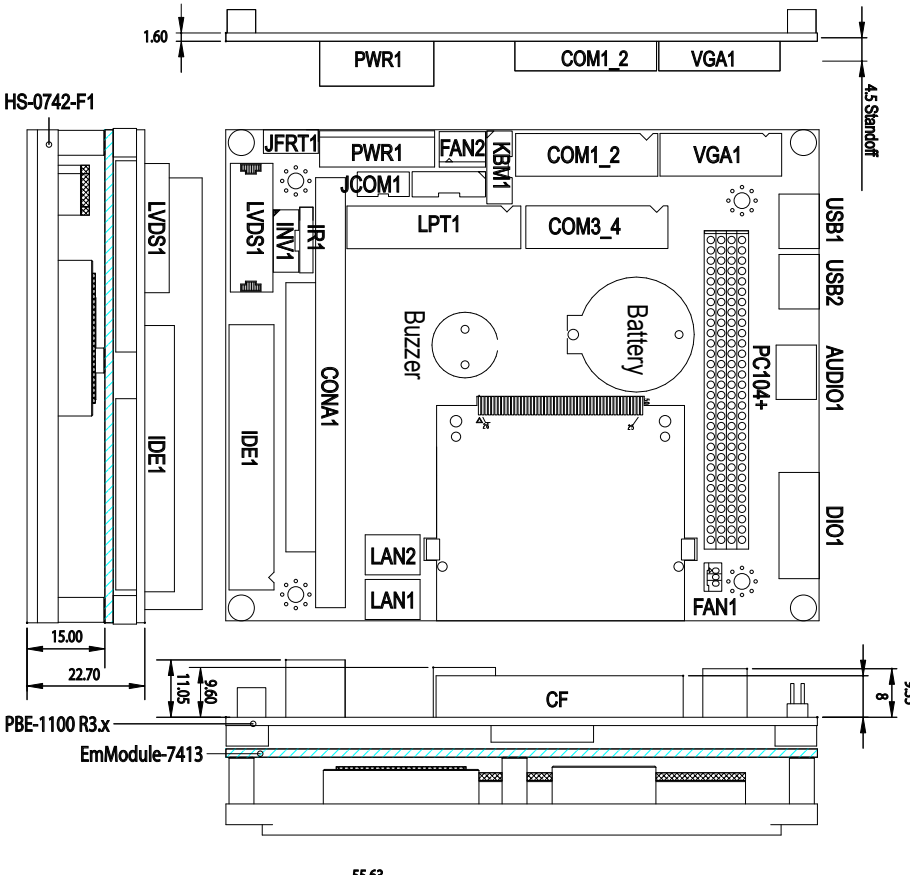
1.9 Ordering Information

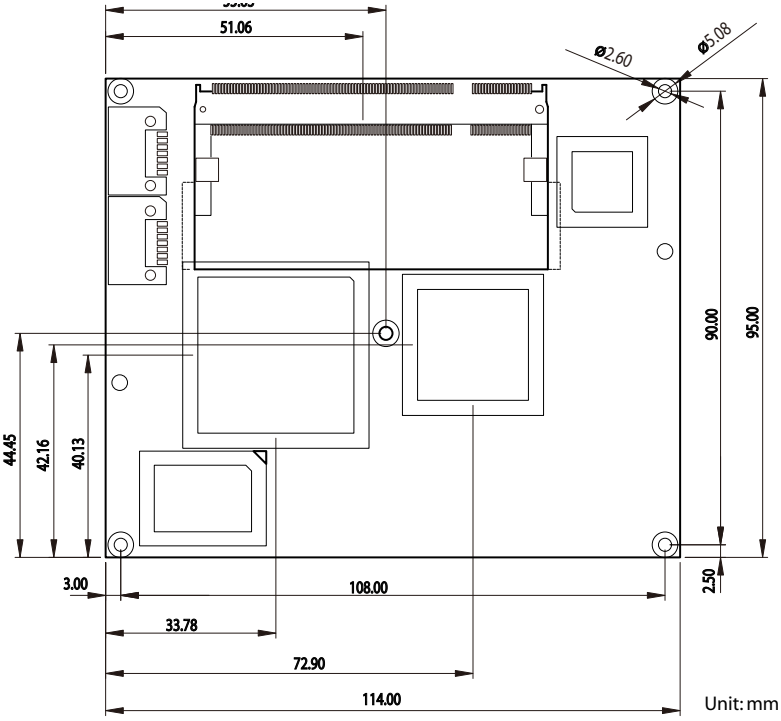
EmModule-7413-RG	ETX-742E ETX CPU Module + PBE-1100-RG R3.x ETX Carrier Board
CBK-16-1100-01	Cable Kit for PBE-1100 R3.x
HS-0742-F1	Heat Spreader (114 x 95 x 18mm)

1.10 Specifications

Form Factor	ETX-PC/104-Plus Complex CPU Module
CPU	Intel® Atom N450 1.6GHz CPU
Chipset	Intel® ICH8M
System Memory	1 x 200-pin SO-DIMM socket Up to 1GB DDR2 667MHz SDRAM
VGA/ LCD Controller	Intel® Graphics Media Accelerator 3150 graphics core with Analog RGB/ Single Channel 18-bit LVDS (Dual independent displays)
Ethernet	1 x Realtek RTL8103EL 10/100 Base-T Ethernet from CPU module
	1 x Realtek RTL8110SCL GbE from PBE-1100-RG
BIOS	AMI PnP Flash BIOS
Serial ATA	2 x Serial ATA with 300MB/s HDD transfer rate
IDE Interface	1 x IDE (Ultra ATA 33), support 2 IDE devices
Serial Port	4 x COM ports (COM1, 3, 4: RS-232, COM2: RS-232/422/485 selectable)
Parallel Port/ Floppy	1 x SPP/EPP/ECP mode 1 x Floppy connector, (shared with Parallel Port #1)
Keyboard / Mouse	One 1x6 wafer connector for Keyboard and Mouse
Universal Serial Bus	4 x USB 2.0 ports
LCD	Single Channel 18-bit LVDS
Expansion Interface	1 x CF II socket shared with IDE1 1 x PCI/104 PCI bus 1 x PC/104 ISA bus
Operation Temp.	-40ºC ~ 85ºC (-40ºF ~ 185ºF)
Watchdog Timer	1~255 levels Reset
Dimension (L x W)	114 x 95 mm (4.5” x 3.7”)

1.11 Board Dimensions

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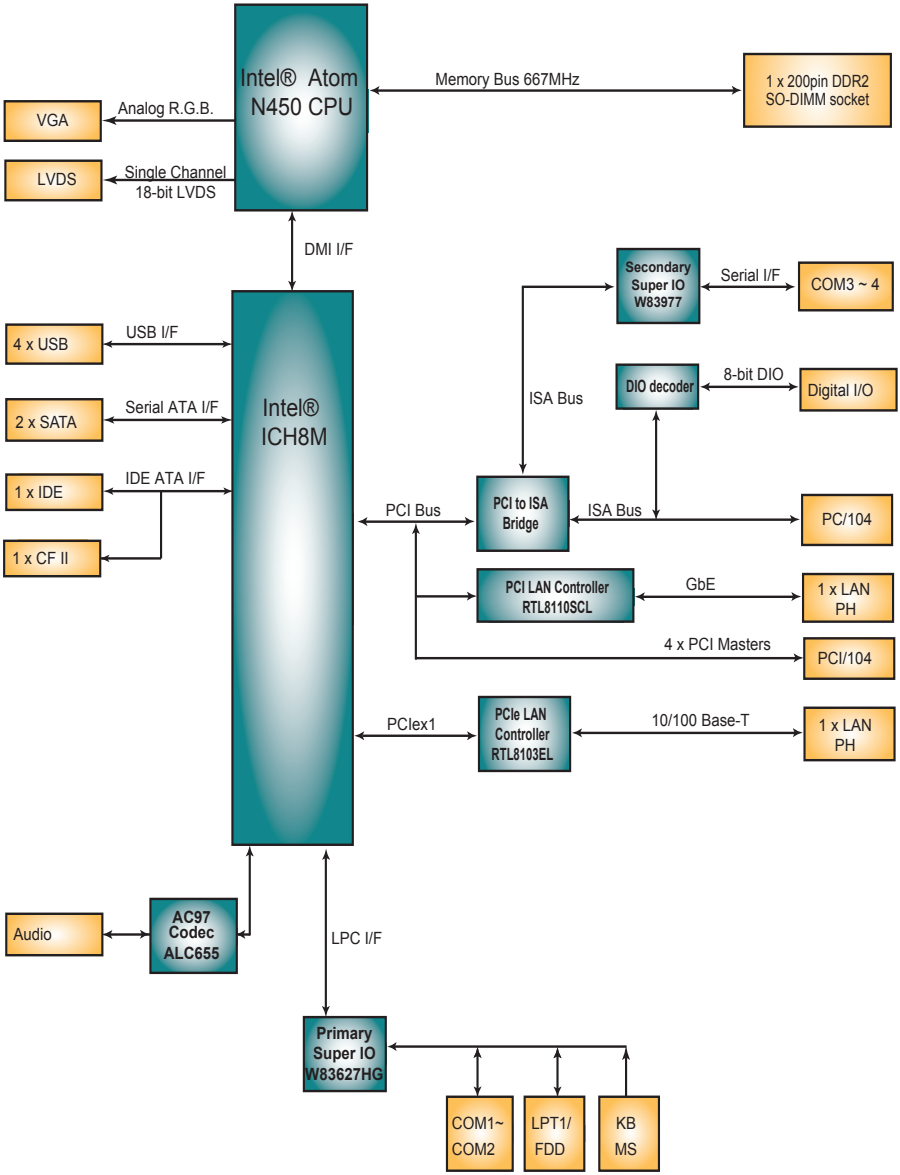
Unit: mm

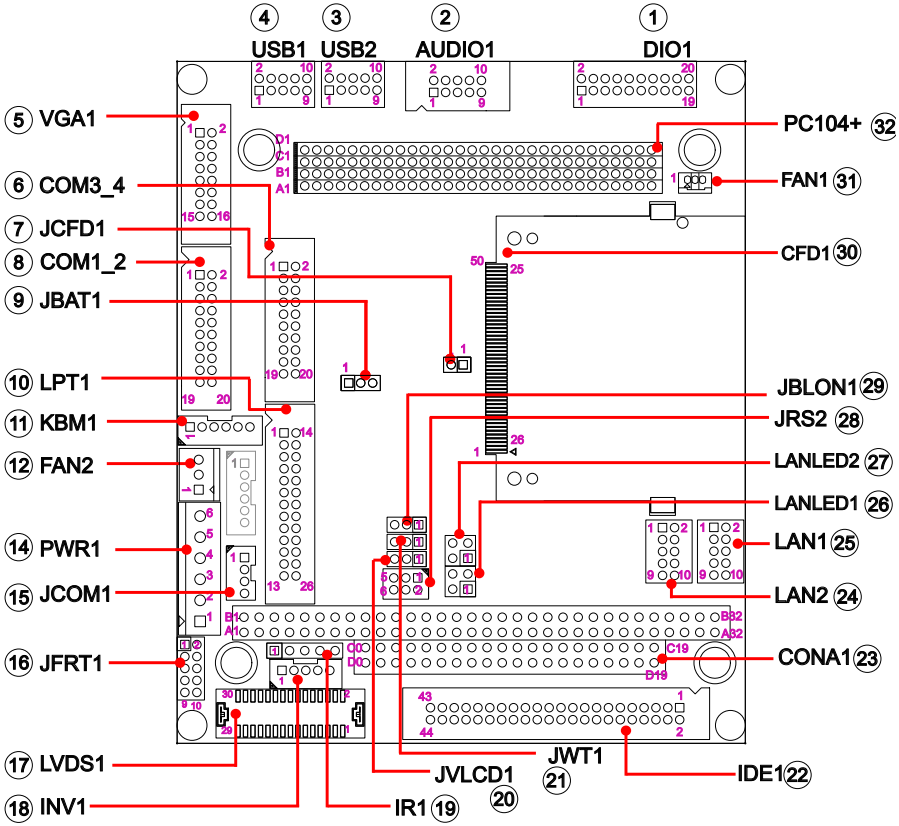
Chapter 2

Installation

2.1 Block Diagrams



2.2 Connectors



Jumpers

JCFD1: CF IDE1 Mode Selection (7)

Connector type: 2.54mm pitch 1x2-pin headers.

Pin	Mode	
Short	Master	
Open	Slave (Default)	

JBAT1: Clear CMOS Setting (9)

If the board refuses to boot due to inappropriate CMOS settings here is how to proceed to clear (reset) the CMOS to its default values.
Connector type: 2.54 mm pitch 1x3-pin headers

Pin	Mode	
1-2	Keep CMOS (Default)	
2-3	Clear CMOS	

You may need to clear the CMOS if your system cannot boot up because you forgot your password, the CPU clock setup is incorrect, or the CMOS settings need to be reset to default values after the system BIOS has been updated. Refer to the following solutions to reset your CMOS setting:

Solution A:

1. Power off the system and disconnect the power cable.
2. Place a shunt to short pin 2 and pin 3 of JBAT1 for five seconds.
3. Place the shunt back to pin 1 and pin 2 of JBAT1.
4. Power on the system.

Solution B:

If the CPU Clock setup is incorrect, you may not be able to boot up. In this case, follow these instructions:

1. Turn the system off, then on again. The CPU will automatically boot up using standard parameters.
2. As the system boots, enter BIOS and set up the CPU clock.

Note:

If you are unable to enter BIOS setup, turn the system on and off a few times.

JVLCD1: LCD Panel Voltage Selection (20)

The voltage of LCD panel could be selected by JVLCD1 in +5V or +3.3V.
Connector type: 2.54 mm pitch 1x3-pin headers

Pin	Voltage	
1-2	+5V	
2-3	+3.3V (Default)	

JWT1: WDT Mode Setting (21)

WDT is widely used for industry application to monitoring the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. The WDT will not be reload by an abnormal system, then WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming I/O ports.

Pin	Voltage	
1-2	NMI	
2-3	RST_SW (Default)	
none	Disable WatchDog Timer	

JRS2: COM2 RS-232/422/485 Selection (28)

The onboard COM2 port can be configured to operate in RS-422 or RS-485 modes. RS-422 modes differ in the way RX/TX is being handled. Jumper JRS1 switches between RS-232 or RS-422/485 mode.
Connector type: 2.00mm pitch 2x3-pin headers.

Mode	RS-232 (Default)	RS-422	RS-485
1-2	ON	OFF	OFF
3-4	OFF	ON	OFF
5-6	OFF	OFF	ON
			

JBLON1: LCD Backligh Selection (29)

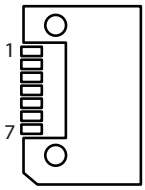
The LCD panel backlight active mode could be selected by JBLON1 in High or Low.
Connector type: 2.00mm pitch 1x3-pin headers.

Pin	Mode	
1-2	Active High (Default)	
2-3	Active Low	

Connectors

SATA1~2: Serial ATA Connectors

Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

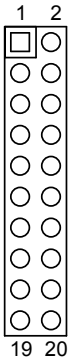


These connectors are on the top side of the module kit.

DIO1: Digital I/O Connector (1)

DIO1 is a 16-bit DIO connector that supports 8-bit In/ 8-bit Out.
Connector type: 2.00 mm pitch 2x10-pin headers.
Output Port IO Based Address: 208H
Input Port IO Based Address: 200H

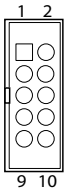
Pin	Description	Pin	Description
1	DO0	2	DO1
3	DO2	4	DO3
5	DO4	6	DO5
7	DO6	8	DO7
9	GND	10	GND
11	DI0	12	DI1
13	DI2	14	DI3
15	DI4	16	DI5
17	DI6	18	DI7
19	+5V	20	+12V



AUDIO1: AC97 Connector (2)

Connect a tape player or another audio source to the light blue Line-in connector to record audio on your computer or to play audio through your computer's sound chip and speakers.
Connect a micro-phone to the pink microphone connector to record audio to your computer.
Connector type: 2.00mm pitch 2x5-pin box headers.

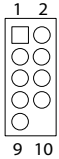
Pin	Description	Pin	Description
1	Line-in Left	2	Line-in Right
3	GND	4	GND
5	MIC	6	N/C
7	GND	8	GND
9	Line-out Left	10	Line-out Right



USB1~ 2: USB Connectors (4, 3)

The module on board supports two headers USB1, and USB2 that can connect up to four high-speed (Data transfers at 480Mb/s), full-speed (Data transfers at 12Mb/s) or low-speed (Data transfers at 1.5Mb/s) USB devices.
Connector type: 2.00mm 2x5-pin headers

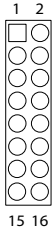
Pin	Description	Pin	Description
1	+5V	2	+5V
3	USBD-	4	USBD-
5	USBD+	6	USBD+
7	GND	8	GND
9	N/C	10	N/C (Key)



VGA1: Analog RGB Connector (5)

Connector type: 2.00mm pitch 2x8-pin headers.

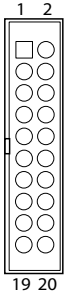
Pin	Description	Pin	Description
1	RED	2	GREEN
3	BLUE	4	N/C
5	GND	6	GND
7	GND	8	GND
9	N/C	10	GND
11	N/C	12	VDDAT
13	HSYNC	14	VSYNC
15	VDCLK	16	N/C



COM1_2/ COM3_4: RS-232 Connectors (6, 8)

Connector type: 2.00mm pitch 2x10-pin box headers.

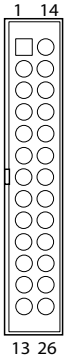
Pin	Description	Pin	Description
1	DCD#1 / 3	2	RXD1 / 3
3	TXD1 / 3	4	DTR#1 / 3
5	GND	6	DSR#1 / 3
7	RTS#1 / 3	8	CTS#1 / 3
9	RI#1 / 3	10	N/C
11	DCD#2/ 4	12	RXD2/ 4
13	TXD2/ 4	14	DTR#2/ 4
15	GND	16	DSR#2/ 4
17	RTS#2/ 4	18	CTS#2/ 4
19	RI#2/ 4	20	N/C



LPT1: Parallel Port Connector (10)

Connector type: 2.54mm pitch 2x13-pin box headers.
Shared with FDD port connector, LPT can be configured as a connector floppy disk drive interface through BIOS setup.

Pin	Description	Pin	Description
1	STB#	14	AFD#
2	PTD0	15	ERROR#
3	PTD1	16	INIT#
4	PTD2	17	SLIN#
5	PTD3	18	GND
6	PTD4	19	GND
7	PTD5	20	GND
8	PTD6	21	GND
9	PTD7	22	GND
10	ACK#	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SELECT	26	N/C



BIOS Setup

The default is to set LPT1 as FDD connector. To change the value, get into BIOS setup --> Integrated Peripheral --> Super IO Device.

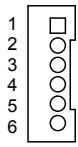
BIOS Option	Setting	Description
External FDD Controller	Enabled	Set as FDD connector
Onboard Parallel Port	Disabled	
External FDD Controller	Disabled	
Onboard Parallel Port	378/IRQ7	Set as Parallel Port

Note:
1. When FDD active, LPT is not able to use, vice versa.
2. Floppy drive LED always light on when LPT to FDD cable connected.

KBM1: Keyboard & Mouse Connector (11)

Connector type: 2.0mm pitch 1x6-pin box wafer connector.

Pin	Description
1	KB_DATA
2	GND
3	MS_DATA
4	KB_CLK
5	KB_VCC
6	MS_CLK



FAN2: Fan Connectors (12)

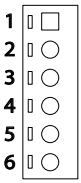
FAN2 is a 3-pin headers for the fan. The fan must be a +12V fan.

Pin	Description
1	GND
2	+12V
3	N/C

PWR1: Power Supply Connector (14)

Connector type: Terminal Blocks

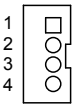
Pin	Description
1	+12V
2	GND
3	GND
4	GND
5	+5V
6	+5V



JCOM1: RS-422/ 485 Output Connector (15)

Connector type: 2.00mm pitch 1x4 box wafer connector

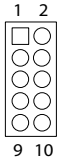
Pin	RS-422	RS-485
1	TX+	Data+
2	TX-	Data-
3	RX+	N/C
4	RX-	N/C



JFRT1: Switches and Indicators (16)

It provides connectors for system indicators that provides light indication of the computer activities and switches to change the computer status.
Connector type: 2.00 mm pitch 2x5-pin headers

Pin	Description	Pin	Description
1	RESET+	2	RESET-
3	POWER LED+	4	POWER LED-
5	HDD LED+	6	HDD LED-
7	SPEAKER+	8	SPEAKER-
9	ETXSMI	10	GND



RES: Reset Button, pin 1-2.

This 2-pin connector connects to the case-mounted reset switch and is used to reboot the system.

PLED: Power LED Connector, pin 3-4.

This 2-pin connector connects to the case-mounted power LED. Power LED can be indicated when the CPU card is on or off. And keyboard lock can be used to disable the keyboard function so the PC will not respond by any input.

HLED: HDD LED Connector, pin 5-6.

This 2-pin connector connects to the case-mounted HDD LED to indicate hard disk activity.

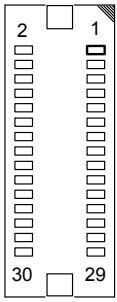
SPK: External Speaker, pin 7-8.

This 2-pin connector connects to the case-mounted speaker.

LVDS1: LVDS Connector (17)

The LVDS connector supports single channel 18-bit LVDS.
VDD could be selected by JVLCD1 in +5V or +3.3V.
Connector type: DF-13-30DP-1.25V

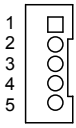
Pin	Description	Pin	Description
2	VDD	1	VDD
4	N/C	3	TX1CLK+
6	N/C	5	TX1CLK-
8	GND	7	GND
10	N/C	9	TX1D0+
12	N/C	11	TX1D0-
14	GND	13	GND
16	N/C	15	TX1D1+
18	N/C	17	TX1D1-
20	GND	19	GND
22	N/C	21	TX1D2+
24	N/C	23	TX1D2-
26	GND	25	GND
28	N/C	27	N/C
30	N/C	29	N/C



INV1: LCD Inverter Connector (18)

Connector type: 2.00mm pitch 1x5-pin box wafer connector.

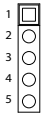
Pin	Description
1	+12V
2	GND
3	Backlight on/off
4	Brightness control
5	GND



IR1: Infrared Connector (19)

Connector type: 2.54mm pitch 1x5-pin headers

Pin	Description
1	+5V
2	N/C
3	IRRX
4	GND
5	IRTX



The IR connector can be configured to support wireless infrared module, user can transfer files to or from notebooks, PDA and printers.

Install infrared module onto IrDA connector and enable infrared function from BIOS setup and make sure to have correct orientation when you plug onto IrDA connector.

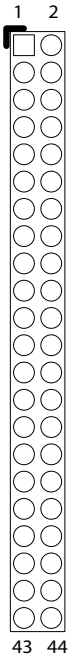
IDE1: IDE Connector (22)

An IDE drive ribbon cable has two connectors to support two IDE devices. If a ribbon cable connects to two IDE drives at the same time, one of them has to be configured as Master and the other has to be configured as Slave by setting the drive select jumpers on the drive.

Consult the documentation that came with your IDE drive for details on jumper locations and settings. You must orient the cable connector so that the pin 1 (color) edge of the cable corresponds to pin 1 of the IDE connector.

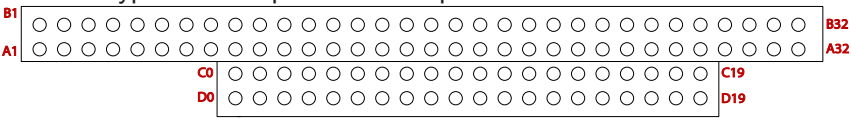
Connector type: 2.0mm pitch 2x22-pin headers

Pin	Description	Pin	Description
1	RESET#	2	GND
3	DATA7	4	DATA8
5	DATA6	6	DATA9
7	DATA5	8	DATA10
9	DATA4	10	DATA11
11	DATA3	12	DATA12
13	DATA2	14	DATA13
15	DATA1	16	DATA14
17	DATA0	18	DATA15
19	GND	20	N/C
21	DREQ	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IRDY	28	N/C
29	ACK#	30	GND
31	IRQ	32	N/C
33	AD1	34	ATA66 DETECT
35	AD0	36	AD2
37	CS#2	38	CS#3
39	ACT#	40	GND
41	+5V	42	+5V
43	GND	44	N/C



CONA1: PC/104 ISA Interface (23)

Connector type: PC/104 press fit 2x20-pin connector

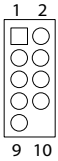


Pin	Description	Pin	Description	Pin	Description	Pin	Description
D0	GND	C0	GND	A1	IOCHCK#	B1	GND
D1	MEMCS16#	C1	SBHE#	A2	SD7	B2	RST_DRV
D2	IOCS16#	C2	LA23	A3	SD6	B3	+5V
D3	IRQ10	C3	LA22	A4	SD5	B4	IRQ9
D4	IRQ11	C4	LA21	A5	SD4	B5	N/C
D5	IRQ12	C5	LA20	A6	SD3	B6	DREQ2
D6	IRQ15	C6	SA19	A7	SD2	B7	N/C
D7	IRQ14	C7	SA18	A8	SD1	B8	0WS#
D8	DACK0#	C8	SA17	A9	SD0	B9	+12V
D9	DREQ0	C9	MEMR#	A10	IOCHRDY	B10	GND
D10	DACK5#	C10	MEMW#	A11	AEN	B11	SMEMW#
D11	DREQ5	C11	SD8	A12	SA19	B12	SMEMR#
D12	DACK6#	C12	SD9	A13	SA18	B13	IOW#
D13	DREQ6	C13	SD10	A14	SA17	B14	IOR#
D14	DACK7#	C14	SD11	A15	SA16	B15	DACK3#
D15	DREQ7	C15	SD12	A16	SA15	B16	DREQ3
D16	+5V	C16	SD13	A17	SA14	B17	DACK1#
D17	MASTER#	C17	SD14	A18	SA13	B18	DREQ1
D18	GND	C18	SD15	A19	SA12	B19	REFRESH#
D19	GND	C19	GND	A20	SA11	B20	SYSCLK
				A21	SA10	B21	IRQ7
				A22	SA9	B22	IRQ6
				A23	SA8	B23	IRQ5
				A24	SA7	B24	IRQ4
				A25	SA6	B25	IRQ3
				A26	SA5	B26	DACK2#
				A27	SA4	B27	TC
				A28	SA3	B28	BALE
				A29	SA2	B29	+5V
				A30	SA1	B30	ISA_CLK
				A31	SA0	B31	GND
				A32	GND	B32	GND

LAN1 ~ 2: Ethernet Connectors (25, 24)

Connector type: 2.0mm pitch 2x5-pin headers

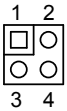
Pin	Description	Pin	Description
1	TX_MDI0+	2	TX_MDI0-
3	RX_MID1+	4	MDI2-
5	MDI2-	6	RX_MDI1-
7	MDI3+	8	MDI3-
9	N/C	10	N/C (Key)



LANLED1, LANLED2: LAN1, LAN2 LED Indicators (26, 27)

Connector type: 2.54mm pitch 2x2-pin headers.

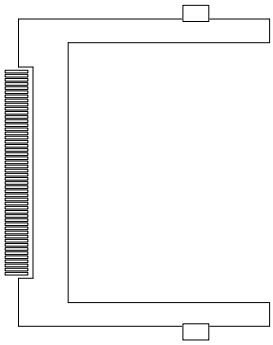
Pin	Description	Pin	Description
1	ACTLED-	2	ACTLED+
3	LILED-	4	LILED+



CFD1: Compact Flash Type II Socket (30)

Connector type: 50-pin compact flash connector

Pin	Description	Pin	Description
1	GND	26	N/C
2	PDD3	27	PDD11
3	PDD4	28	PDD12
4	PDD5	29	PDD13
5	PDD6	30	PDD14
6	PDD7	31	PDD15
7	PDCS1#	32	PDCS3#
8	GND	33	N/C
9	GND	34	PDIOR#
10	GND	35	PDIOW#
11	GND	36	+5V
12	GND	37	PIDEIRQ
13	+5V	38	+5V
14	GND	39	CSEL#
15	GND	40	N/C
16	GND	41	IDERST#
17	GND	42	PIORDY
18	PDA2	43	PDDREQ
19	PDA1	44	PDDACK#
20	PDA0	45	HD_LED1#
21	PDD0	46	PDIAG#
22	PDD1	47	PDD8
23	PDD2	48	PDD9
24	N/C	49	PDD10
25	N/C	50	GND



The interface of Compact Flash socket is designated to use IDE1.

Installation instructions

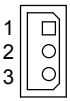
Compact Flash (CF) card is “not hot-swappable”. If the CF card is swapped in the condition of system power-on, it will damage the CF card.

1. Make sure the Single Board Computer is powered OFF.
2. Plug the Compact Flash Type II device into its socket. Verify the direction is correct.
3. Power up the system.

FAN1: System Fan Connector (31)

FAN1 is a 3-pin headers for the System fan. The fan must be a +5V fan.

Pin	Description
1	N/C
2	+5V
3	GND



PC104+: PC/104-Plus PCI Bus Expansion Slot (32)

2.3 The Installation Paths of CD Driver

Windows 2000 & XP

Driver	Path
CHIPSET	\CHIPSET\INTEL\INF 9.11
VGA	\GRAPHICS\INTEL_2K_XP_32\5182
AUDIO	\AUDIO\REALTEK_HD\WIN2K_XP_x86x64_R252
LAN	\ETHERNET\REALTEK\8103EL_WIN5736 \ETHERNET\REALTEK\8110SCL_XP_2K_5719

Windows 7

Driver	Path
CHIPSET	\CHIPSET\INTEL\INF 9.11
VGA	\GRAPHICS\INTEL_WIN7_32\2230
AUDIO	\AUDIO\REALTEK_HD\Win7_R257
LAN	\ETHERNET\REALTEK\8103EL_Win7_7040 \ETHERNET\REALTEK\8110SCL_Win7_7037

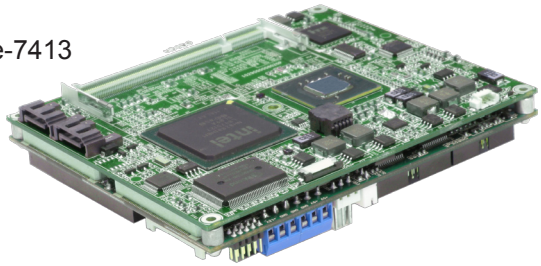
2.4 Heatsink Installation and Replacement

Please follow the steps and the figure below for heatsink installation and replacement.

1. Align the screw holes for the module kit and the heatsink.

HS-0742-F1

EmModule-7413



2. Tighten and secure with proper-sized screws.

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Chapter 3

BIOS

3.1 BIOS Introduction

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility and configurations.

When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILILTY, press “Delete” once the power is turned on.

When the computer is shut down, the battery on the motherboard supplies the power for BIOS RAM.

The Main Setup screen lists the following information

System Overview

BIOS Version: displays the current version information of the BIOS

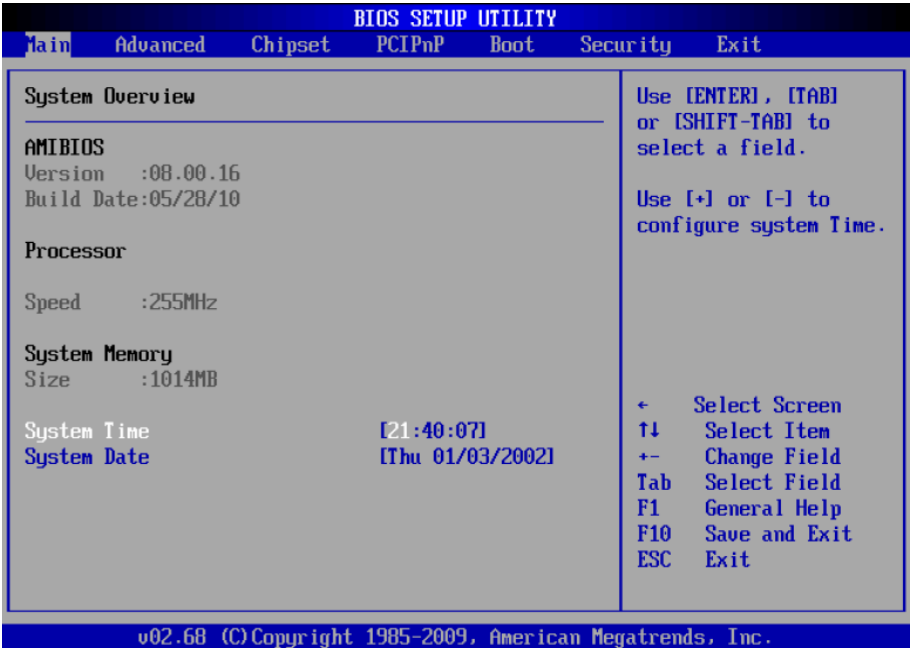
Build Date: the date that the BIOS version was made/updated

Processor (auto-detected if installed)

Speed: displays the processor speed

System Memory (auto-detected if installed)

Size: lists the memory size information



Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

"←""→"	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
"↓" "↑"	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select "OK" or "Cancel" for exiting and discarding changes. Use "←" and "→" to select and press "Enter" to confirm) On the Sub Menu – Exit current page and return to main menu
Page Up / +	Increase the numeric value on a selected setup item / make change
Page Down -	Decrease the numeric value on a selected setup item / make change
F1	Activate "General Help" screen
F10	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select "OK" or "Cancel" for exiting and saving changes. Use "←" and "→" to select and press "Enter" to confirm)

System Time

Set the system time.
The time format is:
Hour : 00 to 23
Minute : 00 to 59
Second : 00 to 59

System Date

Set the system date. Note that the 'Day' automatically changes when you set the date.
The date format is:
Day : Sun to Sat
Month : 1 to 12
Date : 1 to 31
Year : 1999 to 2099

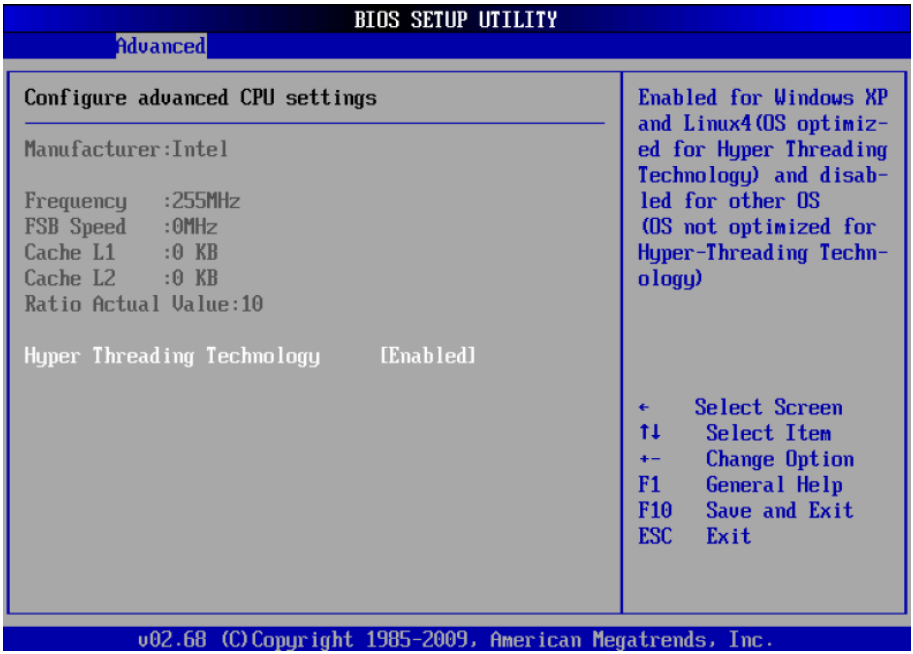
3.2 Advanced Settings

The “Advanced” screen provides the setting options to configure CPU, IDE, SuperIO and other peripherals. You can use “←” and “→” keys to select “Advanced” and use the “↓” and “↑” to select a setup item.

Note: please pay attention to the “WARNING” part at the left frame before you decide to configure any setting of an item.

3.2.1 CPU Configuration

Press “Enter” on “CPU Configuration” and you will be able to configure the CPU on the “Configure advanced CPU settings” screen.



CPU Details

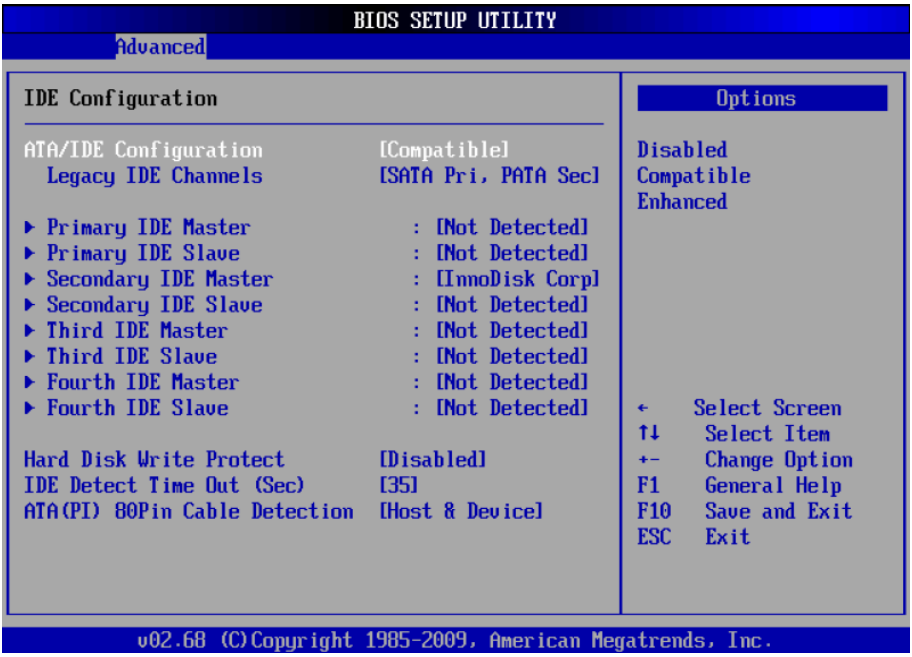
Manufacturer: shows the name of the CPU manufacturer
Frequency: indicates the processor speed
FSB Speed: the data flow speed of FSB (Front Side Bus)
Cache L1: shows the Cache L1 size for the CPU
Cache L2: shows the Cache L2 size for the CPU
Ratio Actual Value: actual value of clock ratio for the CPU

Hyper-Threading Technology

Enabled: activates the Hyper-Threading Technology for higher CPU threading speed. (Recommended)
Disabled: Disactivates the Hyper-Threading Technology.

3.2.2 IDE Configuration

Select the “IDE Configuration to configure the IDE settings. When an item is selected, there is a status description appearing at the right. You can use “Page Up/+” and “Page Down/-” keys to change the value of a selected item.



ATA/IDE Configuration

Configures the options of ATA/IDE controllers connected to the board
Disabled: disables the ATA/IDE controllers connected to the board
Compatible: sets the ATA/IDE controllers to be compatible
Enhanced: sets the ATA/IDE controllers to be in enhanced mode

Legacy IDE Channels (SATA Pri, PATA Sec)

Specifies SATA or PATA controllers to be primary or secondary.

Primary IDE Master/Slave, Secondary IDE Master/Slave, Third IDE Maser/Slave, Fourth IDE Master/Slave

The BIOS Setup displays all the available, connected IDE devices as well as the IDE status. You may enter a specific IDE device to do particular configurations. Press “Enter” to access the submenu of an IDE device on the list.

Hard Disk Write Protect

Enable or disable Hard Disk Write Protect. If you select “Enabled”, the hard disk will turn into a “write-protected” mode.

IDE Detect Time-out (sec)

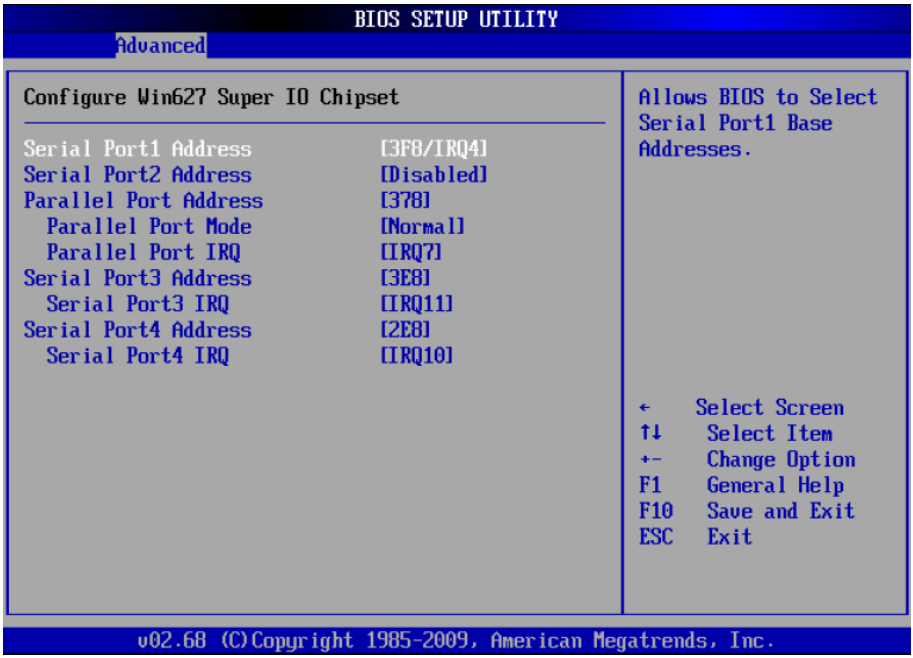
Specifies the delay time for initializing IDE devices. The default value is 0.

ATA (PI) 80Pin Cable Detection

You can set it as “Host & Device”, “Host” or “Device”. Host refers to the capability of IDE controllers to be able to detect connected IDE cable, while Device is defined as the ability of IDE devices to recognize the connected IDE cable.

3.2.3 Super IO Configuration

Use “Super IO Configuration to specify address and modes for Serial Port and Parallel Port.



Serial Port1 / Port2 Address

Select an address and corresponding interrupt for the first and second serial ports.

The choice:

3F8/IRQ4
2E8/IRQ3
3E8/IRQ4
2F8/IRQ3
Disabled
Auto

Serial Port2 Mode

Allows BIOS to select mode for serial Port2.

Parallel Port Address

Select an address for the parallel port.
The choice:
- 3BC
- 378
- 278
- Disabled

Parallel Port Mode

Select an operating mode for the onboard parallel port. Select Normal, Compatible or SPP unless you are certain your hardware and software both support one of the other available modes.
The choice:
- SPP
- EPP
- ECP
- ECP + EPP
- Normal

Parallel Port IRQ

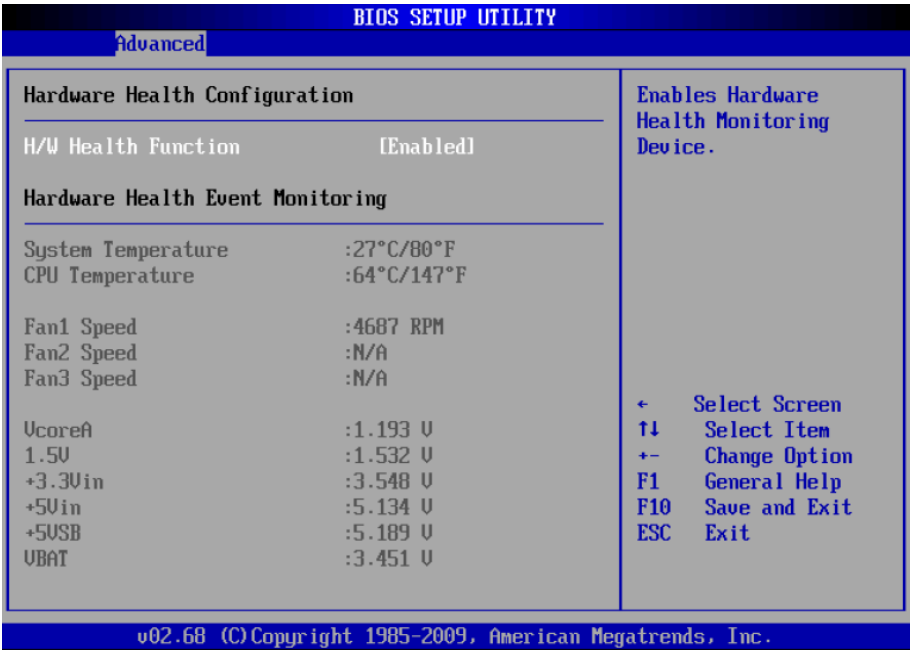
Select an interrupt for the parallel port.
The choice:
- IRQ5
- IRQ7

Serial Port 3 / Port 4 Address

Select an address and corresponding interrupt for the first and second serial ports.
The choice:
- 3F8
- 2F8
- 2E8
- 3E8 (Default)
- Disabled
- Auto
- * The IRQ are 10 and 11 respectively.

3.2.4 Hardware Health Configuration

The “Hardware Health Configuration” lists out the temperature and voltage information that is being monitored. The default for “H/W Health Function” is “Enabled.



System/ CPU Temperature

Show you the current System / CPU fan temperature.

CPU / System / Chassis Fan Speed

Show you the current CPU / System / Chassis Fan operating speed.

Vcore

Show you the voltage level of CPU (Vcore).

+1.5V / +3.3Vin / +5Vin / 5VSB / VBAT

Show you the voltage level of the +1.5V, +3.3Vin, +5Vin, 5VSB and battery.

3.2.5 USB Configuration

Legacy USB Support

Enables support for legacy USB. AUTO option disables legacy support if no USB devices are connected.

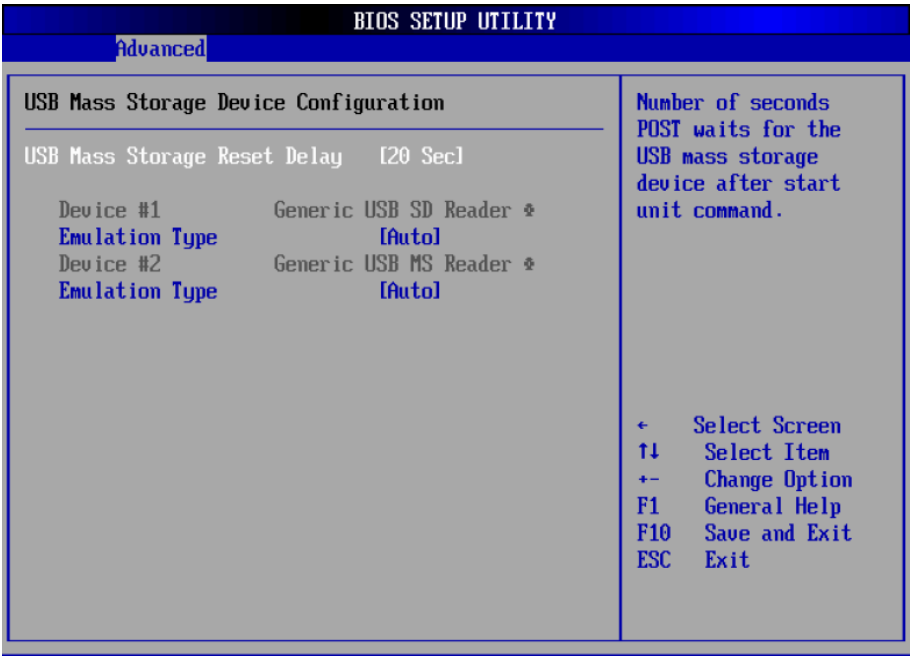
USB 2.0 Controller Mode

Configures the USB 2.0 controller in High Speed (480Mbps) or Full Speed (12Mbps).

BIOS EHCI Hand-Off

Enabled: enables the EHCI Hand-Off function by BIOS
Disabled: disables the EHCI Hand-Off function by BIOS
Note: this setting potion allows you to enable EHCI Hand Off if your computer operating system does not support it.
EHCI is the abbreviation for Enhanced Host Controller Interface which is necessary for high speed USB operation.

3.2.6 USB Mass Storage Device Configuration



USB Mass Storage Reset Delay

Number of seconds POST waits for the USB mass storage device after start unit command.

Emulation Type

If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to BOOT as FDD. (Ex. ZIP drive).

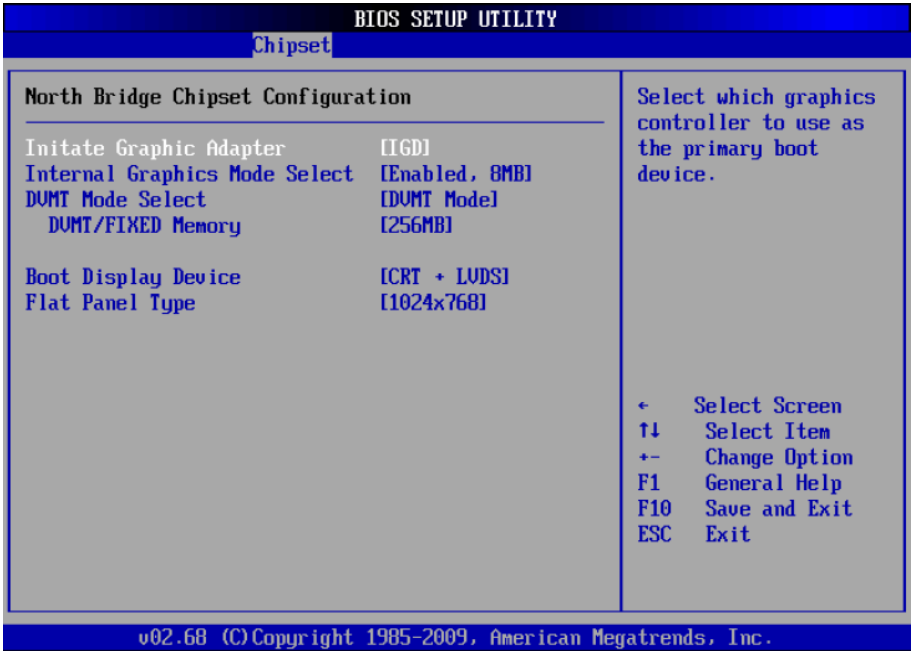
Note

If “Auto” is selected, USB device with storage less than 530MB will be emulated as Floppy and remain as hard drive. Forced FDD option can be used to force a HDD formatted drive to “BOOT” as FDD (for example, ZIP drive)

3.3 Advanced Chipset Settings

Select “Chipset” to access to “North Bridge Configuration” and “South Bridge Configuration”. You can enter the sub menu of the two configuration options.

3.3.1 North Bridge Chipset Configuration



Initate Graphic Adapter

Select which graphics controller to use as the primary boot device.

Internal Graphic Mode Select

Select the amount of system memory used by the Internal graphics device.

DVMT Mode

Setting: FIXED, DVMT (Default), BOTH.

DVMT/FIXED Memory Size

Setting: 64MB, 128MB (Default), 256MB.

Boot Display Device

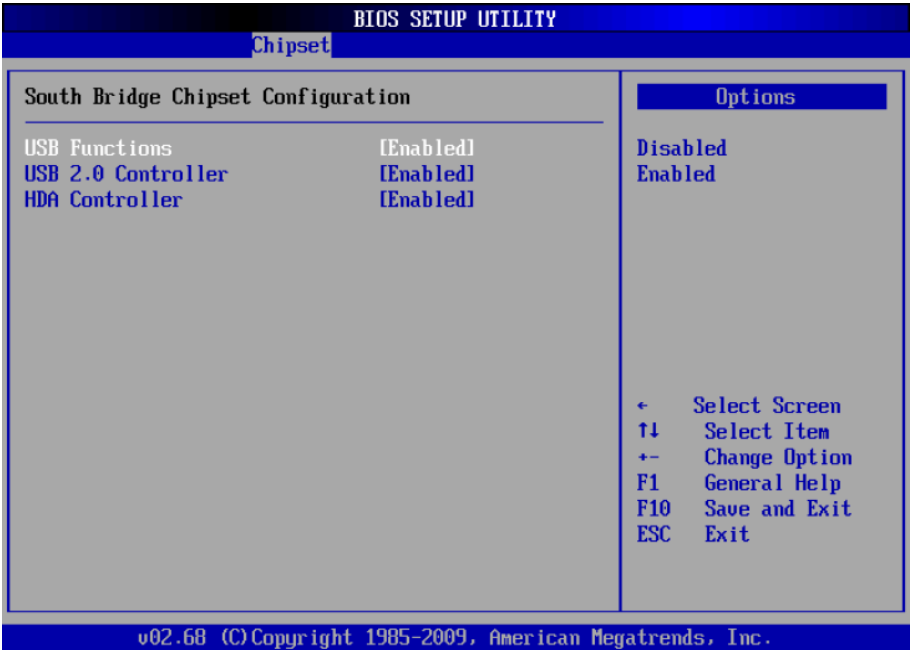
Boot setting for the display device connected to the computer, such as “CRT” monitor.

Flat Panel Type

The resolution types of the connected flat panel display device.

3.3.2 South Bridge Chipset Configuration

Normally, the south bridge controls the basic I/O functions, such as USB and audio. This screen allows you to access to the configurations of the I/Os.



USB Funtion

This item allows you to active USB ports.

The Choice: Disabled, 2 USB Ports, 4 USB Ports

USB 2.0 Controller

Select “Enabled” if your system contains a Universal Serial Bus 2.0 (USB 2.0) controller and you have USB peripherals.

The Choice: Enabled, Disabled.

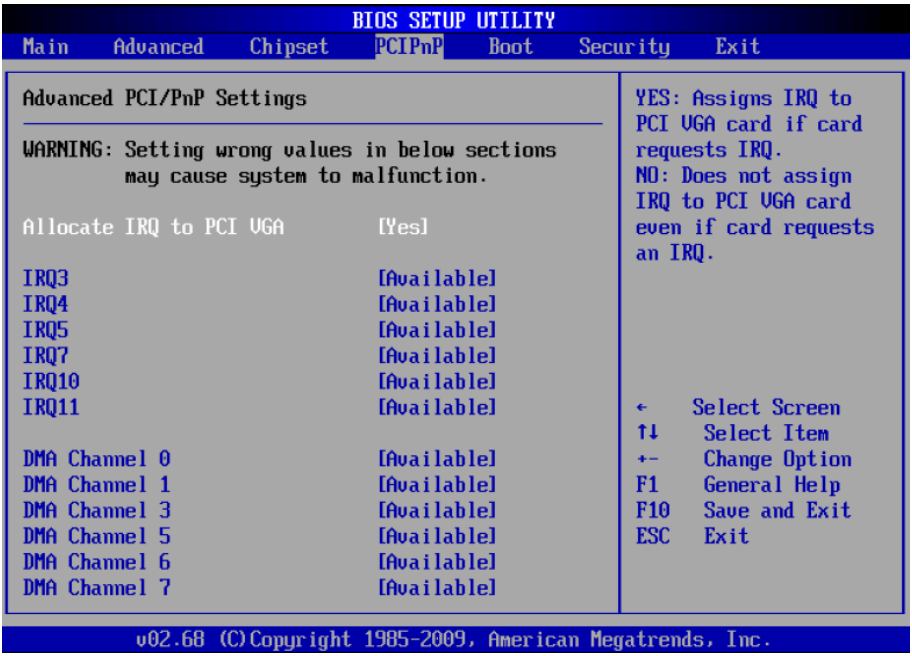
HDA Controller

This item allows you to select the chipset family to support High Definition Audio Controller.

The Choice: Enabled, Disabled.

3.3 Advanced PCI/PnP Settings

The “PCIPnP” screen provides advanced setting options for your PCI or PnP (plug and play) peripherals.



Allocate IRQ to PCI VGA

Yes: Assigns IRQ to PCI VGA card if card requests IRQ.
No: Does not assign IRQ to PCI VGA card even if card requests an IRQ.
[Available]: if an item is specified “Available”, the particular item can be used by PCI or PnP peripherals/devices
[Reserved]: if an item is specified as “Reserved”, the particular item can only be used by legacy ISA peripherals/devices
Note: please pay attention to the “WARNING” part at the left frame before you decide to configure any setting of an item.

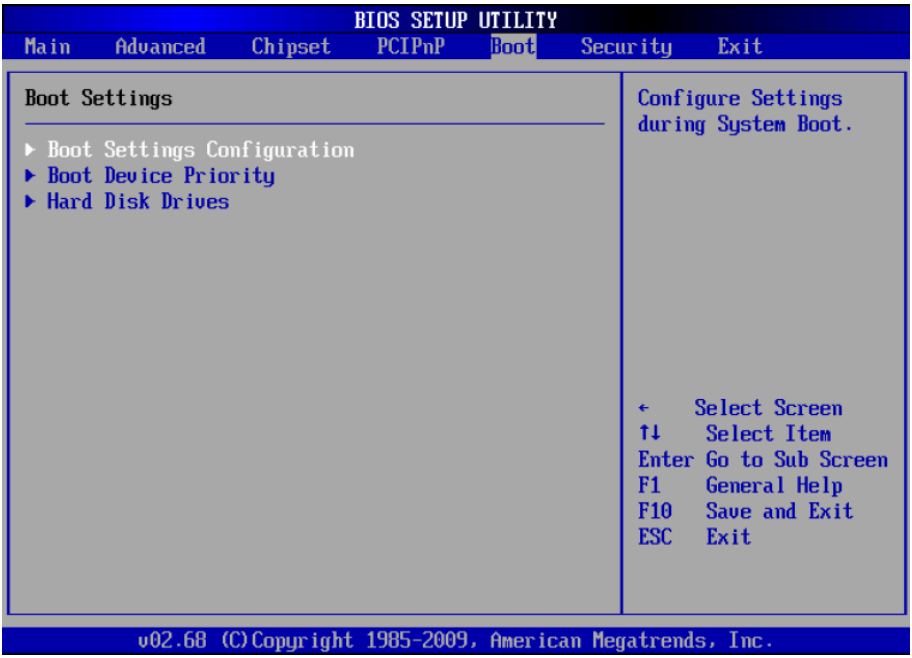
IRQ3 - IRQ15

Available: Specified IRQ is available to be used by PCI/PnP devices.
Reserved: Specified IRQ is reserved for use by Legacy ISA devices.

DMA Channel 0 - DMA Channel 7

Available: Specified DMA is available to be used by PCI/PnP devices.
Reserved: Specified DMA is reserved for use by Legacy ISA devices.

3.4 Boot Settings



Boot Setting Configuration

Press Enter the sub menu for boot setting.

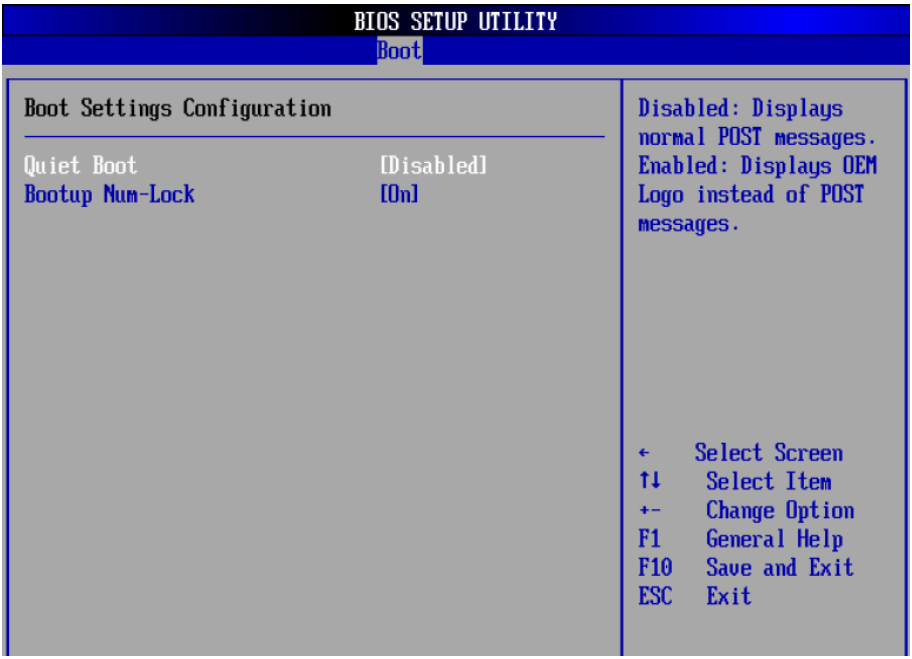
Boot Device Priority

Access to the sub menu for boot device priority.

Hard Disk Drives

Configure the boot settings for the Hard Disk Drives connected to the system.

3.4.1 Boot Settings Configuration



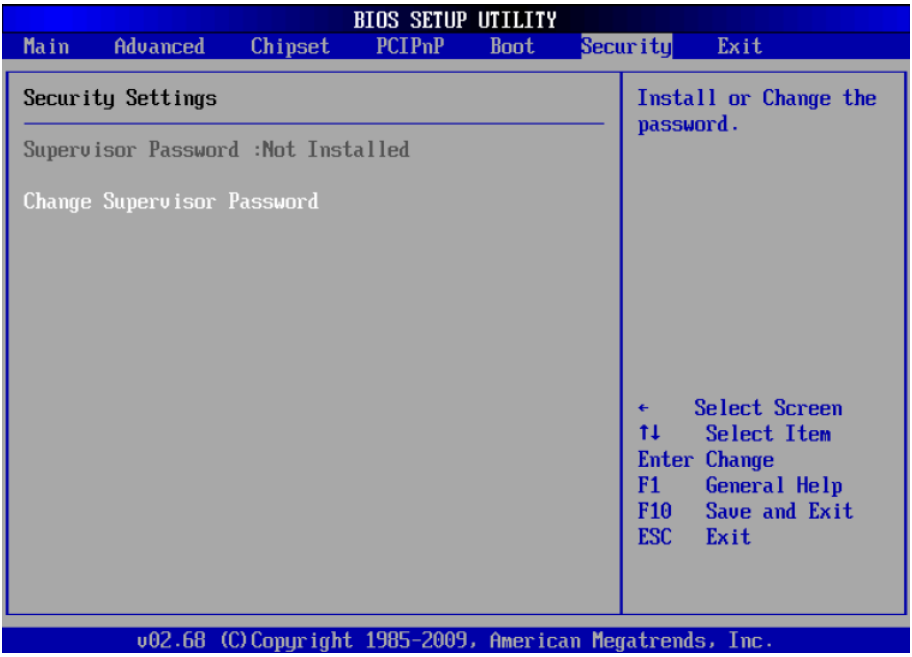
Quiet Boot

Displays normal POST messages when it's selected as "Disabled".
When it is set as "Enabled", OEM messages will be displayed instead of POST messages. The default is "Disabled".

Bootup Num-Lock

Modifies Number Lock setting when the system boots up. Select "On" to automatically enable the Number Lock on keyboard when the system is booting up.

3.5 Security



Supervisor Password & User Password

You can set either supervisor or user password, or both of them. The differences between are:

Set ***Supervisor Password***: Can enter and change the options of the setup menus.

Set ***User Password***: Just can only enter but do not have the right to change the options of the setup menus. When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

ENTER PASSWORD:

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <ESC> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

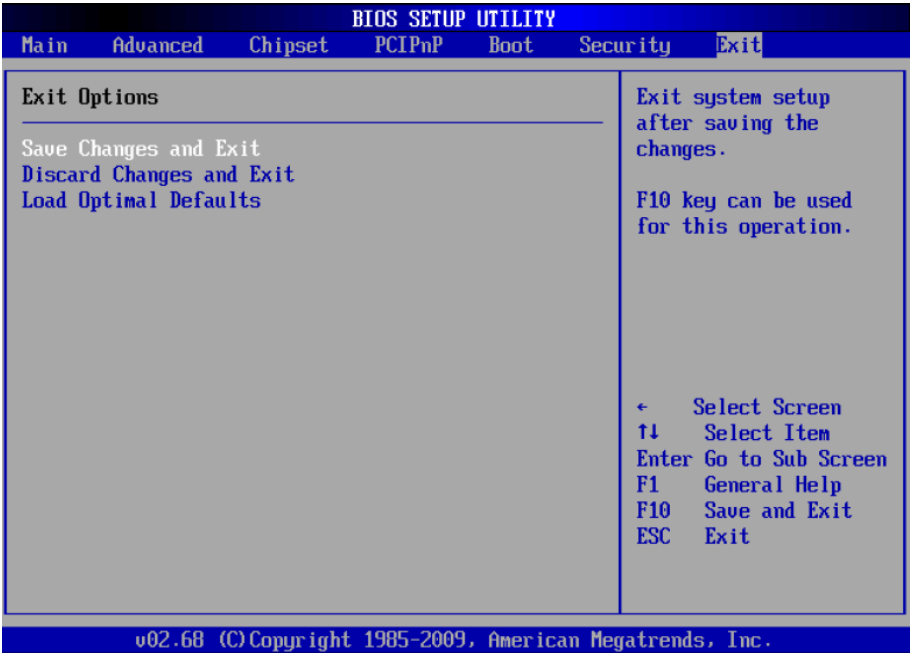
PASSWORD DISABLED.

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You determine when the password is required within the BIOS Features Setup Menu and its Security option. If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If set to “Setup”, prompting only occurs when trying to enter Setup.

3.6 Exit Options



Save Changes and Exit

Pressing <Enter> on this item asks for confirmation:

Save configuration changes and exit setup?

Pressing <OK> stores the selection made in the menus in CMOS - a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

Discard Changes and Exit

Exit system setup without saving any changes.
You can also press <ESC> to activate this function.

Load Optimal Defaults

When you press <Enter> on this option, a message dialog box will appear asking for your confirmation:

Load Optimal Defaults?
[OK] [Cancel]

Press [OK] to load the BIOS Optimal Default values for all the setup options.
You can also press <F9> key to enable this operation.

3.7 Beep Sound codes list

3.7.1 Boot Block Beep codes

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

3.7.2 POST BIOS Beep codes

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

3.7.3 Troubleshooting POST BIOS Beep codes

Number of Beeps	Description
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

3.8 AMI BIOS Checkpoints

3.8.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS *(Note)*:

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processo (BSP) initialization like microcode update, frequency and other CPU cirtical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is deisabled. Perfrom keyboard controller BAT test. Save power-on CPUID value in scretch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enabled CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Perfroms main BIOS checksum and updates recovery status accordingly.

D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows tocheckpoint E0. Seed *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether in memory.
D8	The Tuntime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POS (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.
DC	System is saking from ACPI S3 state.
E1 - E8 EC - EE	OEM memory detection / configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to be next.

3.8.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS *(Note)*:

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L2 cache is enabled.
E9	Set up floppy controller and data. Attempt to red from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.

FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

3.8.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS *(Note)*:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system.
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor

C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information. USB controllers are initialized at this point.

39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to theuser and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disalbe NMI as selected.
90	Initialization of system management interrupt by invoking all handlers.
A1	Lian-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.

A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for userinput at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

3.8.4 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system buses. The following table describes the main checkpoints where the DIM module is accessed *(Note)*:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble “X” indicates the function number that is being executed. “X” can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.
3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = On-board System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

3.8.5 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events *(Note)*:

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Entering sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Waking from sleep state S1, S2, S3, S4, or S5.

Note:
Please note that checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Appendix

Apendix A - I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.
The following table lists the I/O port addresses used.

Address	Device Description
00000000-00000CF7	PCI bus
00000000-00000CF7	Direct memory access controller
00000D00-0000FFFF	PCI bus
0000B480-0000B487	Intel(R) Graphics Media Accelerator 3150
000003B0-000003BB	Intel(R) Graphics Media Accelerator 3150
000003C0-000003DF	Intel(R) Graphics Media Accelerator 3150
0000D000-0000DFFF	Intel(R) ICH8 Family PCI Express Root Port 1 - 283F
0000D800-0000D8FF	Realtek PCIe FE Family Controller
0000E000-0000EFFF	Intel(R) ICH8 Family PCI Express Root Port 2 - 2841
0000E400-0000E407	Standard Dual Channel PCI IDE Controller
0000EC00-0000EC03	Standard Dual Channel PCI IDE Controller
0000E880-0000E887	Standard Dual Channel PCI IDE Controller
0000E800-0000E803	Standard Dual Channel PCI IDE Controller
0000E480-0000E48F	Standard Dual Channel PCI IDE Controller
0000B880-0000B89F	Intel(R) ICH8 Family USB Universal Host Controller - 2830
0000B800-0000B81F	Intel(R) ICH8 Family USB Universal Host Controller - 2831
0000C800-0000C8FF	Realtek RTL8169/8110 Family Gigabit Ethernet NIC #2
00000A79-00000A79	ISAPNP Read Data Port
00000279-00000279	ISAPNP Read Data Port
00000274-00000277	ISAPNP Read Data Port
00000020-00000021	Programmable interrupt controller
000000A0-000000A1	Programmable interrupt controller

00000081-00000083	Direct memory access controller
00000087-00000087	Direct memory access controller
00000089-0000008B	Direct memory access controller
0000008F-0000008F	Direct memory access controller
000000C0-000000DF	Direct memory access controller
00000040-00000043	System timer
00000070-00000071	System CMOS/real time clock
00000061-00000061	System speaker
000000F0-000000FF	Numeric data processor
000003F8-000003FF	Communications Port (COM1)
000002F8-000002FF	Communications Port (COM2)
00000378-0000037F	Printer Port (LPT1)
00000A00-00000A0F	Motherboard resources
000003E8-000003EF	Communications Port (COM3)
000002E8-000002EF	Communications Port (COM4)
00000370-00000371	Motherboard resources
00000010-0000001F	Motherboard resources
00000022-0000003F	Motherboard resources
00000044-0000005F	Motherboard resources
00000062-00000063	Motherboard resources
00000065-0000006F	Motherboard resources
00000072-0000007F	Motherboard resources
00000080-00000080	Motherboard resources
00000084-00000086	Motherboard resources
0000008C-0000008E	Motherboard resources
00000090-0000009F	Motherboard resources
000000A2-000000BF	Motherboard resources
000000E0-000000EF	Motherboard resources
000004D0-000004D1	Motherboard resources
00000800-0000087F	Motherboard resources
00000500-0000053F	Motherboard resources

00000060-00000060	Motherboard resources
00000064-00000064	Motherboard resources
0000FFA0-0000FFAF	Intel(R) ICH8M 3 port Serial ATA Storage Controller - 2828
0000FF90-0000FF9F	Intel(R) ICH8M 3 port Serial ATA Storage Controller - 2828
000001F0-000001F7	Primary IDE Channel
000003F6-000003F6	Primary IDE Channel
00000170-00000177	Secondary IDE Channel
00000376-00000376	Secondary IDE Channel
00000400-0000041F	Intel(R) ICH8 Family SMBus Controller - 283E

Apendix B - Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System Timer
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 5	Intel(R) ICH8 Family SMBus Controller -283E
IRQ 8	System CMOS/real time clock
IRQ 9	Microsoft ACPI-Compliant System
IRQ 10	Communications Port (COM4)
IRQ 11	Communications Port (COM3)
IRQ 13	Numeric data processor
IRQ 14	Primary IDE Controller
IRQ 15	Secondary IDE Channel
IRQ 16	Intel(R) Graphics Media Accelerator 3150
IRQ 16	Realtek PCIe FE Family Controller
IRQ 16	Realtek RTL8169/8110 Family Gigabit Ethernet NIC #2
IRQ 17	Standard Dual Channel PCI IDE Controller
IRQ 19	Intel(R) ICH8 Family USB Universal Host Controller - 2831
IRQ 21	Microsoft UAA Bus Driver for High Definition Audio
IRQ 22	Intel(R) ICH8 Family PCI Express Root Port 1 - 283F
IRQ 23	Intel(R) ICH8 Family PCI Express Root Port 2 - 2841
IRQ 23	Intel(R) ICH8 Family USB Universal Host Controller - 2830
IRQ 23	Intel(R) ICH8 Family USB2 Enhanced Host Controller - 2836

Apendix C - Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitoring the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. Then, WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming. Below are the source codes written in assembly & C, please take them for WDT application examples.

Assembly Code

```
;-- Initial W83627 --
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 87h
        out     DX, AX          ;
        out     DX, AX          ; initial W83627 start
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 2Bh
        out     DX, AL          ; Select CR2B
        mov     AL, 00h
        inc     DX
        out     DX, AL          ; Set CR2B bit 4=0, PIN89=WDTO
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 07h
        out     DX, AL          ; Point to Logical Device Selector
        mov     AL, 08h
        inc     DX
        out     DX, AL          ; Select Logical Device 8
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 30h
        out     DX, AL          ; select CR30
        mov     AL, 01h
        inc     DX
        out     DX, AL          ; update CR30 to 01h
```

```
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 0F0h
        out     DX, AL          ; select CRF0
        mov     AL, 00h
        inc     DX
        out     DX, AL          ; set CRF0=00h, output
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 0F5h
        out     DX, AL          ; select CRF5, WDT Timer unit
        mov     AL, 00h         ; bit2 =0 ->second ; bit2 =1 -> minute
        inc     DX
        out     DX, AL          ; update CRF5 bit2 to 00h
;--
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, 0F6h
        out     DX, AL          ; select CRF6, WDT Timer
        mov     AL, 05h
        inc     DX
        out     DX, AL          ; update CRF6 to 5 unit
;---
        mov     AX, 2Eh
        mov     DX, AX
        mov     AL, AAh
        out     DX, AX
;-- end
```

C language Code

```
/*-----     Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

/*-----     routing, sub-routing -----*/

void main()

{
          outportb(0x2e, 0x87);       /* initial IO port twice */
          outportb(0x2e, 0x87);

          outportb(0x2e, 0x2B);       /* select CR2B */
          outportb(0x2e+1, 0x00);     /* update CR2B bit4 to 00h */
                                      /* Set PIN89 as WDTO */

          outportb(0x2e, 0x07);       /* point to logical device selector */
          outportb(0x2e+1, 0x08);     /* select logical device 8 */
          outportb(0x2e, 0x30);       /* select CR30 */
          outportb(0x2e+1, 0x01);     /* update CR30 to 01h */
          outportb(0x2e, 0xf0);       /* select CRF0 */
          outportb(0x2e+1, 0x00);     /* update CRF0 to 00h */
          outportb(0x2e, 0xf5);       /* select CRF5 to set timer unit */
          outportb(0x2e+1, 0x00);     /* update CRF5 bit2, 0:sec; 1:Min. */
          outportb(0x2e, 0xF6);       /* select CRF6 */
          outportb(0x2e+1, 0x05);     /* update CRF6 to 05h (5 sec) */

          outportb(0x2e, 0xAA);       /* stop program W83627, Exit */
}
```

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