EmCORE-i77M3

3.5” Compact Board

User’s Manual

Version 1.2

2014.05

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Revision History

Version	Release Time	Description
1.0	September 2013	Initial release
1.1	March 2014	P.3 Spec 4GB-->8GB P.6 Change Dimension P.8 Change Jumper Board Top P.10,11 Correct JPWR1 & JBAT1 location P.19 Revise USB 2,3 P.21 Revise COM2
1.2	May 2014	P.10 Change JPWR1 Jumper default to ATX mode

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Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

Warning

This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

Replacing Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor.com.tw

E-mail:info@arbor.com.tw

Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

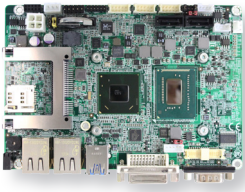
Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

Chapter 1

Introduction

1.1. The Product



The EmCORE-i77M3 is a 3.5” compact CPU board loaded with Intel® Core™ i7-3517UE processor, Intel® PCH QM77 chipset and Intel® Graphics Media Accelerator 4000. The board is provided with two serial ports with RS232/RS422/RS485 supports, six USB ports, two serial ATA port and one CFast socket for storage, and one DVI-I port for video output. The board supports dual independent display to answer the market need for video performance.

1.2. About this Manual

This manual is intended for experienced users and integrators with hardware knowledge of computers. If you are not sure about the description in this manual, consult your vendor before further handling.

We recommend that you keep one copy of this manual for the quick reference for any necessary maintenance in the future. Thank you for choosing ARBOR products.

1.3. Specifications

Form Factor	3.5" Compact Board	
CPU	Soldered onboard Intel® Core™ i7-3517UE 1.7 GHz processor	
Chipset	Intel® PCH QM77	
System Memory	1 x 204-pin SO-DIMM socket, supporting up to 8GB 1333/1600MT/s DDR3 SDRAM	
Graphics Chipset	Integrated Intel® HD Graphics 4000	
Graphics Interface	DVI-I:	Analog RBG support up to 2048 x 1536 @60Hz or TMDS support up to 1920 x 1200 via Chrontel CH7318
	LCD:	Dual-channel 24-bit LVDS
	Dual independent displays support	
Ethernet	1 x Intel® 82579LM PCIe GbE PHY with iAMT support	
	1 x Intel® 82583V PCIe GbE controller	
Super IO Chipset	Fintek F71869ED	
BIOS	AMI® PnP Flash BIOS	
Audio	Realtek ALC662 HD Audio CODEC, MIC-in/ Line-out/Line-in	
Storage	2 x Serial ATA ports with 600MB/s HDD transfer rate	
	1 x CFast socket	
Serial Port	2 x COM ports (1 x RS-232 port, 1 x RS-232/422/485 port selectable)	
Universal Serial Bus	4 x USB 2.0 ports	
	2 x USB 3.0 ports	
Expansion Bus	1 x Mini-card socket	
	1 x micro SIM socket	
Power Requirement	+12V DC	
Power Consumption	3A@+12V (typical)	
Operation Temp.	-20°C ~ 70°C (-4°F ~ 158°F)	
Operating Humidity	10% ~ 95% @ 70°C (non-condensing)	
Watchdog Timer	1~255 levels reset	
Dimension (L x W)	146 x 102 mm (5.7” x 4.0”)	

1.4. Inside the Package

Before starting to install the single board, make sure the following items are shipped:

	1 x EmCORE-i77M3 3.5" Compact Board with cooler
	1 x Driver CD
	1 x Quick Installation Guide

If any of the aforelisted items is damaged or missing, contact your vendor immediately.

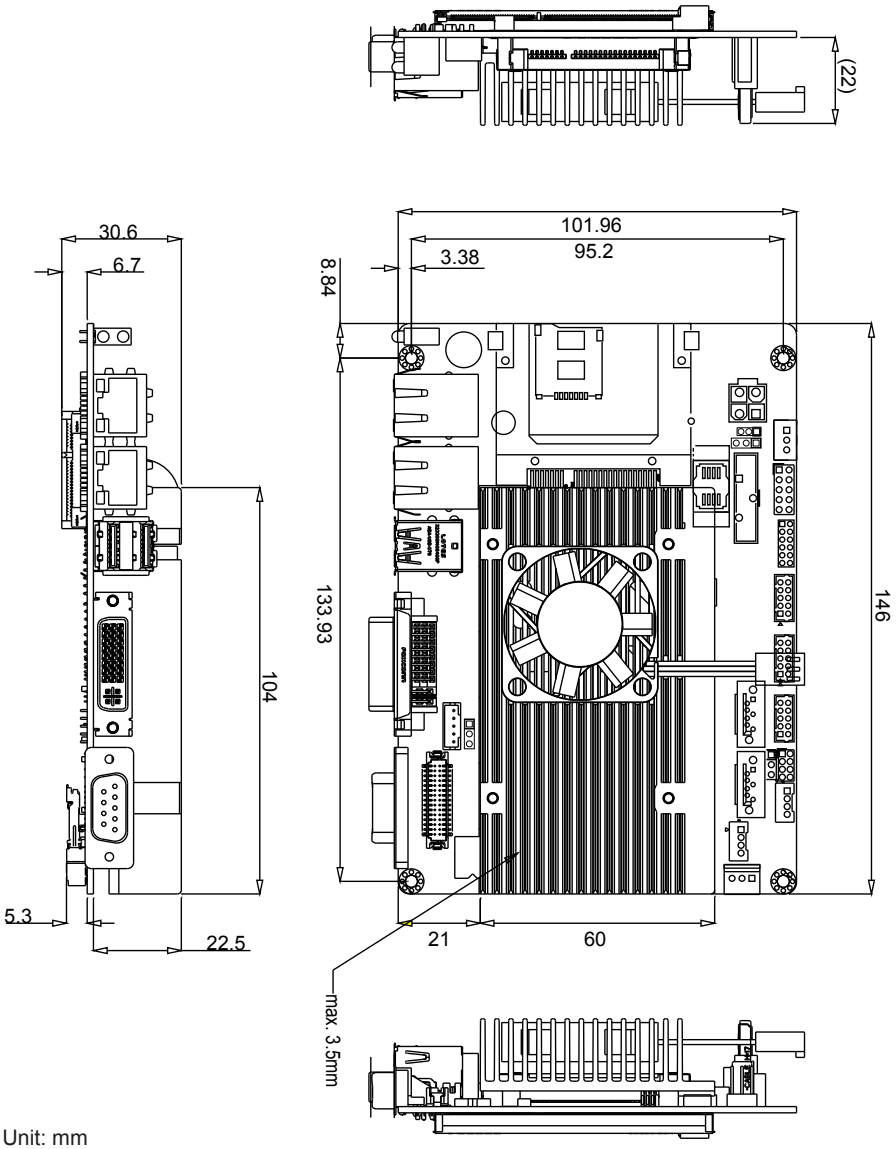
1.5. Ordering Information

EmCORE-i77M3	3.5" Intel® Core™ i7-3517UE Compact Board
CBK-06-77M3-00	Cable Kit 1 x SATA cable 1 x SATA power cable 2 x USB dual port cables 1 x Audio cable 1 x COM port cable

Chapter 2

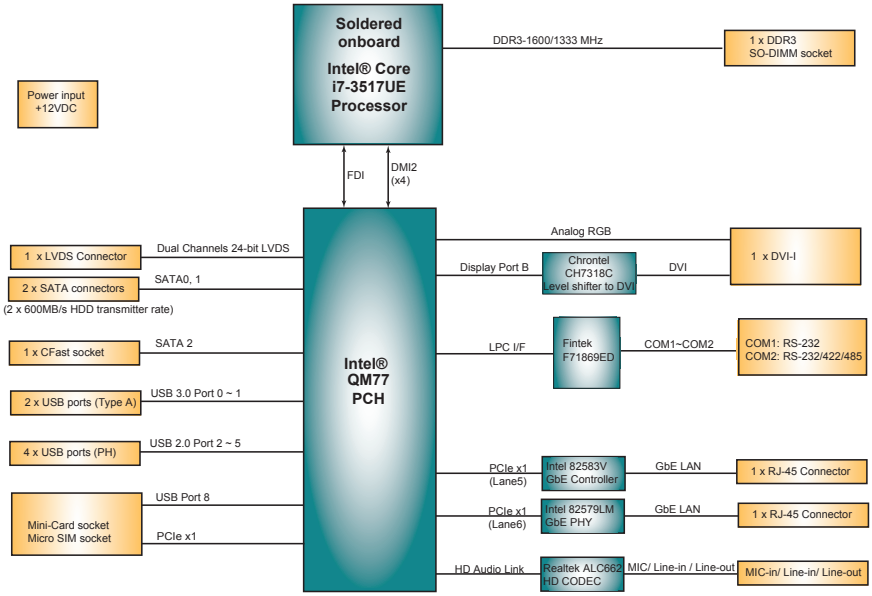
Getting Started

2.1. Board Dimensions



Unit: mm

2.2. Block Diagram



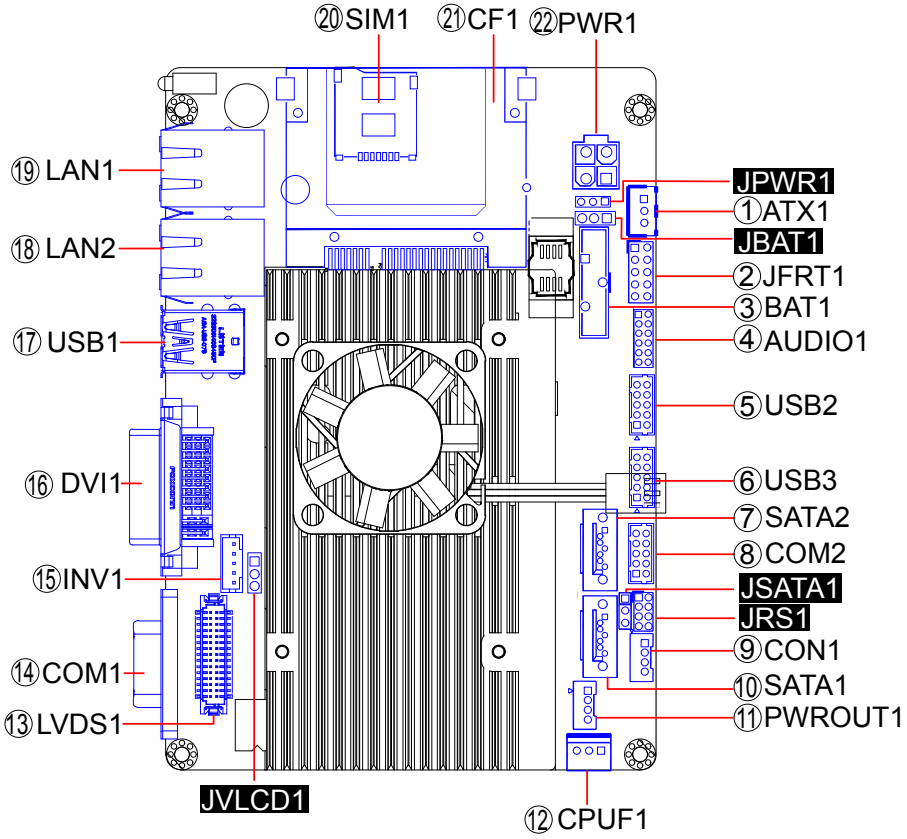
2.3. Jumpers & Connectors

The board comes with some connectors to join some devices and also some jumpers to alter the hardware configuration. The following in this chapter will explicate each of these components one-by-one.

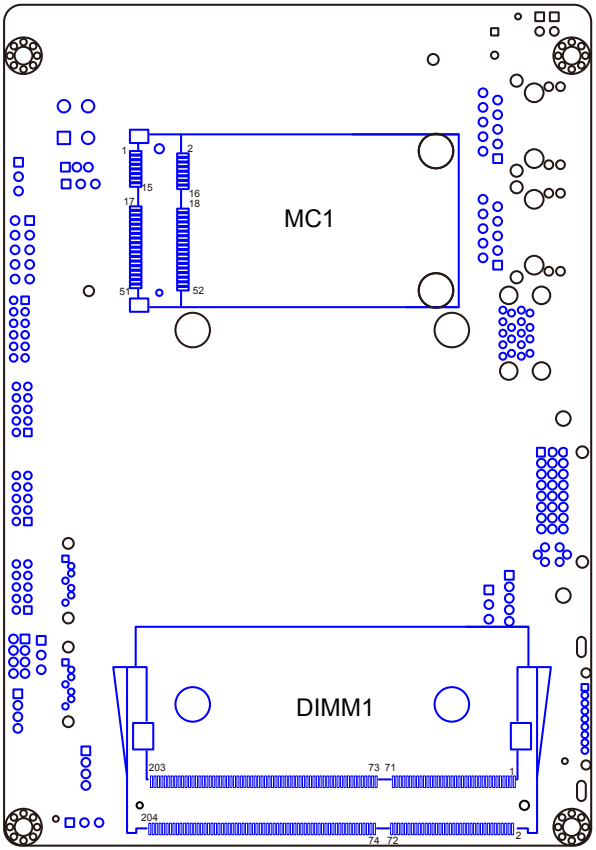
2.3.1. Layout

This section will provide an overview of this board, both the top and bottom sides.

Board Top



Board Bottom



2.3.2. Jumpers

JPWR1

Function: Sets the power mode between AT and ATX

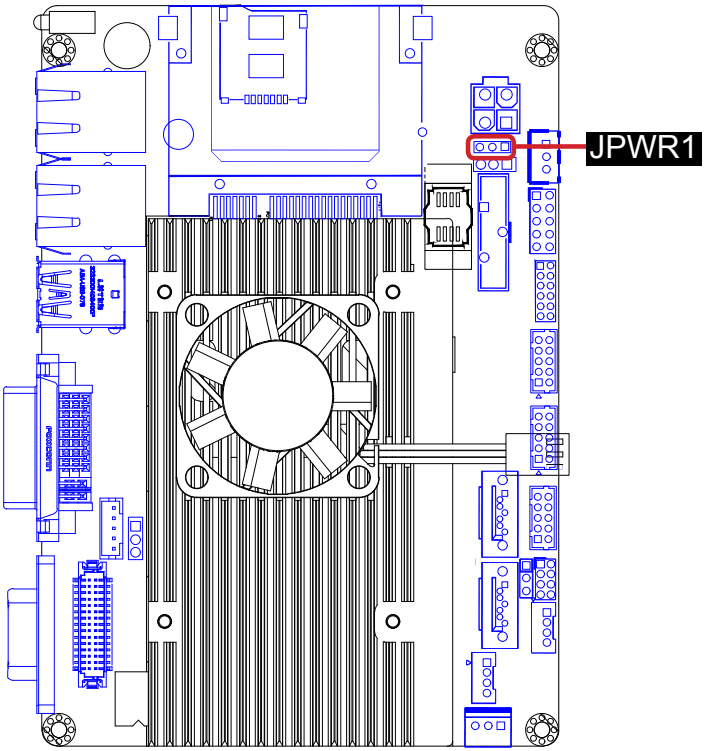
Jumper Type: 2.00 mm pitch 1x3-pin header

Setting:

Pin	Description	
1-2	ATX mode (default)	
2-3	AT mode	

Note to make consistent setting in **BIOS** | **Advanced** menu | **ACPI Settings** | **Power-Supply Type** to avoid possible conflict. See 3.2.1. ACPI Settings on page 43.

Board Top



JBAT1

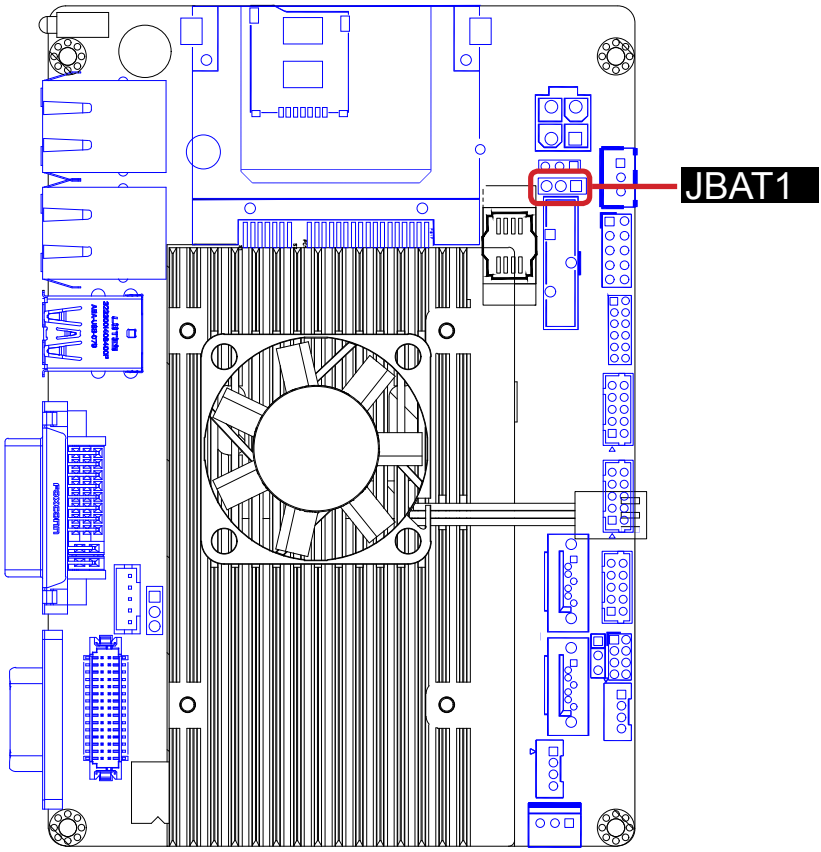
Function: Clears/keeps CMOS

Jumper Type: 2.54 mm pitch 1x3-pin header

Setting:

Pin	Description	
1-2	Keeps CMOS (default)	
2-3	Clears CMOS	

Board Top



JSATA1

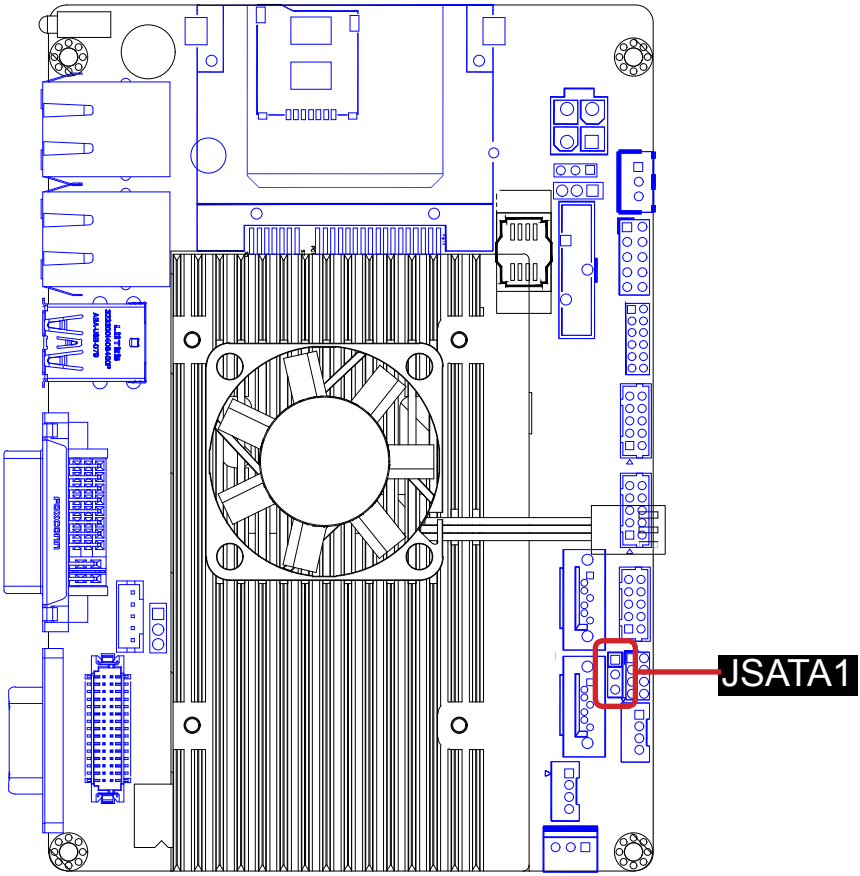
Function: Sets the power for SATA1 pin 7

Jumper Type: 2.54 mm pitch 1x3-pin header

Setting:

Pin	Description	
1-2	+5V	
2-3	GND (default)	

Board Top



JRS1

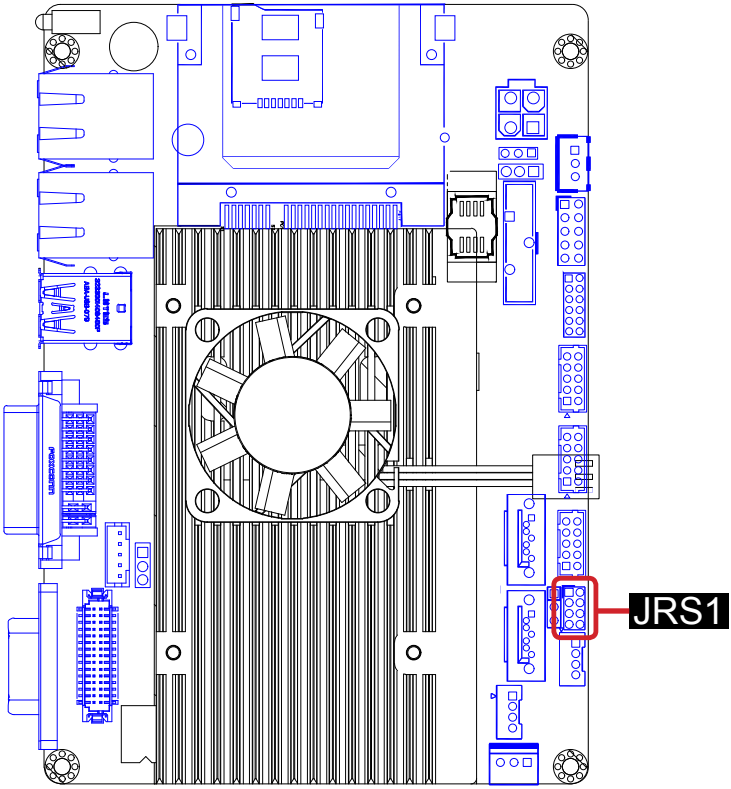
Function: Enables/disables COM2 to/from RS485 auto-flow

Jumper Type: 2.00 mm pitch 2x4-pin header

Setting:

Signal / Pin	RS232 (default)	RS422	RS485	
			Auto-flow Disabled	Auto-flow Enabled
1-2	Short	Open	Open	Open
3-4	Open	Short	Open	Open
5-6	Open	Open	Short	Short
7-8	Short	Open	Short	Open
				

Board Top

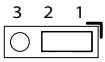
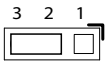


JVLCD1

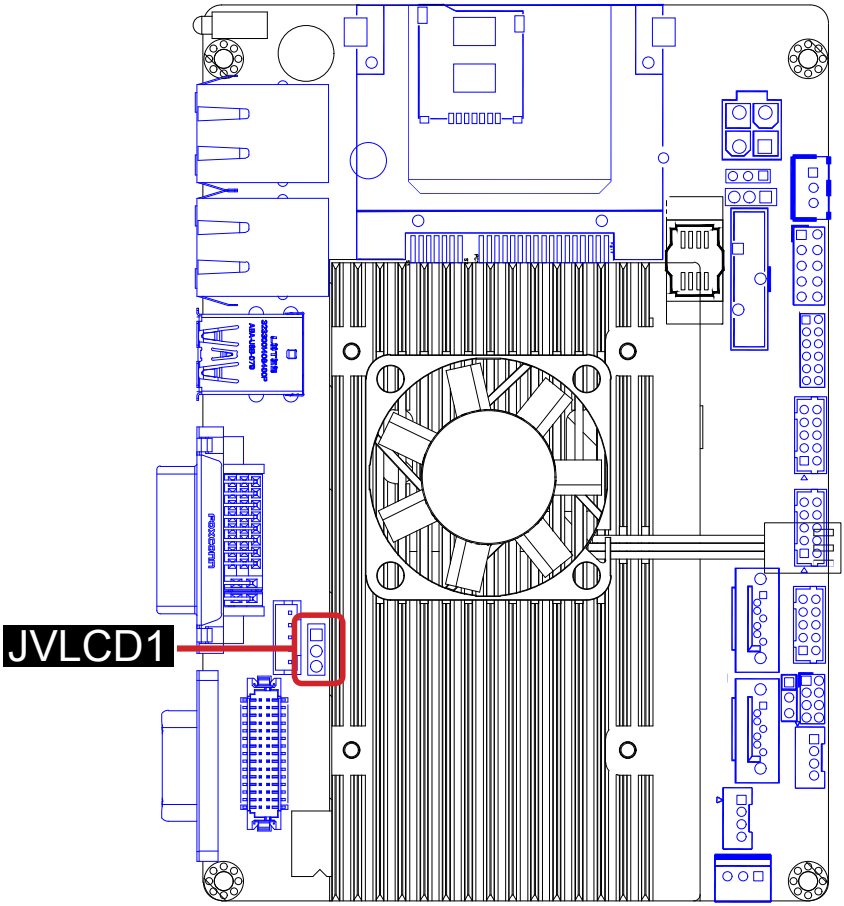
Function: Sets the power voltage for LVDS1 LCD.

Jumper Type: 2.54mm pitch 1x3-pin header

Setting:

Pin	Description	
1-2	+5V	
2-3	+3.3V (default)	

Board Top



2.3.3. Connectors

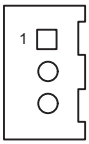
ATX1

Function: Connector for ATX feature

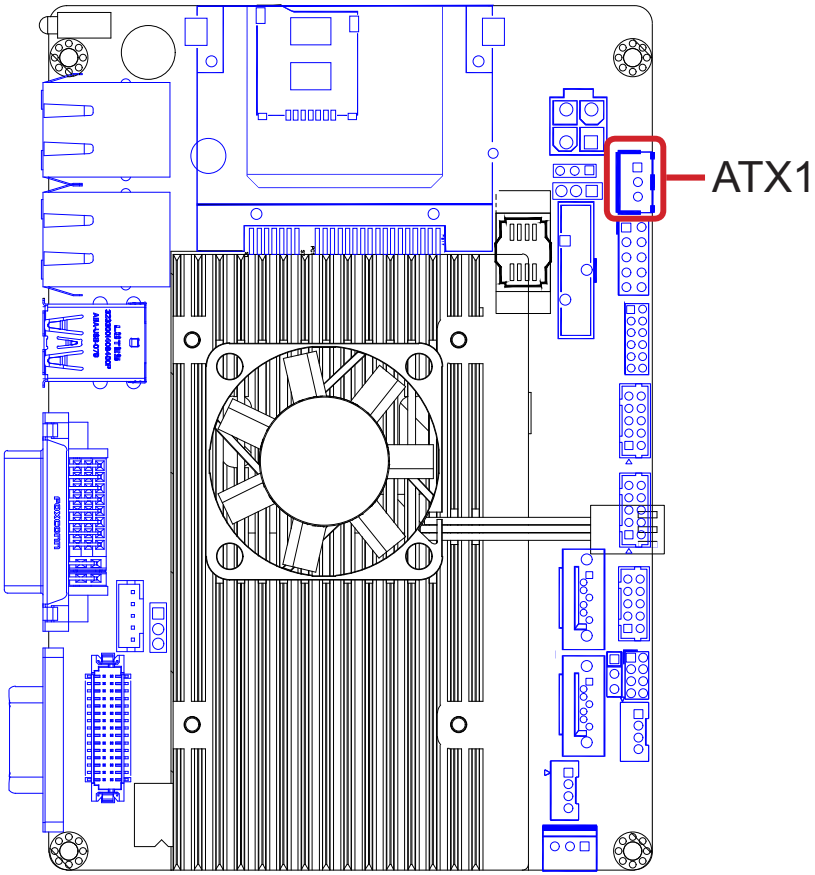
Connector Type: 2.54 mm pitch 1x3-pin box wafer connector

Pin Assignment:

Pin	Description
1	PS-ON
2	GND
3	5V_SB



Board Top



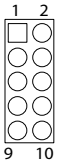
JFRT1

Function: Provides connectors to front-panel status LED and toggles.

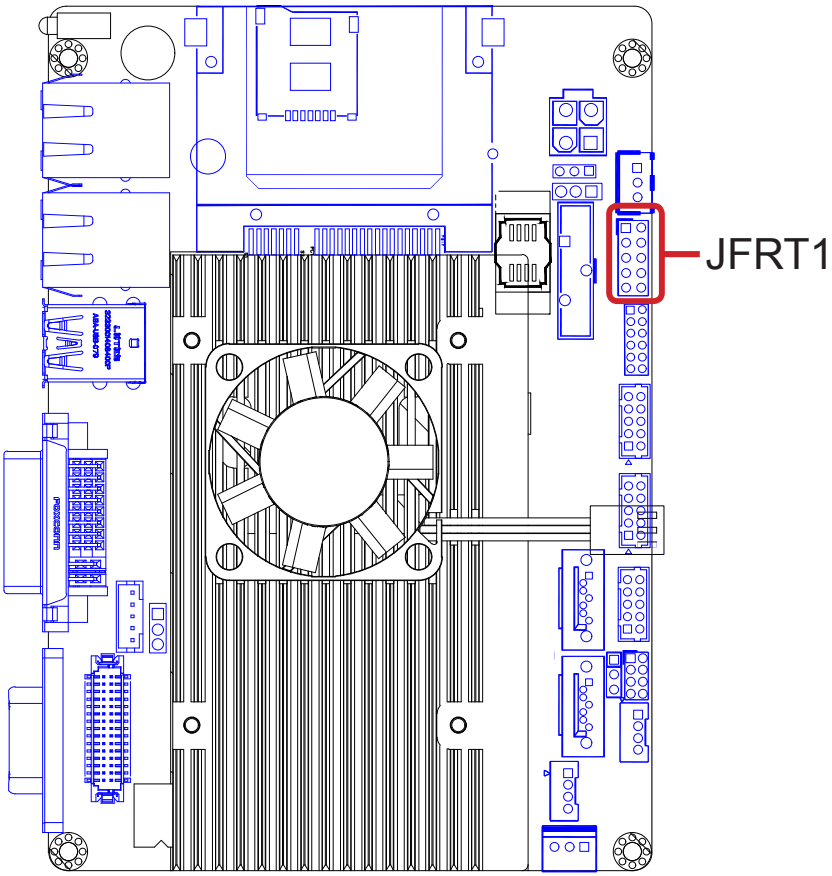
Connector Type: 2.54mm pitch 2x5-pin header

Pin Assignment:

Pin	Description	Pin	Description
1	RESET+	2	RESET-
3	PLED+	4	PLED-
5	HLED+	6	HLED-
7	SPEAK+	8	SPEAK-
9	PSON+	10	PSON-



Board Top



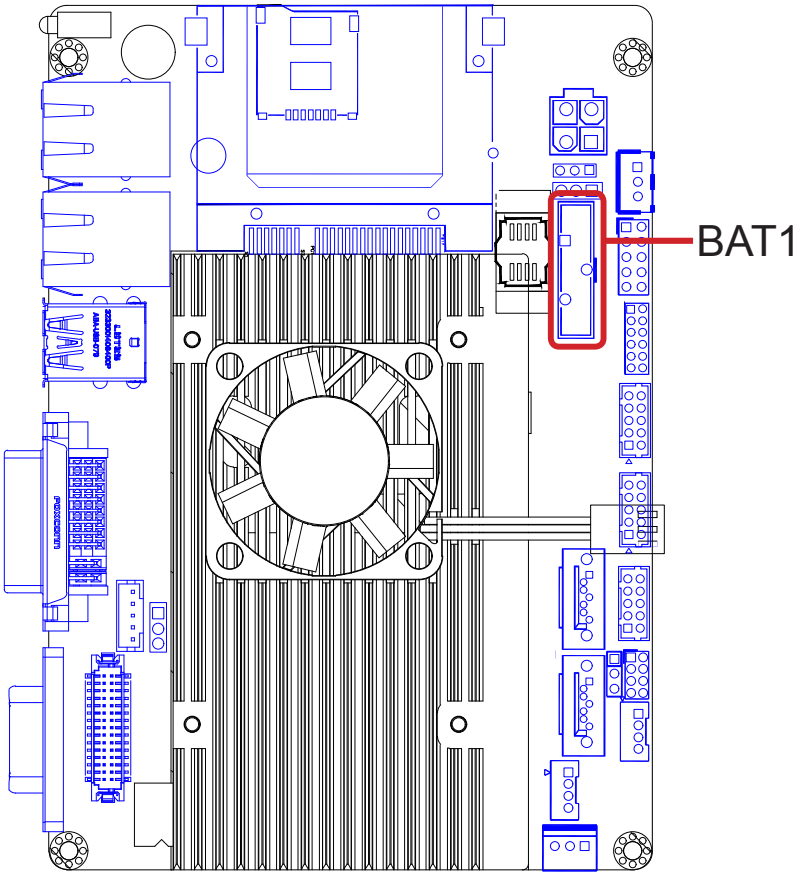
BAT1

Function: RTC battery holder

Pin Assignment:

Pin	Description
1	Battery power
2	GND
3	Battery power

Board Top



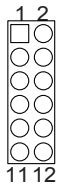
AUDIO1

Function: Audio connector

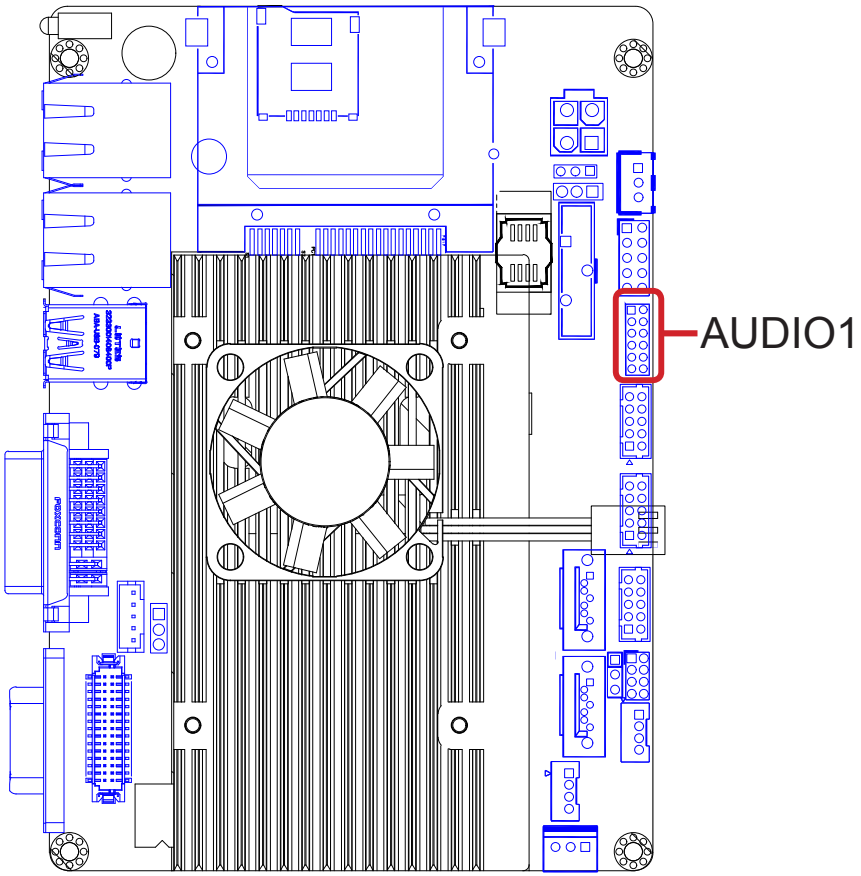
Connector Type: 2.00mm pitch 2x6-pin header

Pin Assignment:

Pin	Description	Pin	Description
1	LINE-L	2	LINE-R
3	LINE_JD	4	AGND
5	MIC1L	6	MIC1R
7	MIC1_JD	8	AGND
9	LOUT-L	10	LOUT-R
11	LOUT-JD	12	AGND



Board Top



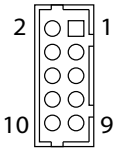
USB2,3

Function: USB port connectors

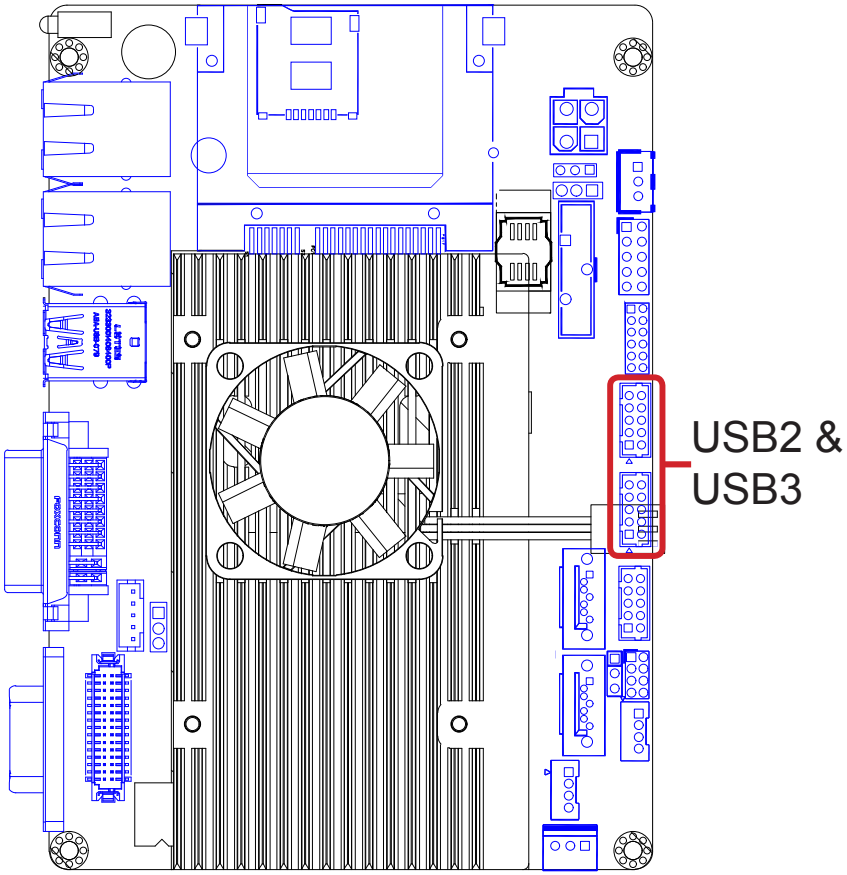
Connector Type: 2.00mm pitch 2x5-pin wafer connector

Pin Assignment:

Pin	Description	Pin	Description
2	+5V	1	+5V
4	USB3/5-	3	USB2/4-
6	USB3/5+	5	USB2/4+
8	GND	7	GND
10	N/C	9	N/C



Board Top



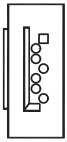
SATA1,2

Function: Serial ATA connectors

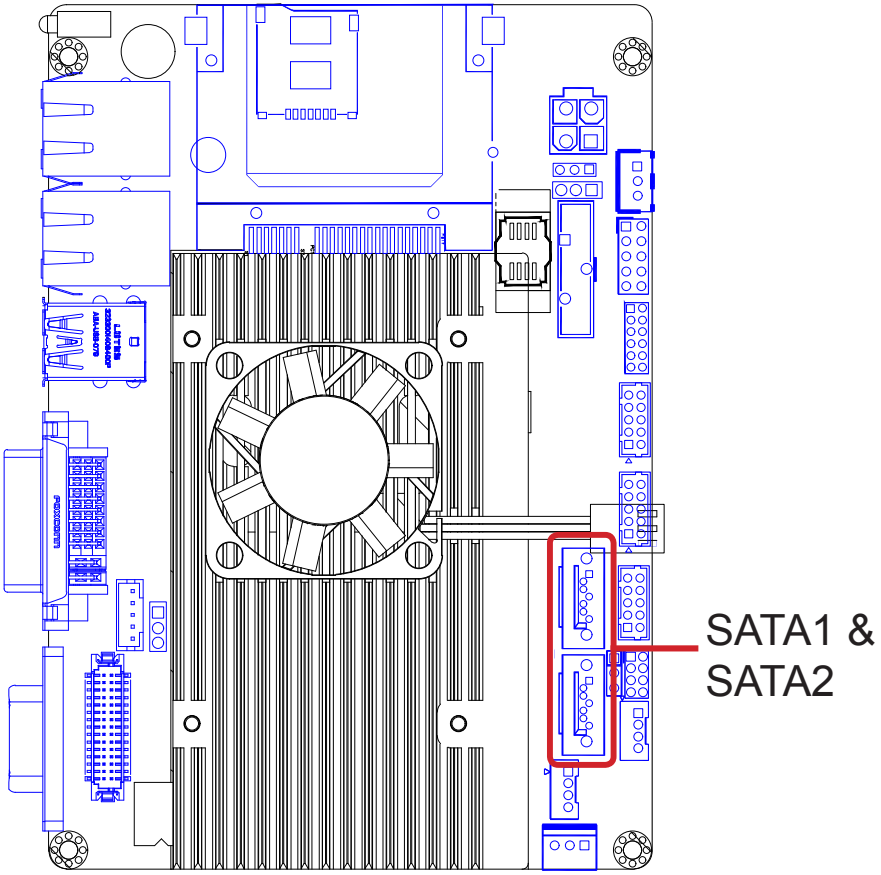
High speed transfer rates (600MB/s).
* Pin 7 can be set to +5V by JSATA1.

Pin Assignment:

Pin	Description	Pin	Description
1	GND	2	TX+
3	TX-	4	GND
5	RX-	6	RX+
7	GND / +5V (SATA1 only)		



Board Top



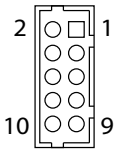
COM2

Function: Serial port connector

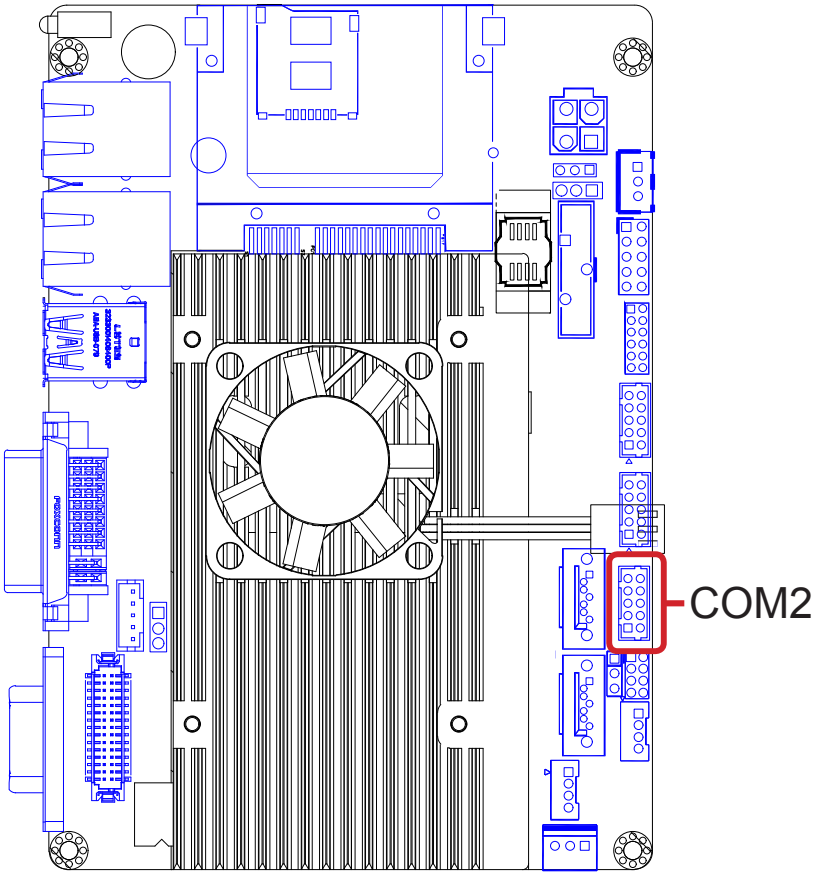
Connector Type: 2.00mm pitch 2x5-pin wafer connector

Pin Assignment:

Pin	Description	Pin	Description
2	RXD2	1	DCD#2
4	DTR#2	3	TXD2
6	DSR#2	5	GND
8	CTS#2	7	RTS#2
10	NC	9	RI2



Board Top



CON1

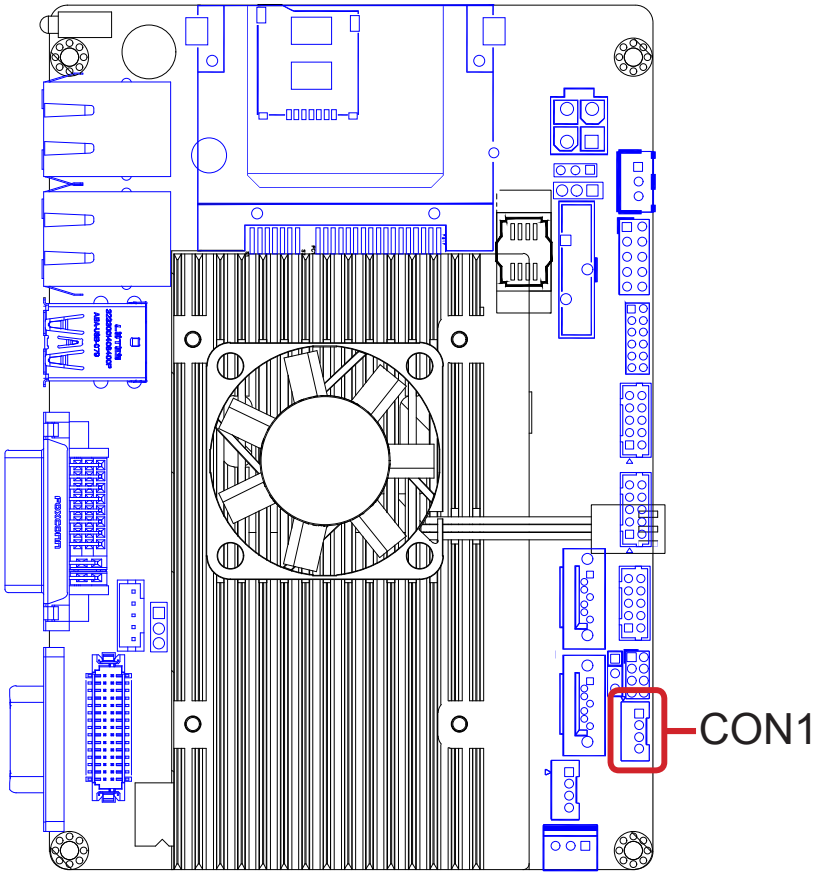
Function: Connector for RS422/485 output

Connector Type: 2.00mm-pitch 1x4-pin box wafer connector

Pin Assignment:

Pin	RS422	RS485
1	422TX+	DATA+
2	422TX-	DATA-
3	422RX+	NC
4	422RX-	NC

Board Top



PWROUT1

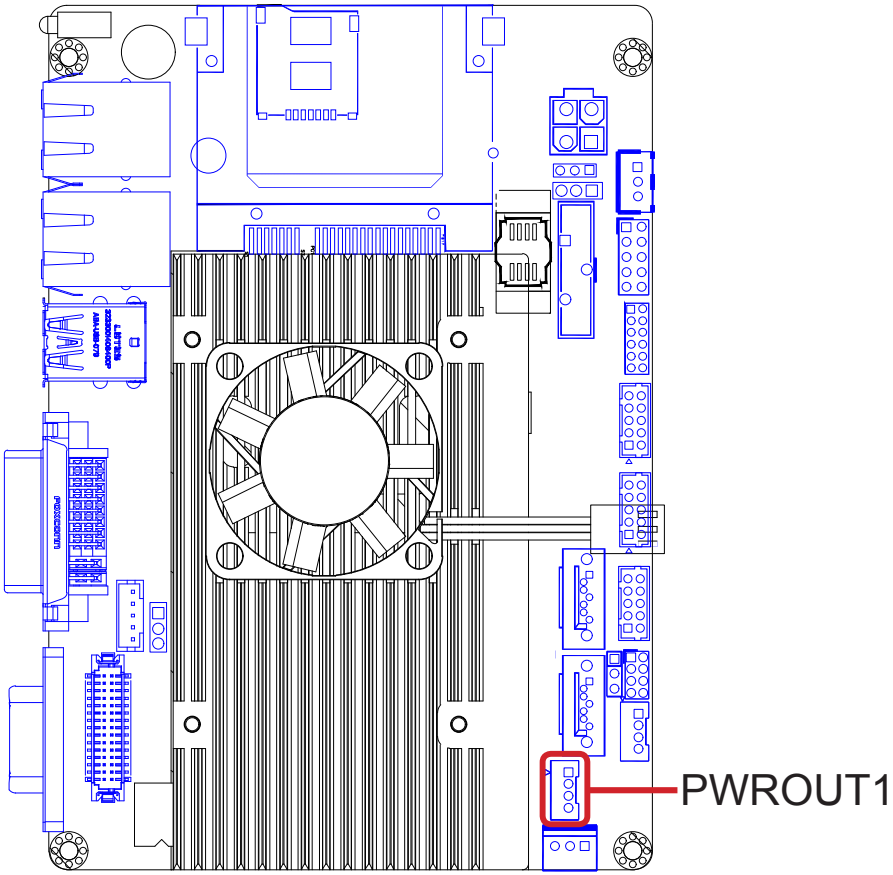
Function: SATA power connector

Connector Type: 2.00mm pitch 1x4-pin wafer connector

Pin Assignment:

Pin	Description
1	5V
2	GND
3	GND
4	12V

Board Top



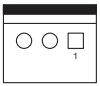
CPUF1

Function: CPU fan power connector

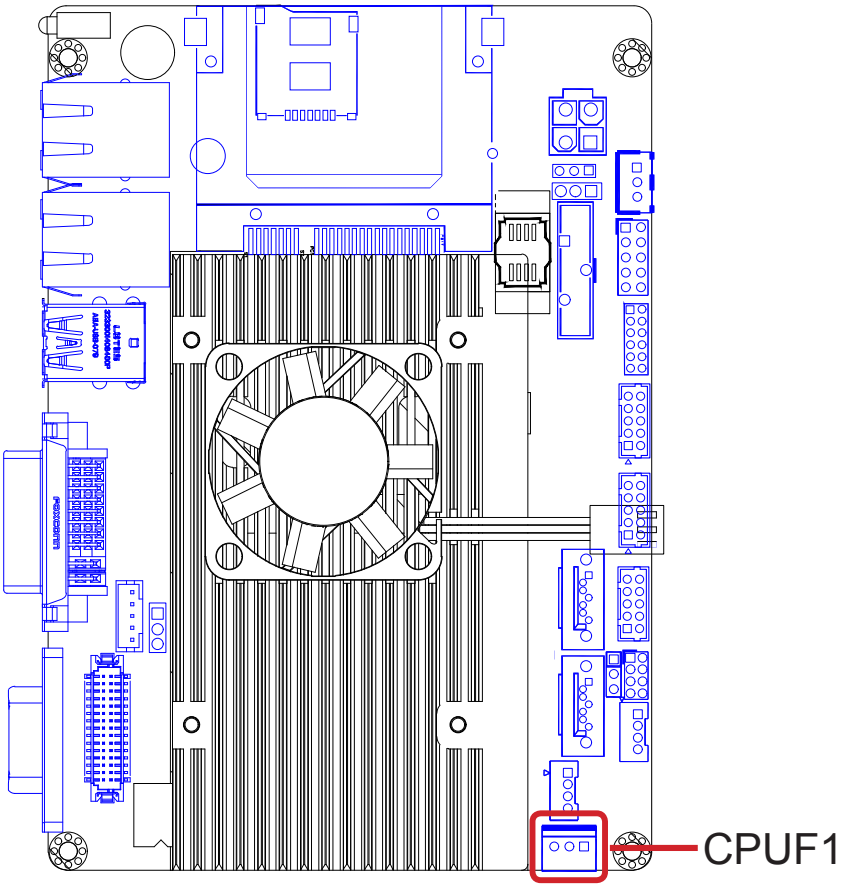
CPUF1 is a 3-pin header for the CPU fan. The fan must be a +12V fan.

Pin Assignment:

Pin	Description
1	GND
2	+12V
3	Fan_Detect



Board Top



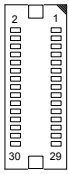
LVDS1

Function: CPU fan power connector

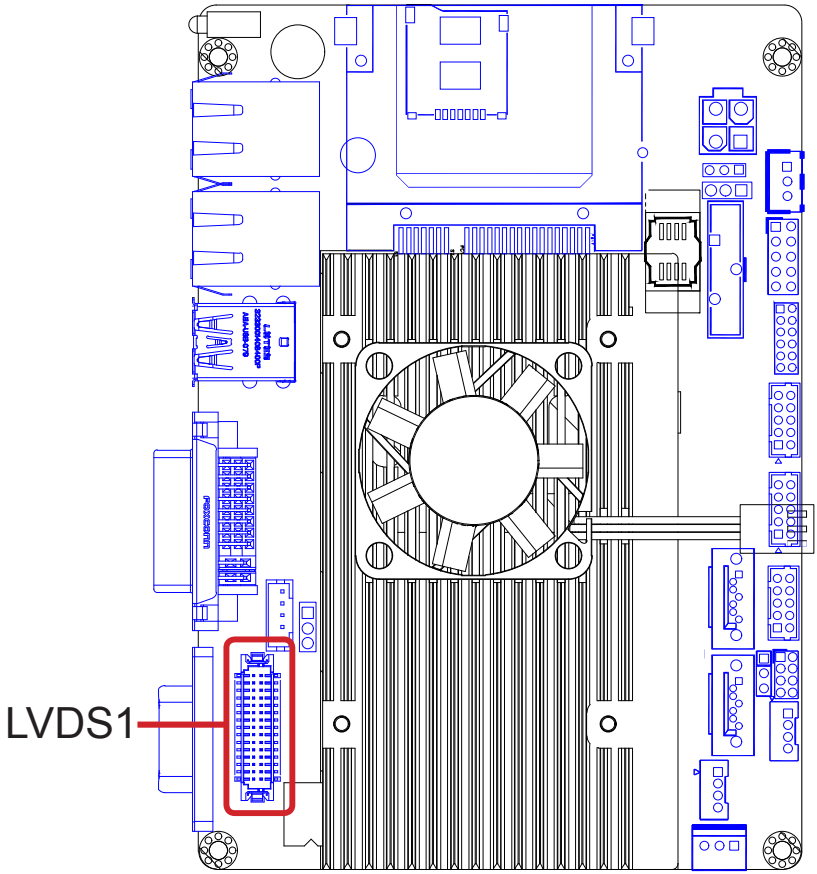
Connector Type: ACES 1.25mm 87209-3040-06 connector that supports 24-bit dual channels.

Pin Assignment:

Pin	Description	Pin	Description	Pin	Description	Pin	Description
2	VDD	1	VDD	18	TX2_D1-	17	TX1_D1-
4	TX2_CLK+	3	TX1_CLK+	20	GND	19	GND
6	TX2_CLK-	5	TX1_CLK-	22	TX2_D2+	21	TX1_D2+
8	GND	7	GND	24	TX2_D2-	23	TX1_D2-
10	TX2_D0+	9	TX1_D0+	26	GND	25	GND
12	TX2_D0-	11	TX1_D0-	28	TX2_D3+	27	TX1_D3+
14	GND	13	GND	30	TX2_D3-	29	TX1_D3-
16	TX2_D1+	15	TX1_D1+				



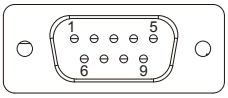
Board Top



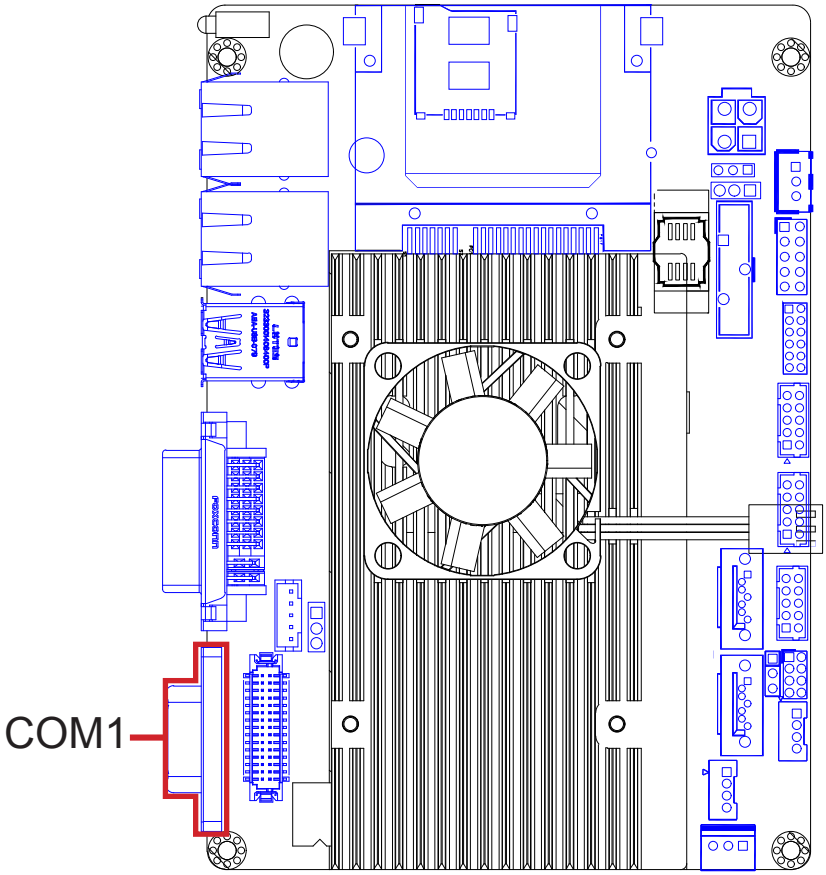
COM1

Function: Serial port

Connector Type: External 9-pin D-sub male connector



Board Top



INV1

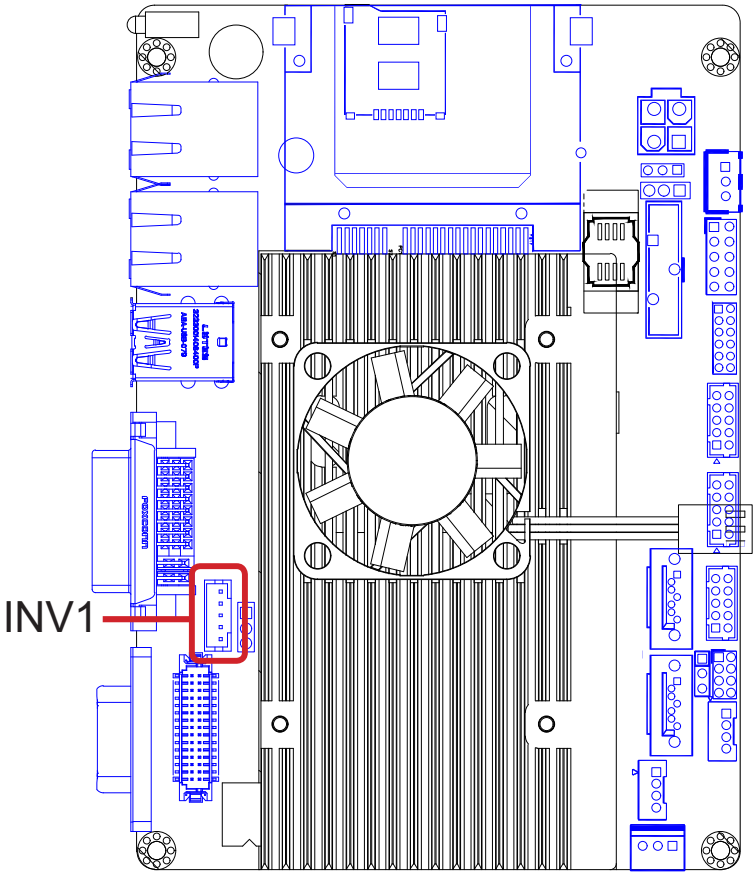
Function: LCD inverter connector

Connector Type: 2.00mm pitch 1x5-pin box wafer connector

Pin Assignment:

Pin	Description
1	+12V
2	GND
3	on/off
4	Brightness control
5	GND

Board Top



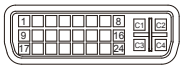
DVI1

Function: DVI-I display connector

Connector Type: 29-pin DIP-type female connector

Pin Assignment:

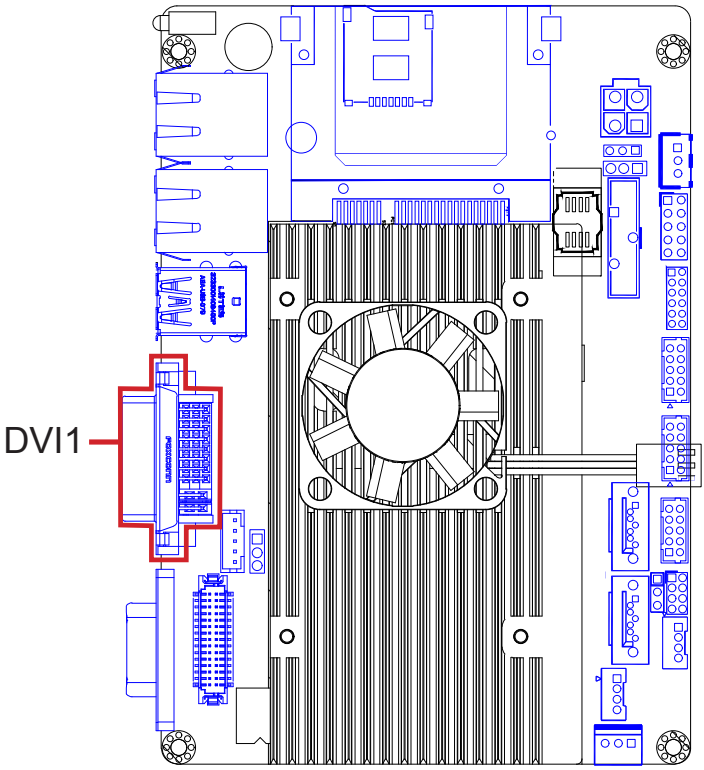
Pin	Description	Pin	Description
1	DATA2-	13	DATA 3+ (LINK 1, NC)
2	DATA2+	14	+5V
3	DATA 2/4 SHIELD	15	GND (for +5V)
4	DATA 4- (LINK 1, NC)	16	Hot Plug Detect
5	DATA 4+ (LINK 1, NC)	17	DATA0-
6	DDC_CLK	18	DATA0+
7	DDC_DATA	19	DATA 0/5 SHIELD
8	VGA_V_Sync	20	DATA 5- (LINK 1, NC)
9	DATA1-	21	DATA 5+ (LINK 1, NC)
10	DATA1+	22	Clock_SHIELD
11	DATA 1/3 SHIELD	23	Clock+
12	DATA 3- (LINK 1, NC)	24	Clock-



Pin	Description
C1	VGA Red
C2	VGA Green
C3	VGA Blue
C4	VGA_H_Sync
C5	VGA_R,G,B_Return

Note: Signals are set to CRT by default.

Board Top



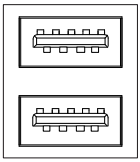
USB1

Function: Double-stacked USB ports

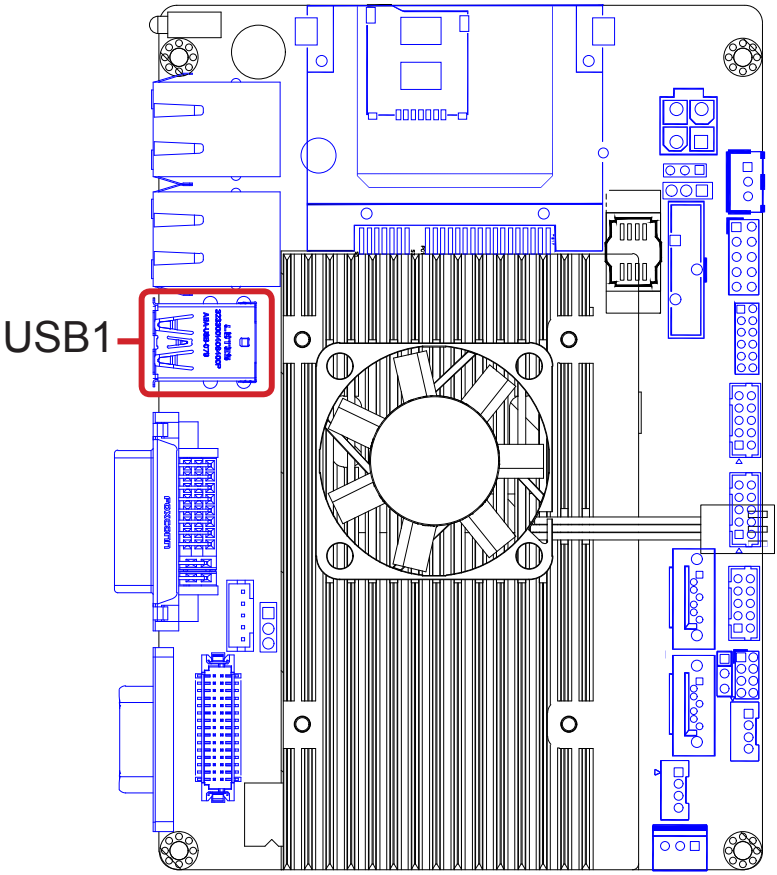
Connector Type: Two SuperSpeed type-A USB 3.0 connectors

Pin Assignment:

Pin	Description	Pin	Description
1	VBUS	2	D-
3	D+	4	GND
5	StdA_SSRX-	6	StdA_SSRX+
7	GND	8	StdA_SSTX-
9	StdA_SSTX+		



Board Top



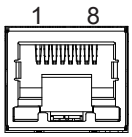
LAN1,2

Function: Gigabit Ethernet ports

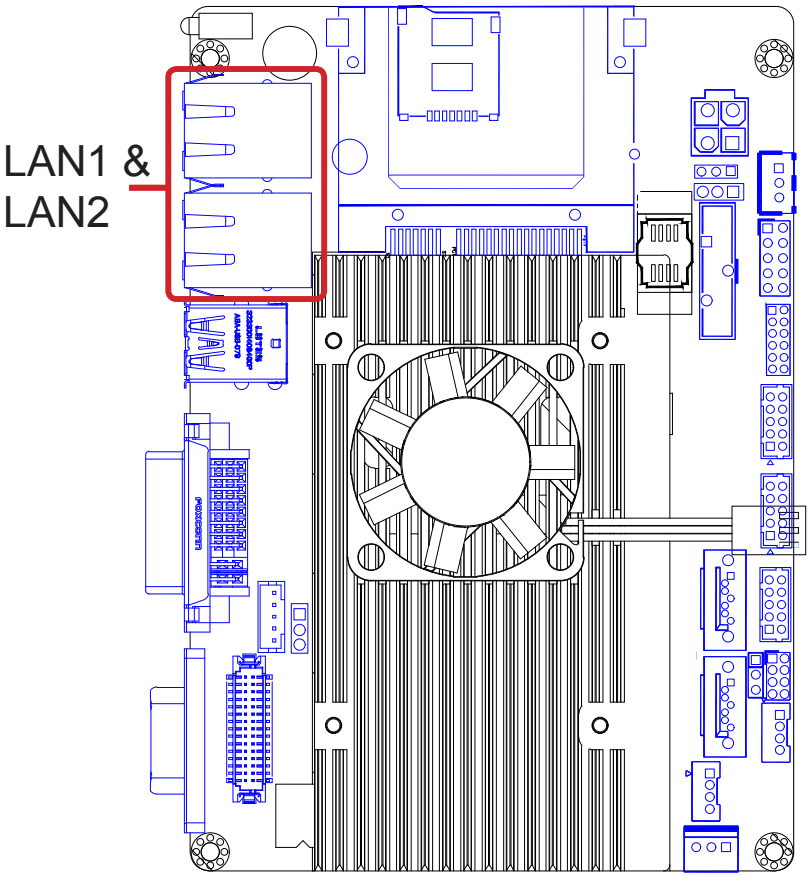
Connector Type: RJ-45 connector that supports 0/100/1000Mbps fast Ethernet

Pin Assignment:

Pin	Description	Pin	Description
1	MDI0	2	MDI0#
3	MDI1	4	MDI1#
5	MDI2	6	MDI2#
7	MDI3	8	MDI3#



Board Top



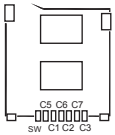
SIM1

Function: Micro SIM card socket

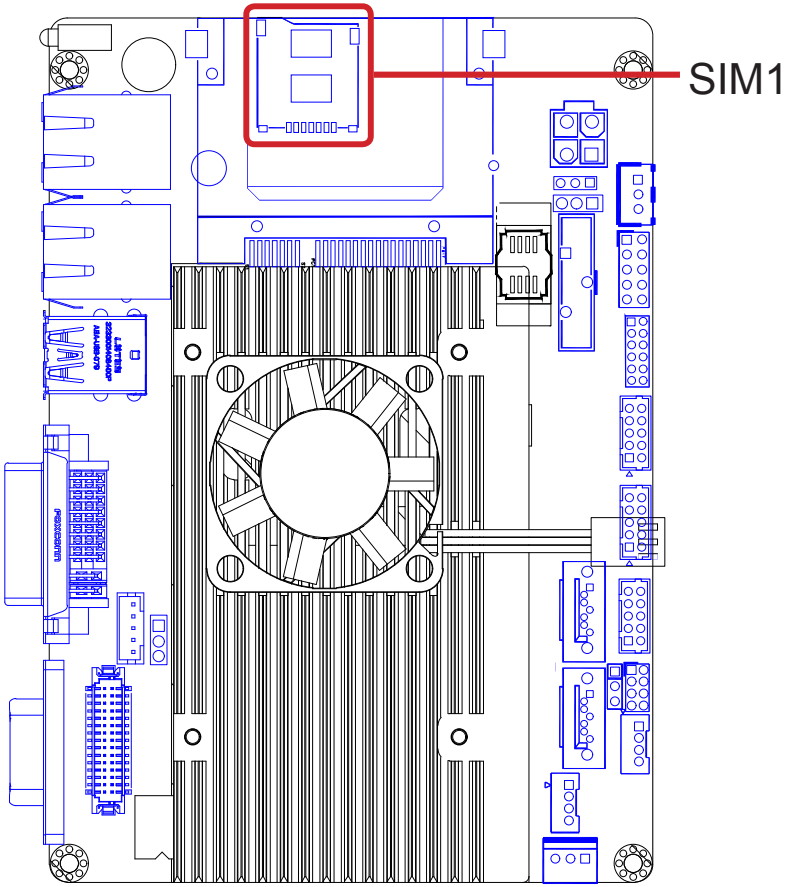
Connector Type: REGO 80440GIH-061T-120L socket

Pin Assignment:

Pin	Description	Pin	Description
C1	VCC	C2	RST
C3	CLK	C5	GND
C6	VPP	C7	I/O



Board Top

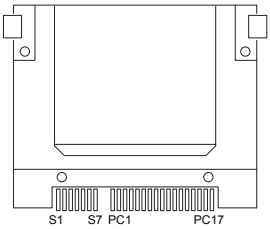


CF1

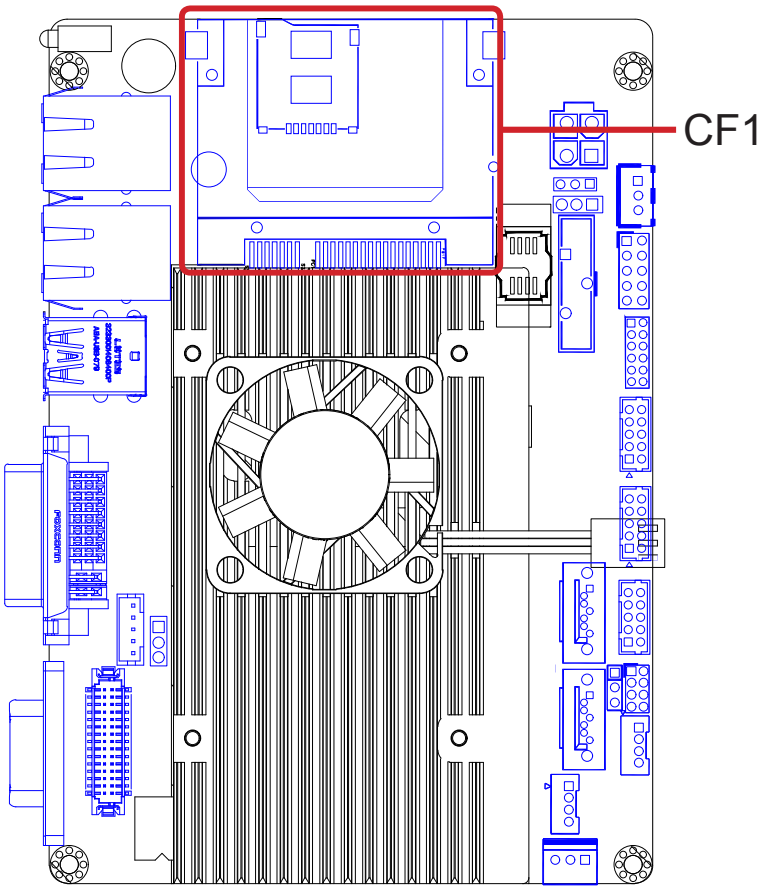
Function: CFast socket

Pin Assignment:

Pin	Desc.	Pin	Desc.	Pin	Desc.
S1	SGND1	**PC2**	GND	**PC10**	IO1
S2	TXP	**PC3**	TBD	**PC11**	IO2
S3	TXN	**PC4**	TBD	**PC12**	IO3
S4	SGND2	**PC5**	TBD	**PC13**	3.3V
S5	RXN	**PC6**	TBD	**PC14**	3.3V
S6	RXP	**PC7**	GND	**PC15**	GND
S7	SGND	**PC8**	LED1	**PC16**	GND
PC1	CDI	**PC9**	LED2	**PC17**	CD0



Board Top



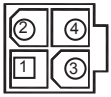
PWR1

Function: Supplies ATX +12V (Vcore)

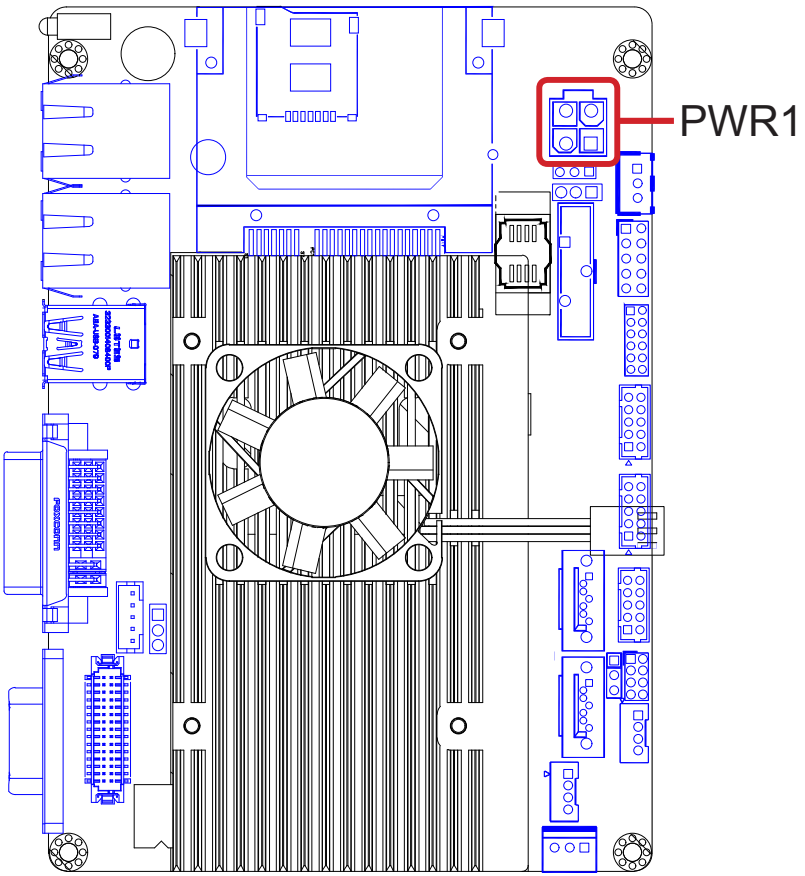
Connector Type: 4-pin power connector

Pin Assignment:

Pin	Description	Pin	Description
2	GND	4	+12V
1	GND	3	+12V



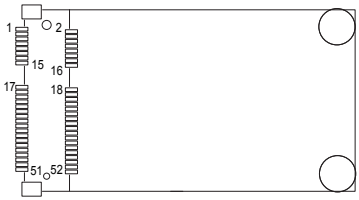
Board Top



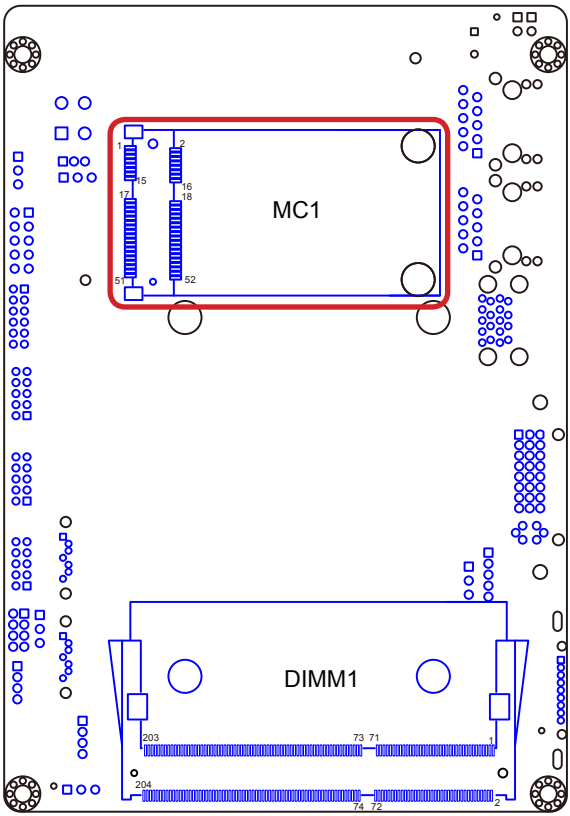
MC1

Function: Mini-card socket

Connector Type: Onboard 0.8mm-pitch 52-pin edge card connector interconnected with SIM card socket



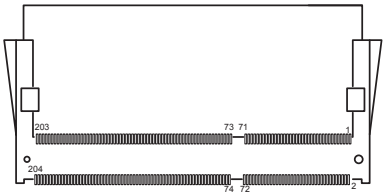
Board Top



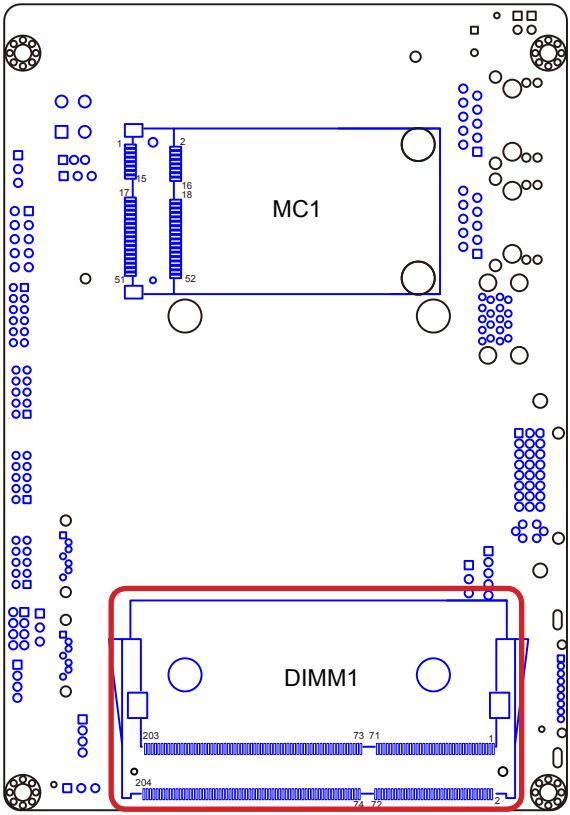
DIMM1

Function: DDR3 SO-DIMM socket

Connector Type: Standard 204-pin DDR3 SODIMM socket



Board Top



2.4. Driver Installation Notes

The board supports Windows XP, Windows 7 and Windows 8. Find the necessary drivers on the CD that comes with your purchase. For different OS, the driver/utility installation may vary slightly, but generally they are similar. **DO** follow the sequence below to install all drivers to prevent errors:

Chipset→.NET Framework→Graphics→Audio→LAN→ME→Intel® Turbo→USB3.0

Find the drivers on CD by the following paths:

Windows XP

Device	Driver Path
Chipset	\EasyBoard-882E\Chipset_INF
VGA	\EasyBoard-882E\Graphic\32\WinXP_32_V6.14.10.5415
	\EasyBoard-882E\Graphic\64\WinXP_64_V6.14.10.5415
LAN	\EasyBoard-882E\Ethernet\32\WinXP
	\EasyBoard-882E\Ethernet\64\WinXP
Audio	\EasyBoard-882E\Audio\WinXP_32_64
Management Engine	\EasyBoard-882E\ME\ME_8.0.20.1513
RAID	\EasyBoard-882E\RAID\WinXP
	\EasyBoard-882E\RAID\32\Intel_RST_F6_floppy_Installer_WinXP_v11.1.0.1006
	\EasyBoard-882E\RAID\64\Intel_RST_F6_floppy_Installer_WinXP_64_v11.1.0.1006
.Net Framwork	\EasyBoard-882E\Framework 3.5

Windows 7

Device	Driver Path
Chipset	\EasyBoard-882E\Chipset_INF
VGA	\EasyBoard-882E\Graphic\32\Win7_Win8_V15.31.3.64.3071
	\EasyBoard-882E\Graphic\64\Win7_Win8_V15.31.3.64.3071
LAN	\EasyBoard-882E\Ethernet\32\Win7_WIN8
	\EasyBoard-882E\Ethernet\64\Win7_Win8
Audio	\EasyBoard-882E\Audio\Win7_Win8\32
	\EasyBoard-882E\Audio\Win7_Win8\64
Management Engine	\EasyBoard-882E\ME\ME_8.0.20.1513
Intel Turbo	\EasyBoard-882E\Turbo Boost
USB3.0	\EasyBoard-882E\USB3.0\Intel(R)_USB_3.0_win7_32_64_Driver_V1.0.5.235

Windows 8

Device	Driver Path
Chipset	\EasyBoard-882E\Chipset_INF
VGA	\EasyBoard-882E\Graphic\32\Win7_Win8_V15.31.3.64.3071
	\EasyBoard-882E\Graphic\64\Win7_Win8_V15.31.3.64.3071
LAN	\EasyBoard-882E\Ethernet\32\Win7_WIN8
	\EasyBoard-882E\Ethernet\64\Win7_Win8
Audio	\EasyBoard-882E\Audio\Win7_Win8\32
	\EasyBoard-882E\Audio\Win7_Win8\64
Management Engine	\EasyBoard-882E\ME\ME_8.0.20.1513
Intel Turbo	\EasyBoard-882E\Turbo Boost

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Chapter 3

BIOS

The BIOS Setup utility is featured by AMI BIOS to configure the system settings stored in the system's BIOS ROM. AMI BIOS is activated once the computer powers on.

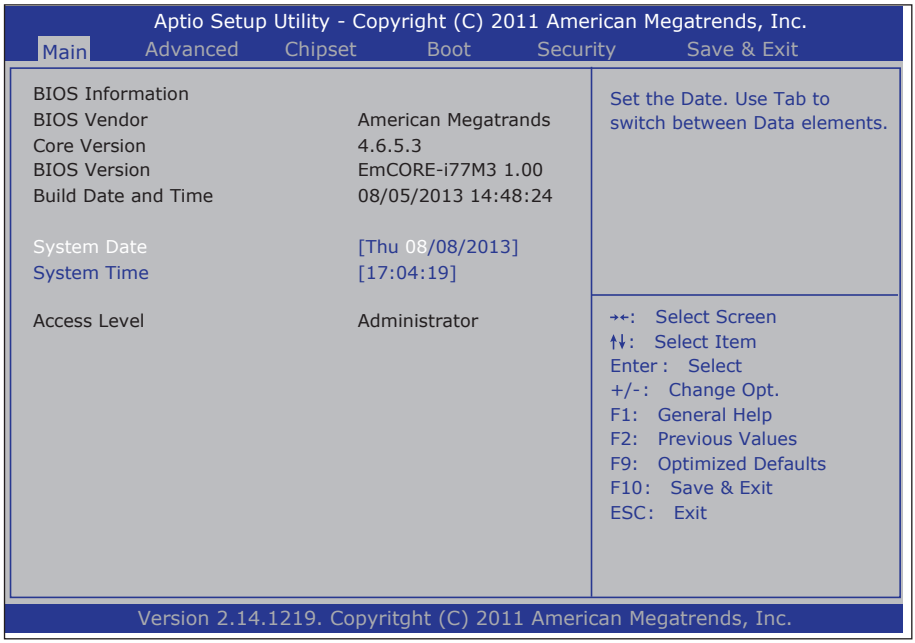
After entering the utility, use the left/right arrow keys to navigate between the top menus and use the down arrow key to access one.

Menu	Description
Main	See 3.1. Main on page 41.
Advanced	See 3.2. Advanced on page 42.
Chipset	See 3.3. Chipset on page 58.
Boot	See 3.4. Boot on page 41.
Security	See 3.5. Security on page 71.
Exit	See 3.6. Save & Exit on page 72.

NOTE: For system stability and performance, this BIOS utility is constantly improved. The screenshots demonstrated and descriptions hereinafter are for reference only and may not exactly meet what is presented onscreen.

3.1. Main

The **Main** menu displays some BIOS info and features the settings of **System Date** and **System Time**.



The BIOS info displayed is:

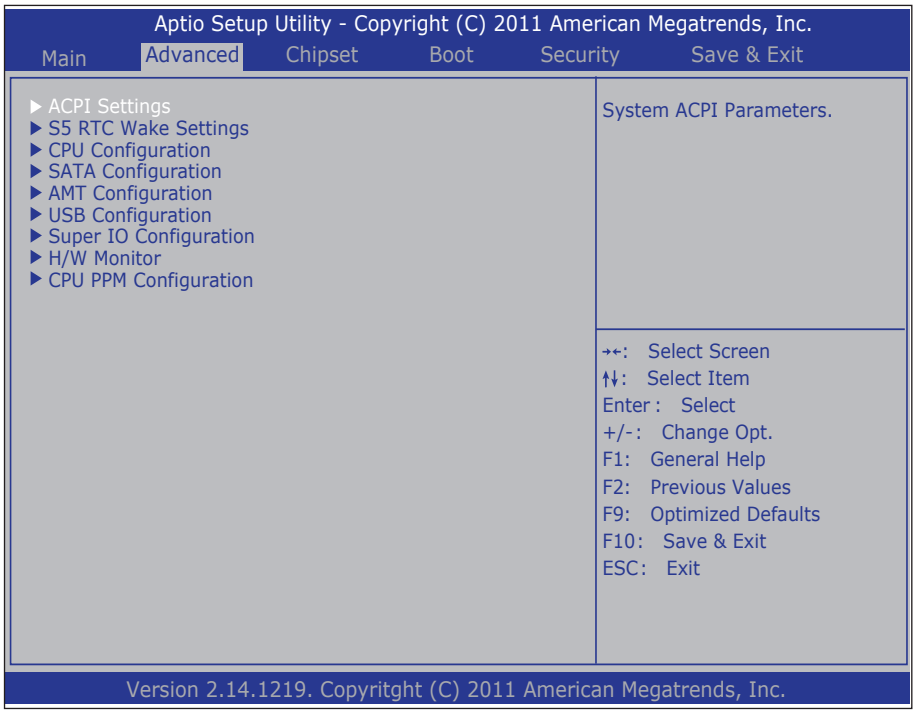
Info Item	Description
BIOS Vendor	Delivers the provider of the BIOS Setup utility.
Core Version	Delivers the version of the core.
BIOS Version	Delivers the computer's BIOS version.
Build Date and Time	Delivers the date and time the BIOS Setup utility was made/updated.
Access Level	Delivers the level by which the BIOS Setup utility is being accessed at the moment.

The featured settings are:

Setting	Description
System Time	Sets system time.
System Date	Sets system date.

3.2. Advanced

The **Advanced** menu controls the system's CPU, IDE, Super IO, AHCI and USB. It also helps users monitor hardware health.

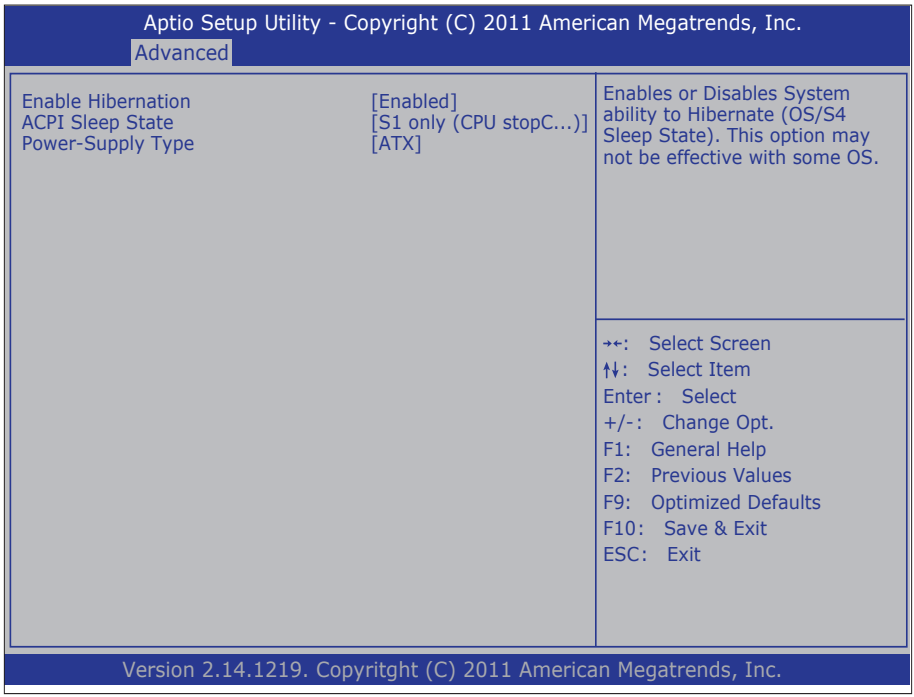


The featured submenus are:

Submenu	Description
ACPI Settings	See 3.2.1. ACPI Settings on page 43.
S5 RTC Wake Settings	See 3.2.2. S5 RTC Wake Settings on page 44
CPU Configuration	See 3.2.3. CPU Configuration on page 46.
SATA Configuration	See 3.2.4. SATA Configuration on page 48.
AMT Configuration	See 3.2.5. AMT Configuration on page 51.
USB Configuration	See 3.2.6. USB Configuration on page 53.
Super IO Configuration	See 3.2.7. Super IO Configuration on page 54.
H/W Monitor	See 3.2.8. Hardware Monitor on page 56.
CPU PPM Configuration	See 3.2.9. CPU PPM Configuration on page 57.

3.2.1. ACPI Settings

Access this submenu to configure the system's ACPI (Advanced Configuration and Power Interface).

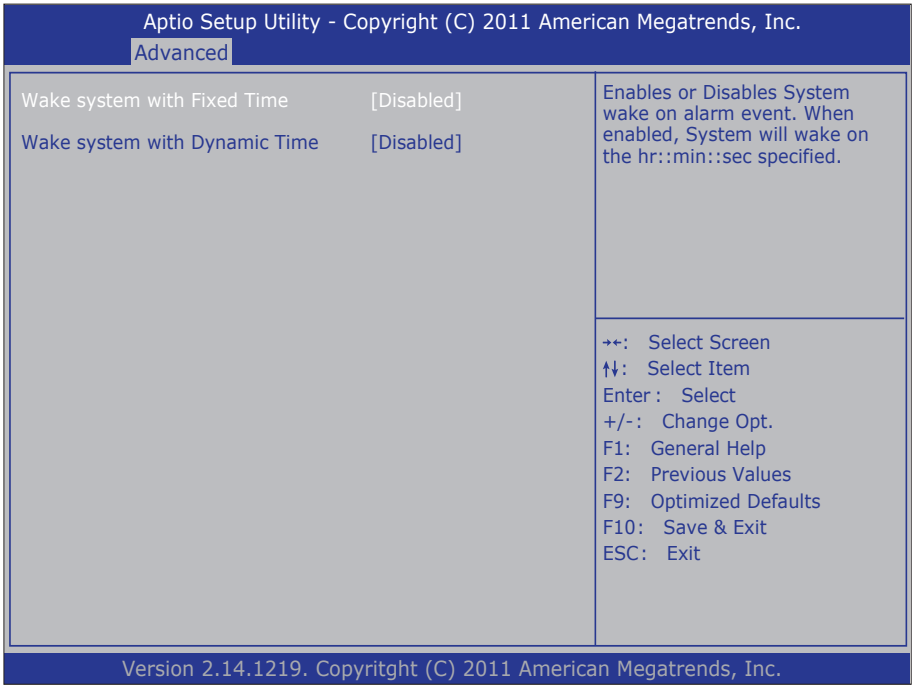


The featured settings are:

Setting	Description
Enable Hibernation	Enables/disables the system to/from hibernation (OS/S4 Sleep State). ▸ This option may not be effective with some OS. ▸ **Enabled** is the default.
ACPI Sleep State	Sets the highest ACPI sleep state that system enters when the suspend button is hit. ▸ **S1 (CPU Stop Clock)** is the only option.
Power-Supply Type	Sets the power-supply type. ▸ Options available are **AT** and **ATX** (default). ▸ Note to make consistent jumper setting for JPWR1 to avoid possible conflict.

3.2.2. S5 RTC Wake Settings

Access this submenu to enable/disable the system to wake up on a specified time.



The featured setting is:

Setting	Description
Wake System with Fixed Time	Sets if to awake the system at a defined moment. ▸ Options available are **Enabled** and **Disabled** (default). ▸ Enable this feature to awake the system at a defined moment in time. When enabled, the following settings become available:

Setting	Description
Wake up hour	Defines the (hour) time to awake the system. ▸ 0 to 23 configurable.
Wake up minute	Defines the (minute) time to awake the system. ▸ 0 to 59 configurable.
Wake up second	Defines the (second) time to awake the system. ▸ 0 to 59 configurable.

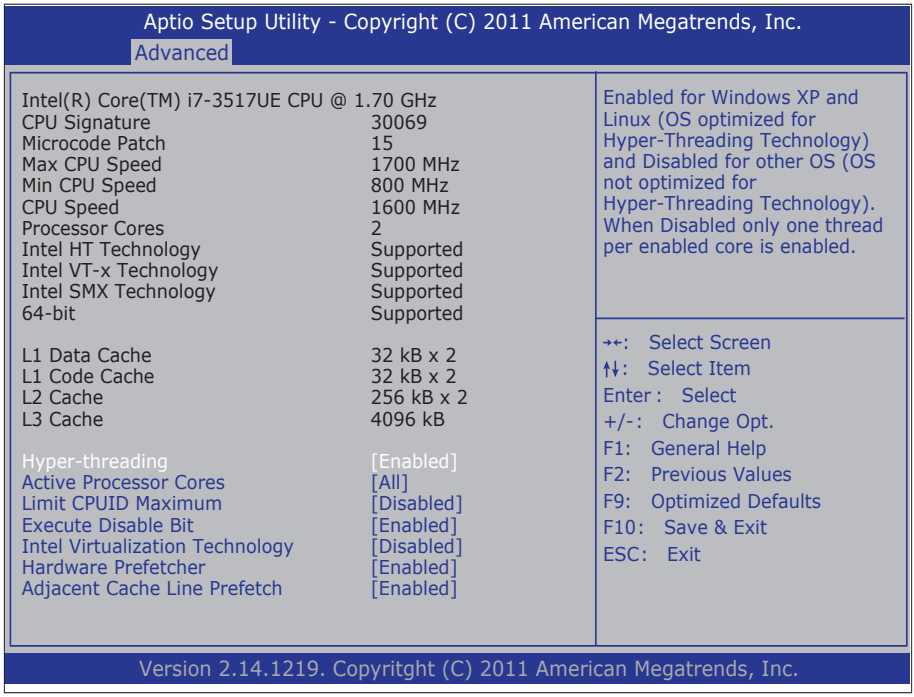
<table>
<tr>
<td>Wake System with Dynamic TIme</td>
<td>Sets if to awake the system some time in the future.

Options available are Enabled and Disabled (default).
Enable this feature to awake the system some time from now. When enabled, the following setting becomes available:

<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>Wake up minute increase</td><td>Defines how long from now to awake the system.
1 to 5 minutes configurable.</td></tr>
</table>
</td>
</tr>
</table>

3.2.3. CPU Configuration

Access this submenu to identify the CPU and its capabilities by running a report listing the CPU's model name, processor speed, microcode revision, max./min. processor speeds, processor cores, Intel® Hyper-Threading Technology support and so on. This submenu also features the following settings to configure the CPU:



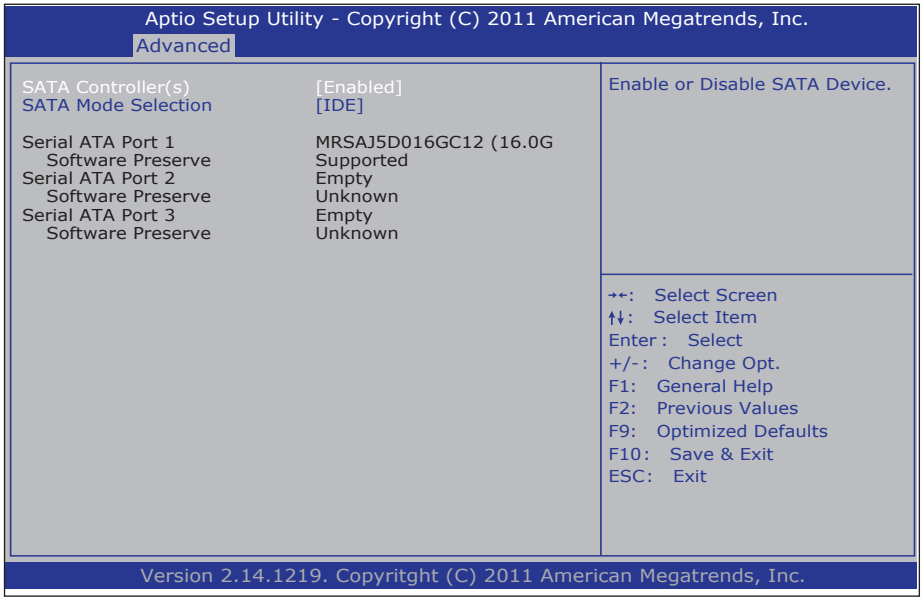
The featured settings are:

Setting	Description
Hyper Threading Technology	Enables/disables the processor's Hyper-threading feature. ▸ Select **Enabled** for Windows XP and Linux4. (These are the OS optimized for Hyper-threading Technology) ▸ Select **Disabled** for the other OS (, which are not optimized for Hyper-threading Technology). ▸ **Enabled** is the default. ▸ When disabled, only one thread per enabled core is enabled.

Active Processor Cores	Configures the number of cores to enable in each processor package. ▸ Available options are: **All** and **1**. ▸ **All** is the default.
Limit CPUID Maximum	Sets whether the processor should limit the maximum CPUID input value to 03h when the operating system queries it upon startup. ▸ Select **Enabled** to allow a processor with Intel® Hyper-Threading technology to work with an operating system that doesn't support it. ▸ **Disabled** is the default.
Execute Disable Bit	Enables/disables the processor's capability to mark the memory as executable or non-executable, when the operating system supports. ▸ This feature can prevent some classes of viruses or worms that exploit buffer over run vulerabilities and can thus help improve the overall security of the system. ▸ **Enabled** is the default.
Intel Virtualization Technology	Enables/disables Intel® Virtualization Technology (IVT) extensions that allow multiple operating systems to simultaneously run on the same computer by creating virtual machine, each running its own x86 operating system. ▸ **Disabled** is the default.
Intel(R) SpeedStep(tm) tech	Enables/disables SpeedStep™ technology for better power saving. ▸ SpeedStep™ is a technology built into some Intel® processors that allows the processor's clock speed to be dynamically changed by software. ▸ **Enabled** is the default.
Hardware Prefetcher	Enables/disables the processor's hardware prefetcher that auto-analyzes its requirements and prefetches data and instructions from the memory into the Level 2 cache that are likely to be required in the near future, which reduces the latency associated with memory reads. ▸ Enable the hardware prefetcher to allow auto-prefetching data and code for the processor.
Adjacent Cache Line Prefetch	Enables/disables the processor's hardware adjacent cache line prefetch mechanism that auto-fetches an extra 64-byte cache line whenever the processor requests 64-byte cache line. This reduces cache latency by makeing the next cache line immediately available if the processors requires it as well. ▸ Select **Enabled** to have the processor retrieve the currently requested cache line as well as the subsequent cache line. ▸ Select **Disabled** to have the processor retrieve only the currently requested cache line.

3.2.4. SATA Configuration

Access this submenu to view SATA device(s) information and also to configure SATA device(s).



The featured settings are:

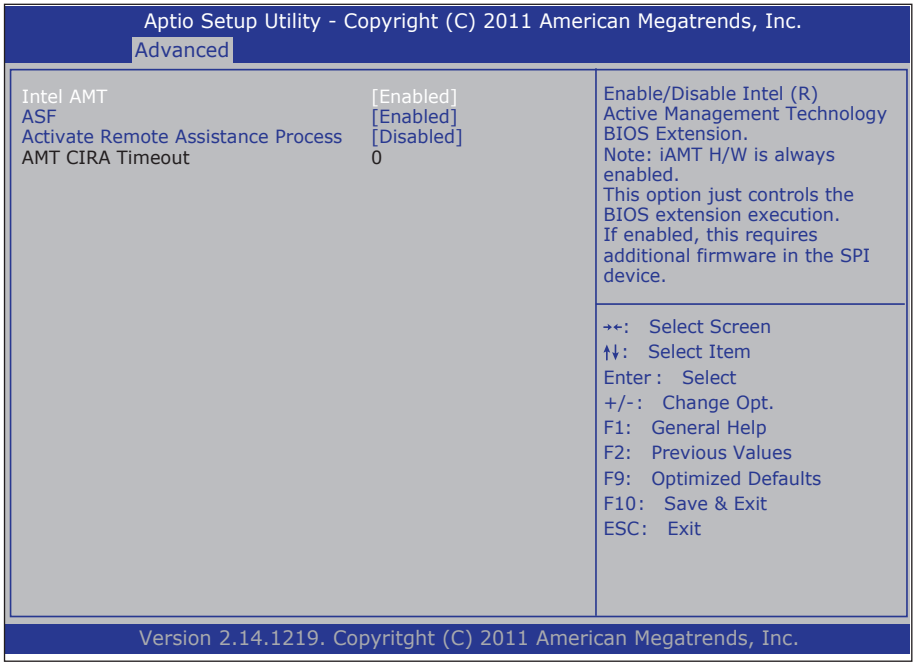
<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>SATA Controller(s)</td><td>Enables/disables SATA device(s).
▸ Enabled is the default.</td></tr>
<tr><td>SATA Mode Selection</td><td>Configures how SATA controller(s) operate.
▸ Options available are IDE (default), AHCI and RAID.</td></tr>
<tr><td>SATA Controller Speed</td><td>Sets the maximum speed for the SATA controller to support.
▸ Options available are: Gen1, Gen2 and Gen3 (default).
▸ This setting is available only when SATA Mode Selection is set to AHCI or RAID.</td></tr>
<tr><td>Software Feature Mask Configuration</td><td>This is a submenu to configure the features of RAID (Redundant Array of Inexpensive Disks).The featured settings are:
<table>
<tr><th>Setting</th><th>Description</th><th>Setting</th><th>Description</th></tr>
<tr><td>RAID0</td><td>Enables/disables RAID0.
▸ Enabled is the default.</td><td>RAID10</td><td>Enables/disables RAID10.
▸ Enabled is the default.</td></tr>
<tr><td>RAID1</td><td>Enables/disables RAID1.
▸ Enabled is the default.</td><td>RAID5</td><td>Enables/disables RAID5.
▸ Enabled is the default.</td></tr>
</table>
▸ This submenu is available only when SATA Mode Selection is set to AHCI or RAID.</td></tr>
</table>

<table>
<tr><td>Alternate ID</td><td>Enables/disables reporting the alternate device ID.
▸ This setting is available only when SATA Mode Selection is set to RAID.
▸ Disabled is the default.</td></tr>
<tr><td>Serial ATA Port 1</td><td>Features the following settings:
<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>Port 0</td><td>Enables/disables the SATA port.
▸ Enabled is the default.</td></tr>
<tr><td>Hot Plug</td><td>Sets whether to make the SATA port an hot pluggable one.
▸ Disabled is the default.</td></tr>
<tr><td>External SATA</td><td>Enables/disables external SATA support.
▸ Disabled is the default.</td></tr>
<tr><td>SATA Device Type</td><td>Defines whether the SATA port is connected to a Solid State Drive or Hard Disk Drive.
▸ Hard Disk Drive is the default.</td></tr>
<tr><td>Spin Up Device</td><td>For the platforms with numerous Serial ATA hard disk drives, the power issue regarding the electrical current load during system power-up is often critical. This setting enables/disables “Staggered Spin Up”, which provides a simple mechanism for SATA HBAs (host bus adapters) to sequence disk drive initialization and spin-up.
▸ Disabled is the default.</td></tr>
</table>
▸ These settings are available only when SATA Mode Selection is set to AHCI or RAID.</td></tr>
<tr><td>Serial ATA Port 2</td><td>Features the following settings:
<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>Port 1</td><td>Enables/disables the SATA port.
▸ Enabled is the default.</td></tr>
<tr><td>Hot Plug</td><td>Sets whether to make the SATA port an hot pluggable one.
▸ Disabled is the default.</td></tr>
<tr><td>External SATA</td><td>Enables/disables external SATA support.
▸ Disabled is the default.</td></tr>
<tr><td>SATA Device Type</td><td>Defines whether the SATA port is connected to a Solid State Drive or Hard Disk Drive.
▸ Hard Disk Drive is the default.</td></tr>
<tr><td>Spin Up Device</td><td>For the platforms with numerous Serial ATA hard disk drives, the power issue regarding the electrical current load during system power-up is often critical. This setting enables/disables “Staggered Spin Up”, which provides a simple mechanism for SATA HBAs (host bus adapters) to sequence disk drive initialization and spin-up.
▸ Disabled is the default.</td></tr>
</table>
▸ These settings are available only when SATA Mode Selection is set to AHCI or RAID.</td></tr>
</table>

<table>
<tr><td>Serial ATA Port 3</td><td>Features the following settings:
<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>Port 4</td><td>Enables/disables the SATA port.
▸ Enabled is the default.</td></tr>
<tr><td>Hot Plug</td><td>Sets whether to make the SATA port an hot pluggable one.
▸ Disabled is the default.</td></tr>
<tr><td>External SATA</td><td>Enables/disables external SATA support.
▸ Disabled is the default.</td></tr>
<tr><td>Spin Up Device</td><td>For the platforms with numerous Serial ATA hard disk drives, the power issue regarding the electrical current load during system power-up is often critical. This setting enables/disables “Staggered Spin Up”, which provides a simple mechanism for SATA HBAs (host bus adapters) to sequence disk drive initialization and spin-up.
▸ Disabled is the default.</td></tr>
</table>
▸ These settings are available only when SATA Mode Selection is set to AHCI or RAID.</td></tr>
</table>

3.2.5. AMT Configuration

Intel® Active Management Technology (Intel® AMT) is a hardware-based solution that uses out-of-band communication for basic management of client systems, which allows a system administrator to monitor and manage the computers and other network equipment by remote control even if the hard drive is crashed, the system is turned off or the operating system is locked.



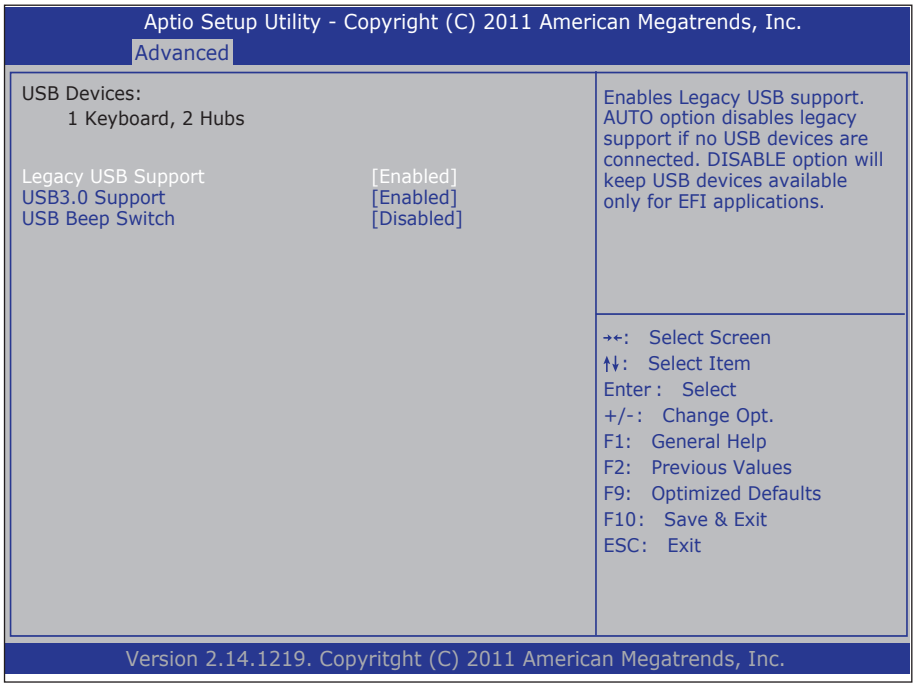
The featured settings are:

Setting	Description
Intel AMT	Enables/disables Intel® Active Management Technology BIOS extensions. ▸ iAMT hardware is always enabled. ▸ This setting only controls BIOS extension execution. ▸ **Enabled** is the default. ▸ When enabled, additional firmware is required in the SPI device.
ASF	Enables/disables Alert Specification Format, a DMTF (Distributed Management Task Force) standard for remote monitoring, management and control of computer system in both OS-present and OS-absent environments. ▸ **Enabled** is the default.

Activate Remote Assistance Process	Enables/disables CIRA (Client-Initiated Remote Access) boot. ▸ **Disabled** is the default.
AMT CIRA Timeout	Customizes the timeout for the establishment of MPS connection. ▸ This setting is only available when **Activate Remote Assistance Process** is enabled. ▸ Set it to 0 to use the default timeout value of 60 seconds. ▸ Set it to 255 to have MEBx wait until the connection succeeds. ▸ CIRA means “Client Initiated Remote Access”.

3.2.6. USB Configuration

Access this submenu to view the USB device(s) enabled in the system. It also configures USB-related features.

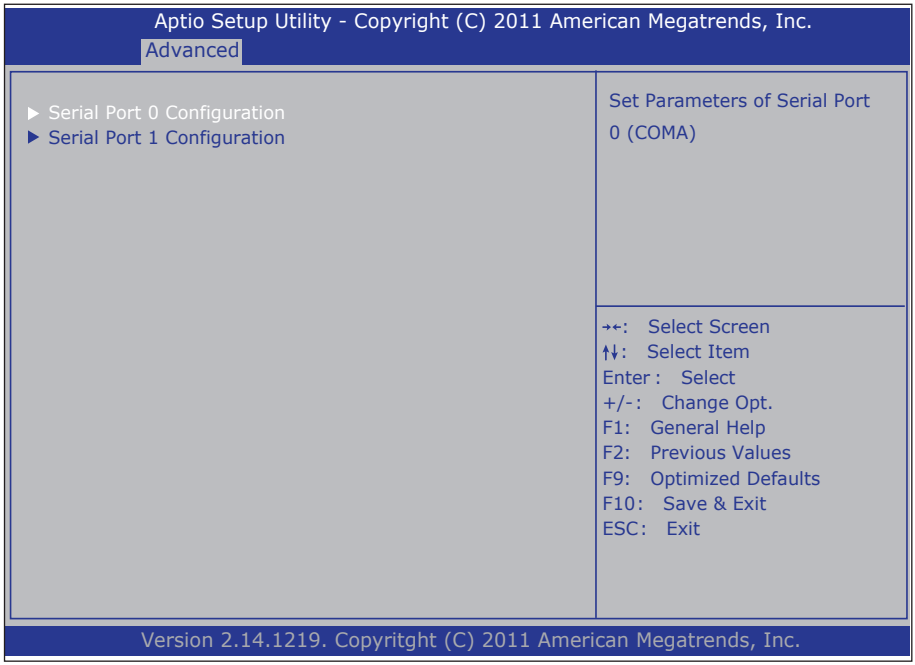


The featured settings are:

Setting	Description / Available Options
Legacy USB Support	Enables/disables legacy USB support including USB flash drives and USB hard drives. ▸ Options available are **Disabled** and **Enabled** (default).
USB3.0 Support	Enables/disables USB 3.0 controller support. ▸ **Enabled** is the default.
USB Beep Switch	Enables/disables USB beep sound. ▸ **Disabled** is the default.

3.2.7. Super IO Configuration

This submenu opens in context with the system's four serial ports, COM1 and COM2, to configure the Super IO chipset.



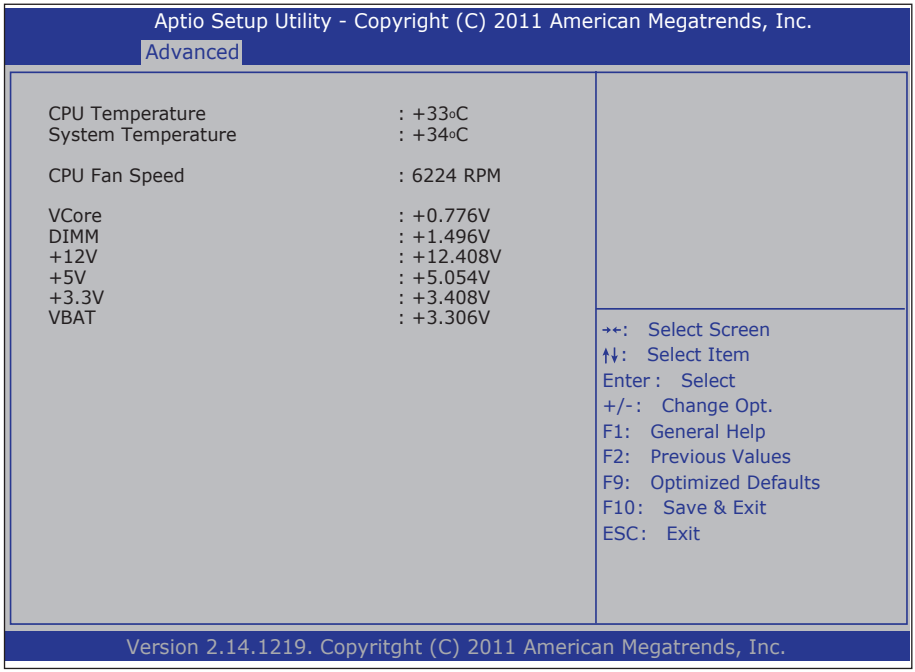
The featured settings are:

Submenu/Setting	Description	
Serial Port 0 Configuration	Configures the system's serial port (COM port). The featured settings are:	
	Setting	**Description**
	Serial Port	Enables/disables the serial port. ▸ **Enabled** is the default.
	Change Settings	Sets the optimal IO address and IRQ info for the serial port. ▸ Options available are: **IO=3F8h; IRQ=4** (default) **IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12**; **IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12**; **IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12**; **IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12**;

<table>
<tr><td>Serial Port 1 Configuration</td><td>Configures the system's serial port (COM port). The featured settings are:
<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>Serial Port</td><td>Enables/disables the serial port.
▸ Enabled is the default.</td></tr>
<tr><td>Change Settings</td><td>Sets the optimal IO address and IRQ info for the serial port.
▸ Options available are:
IO=2F8h; IRQ=3 (default)
IO=3F8h; IRQ=3,4,5,6,7,9,10,11,12;
IO=2F8h; IRQ=3,4,5,6,7,9,10,11,12;
IO=3E8h; IRQ=3,4,5,6,7,9,10,11,12;
IO=2E8h; IRQ=3,4,5,6,7,9,10,11,12;</td></tr>
</table></td></tr>
</table>

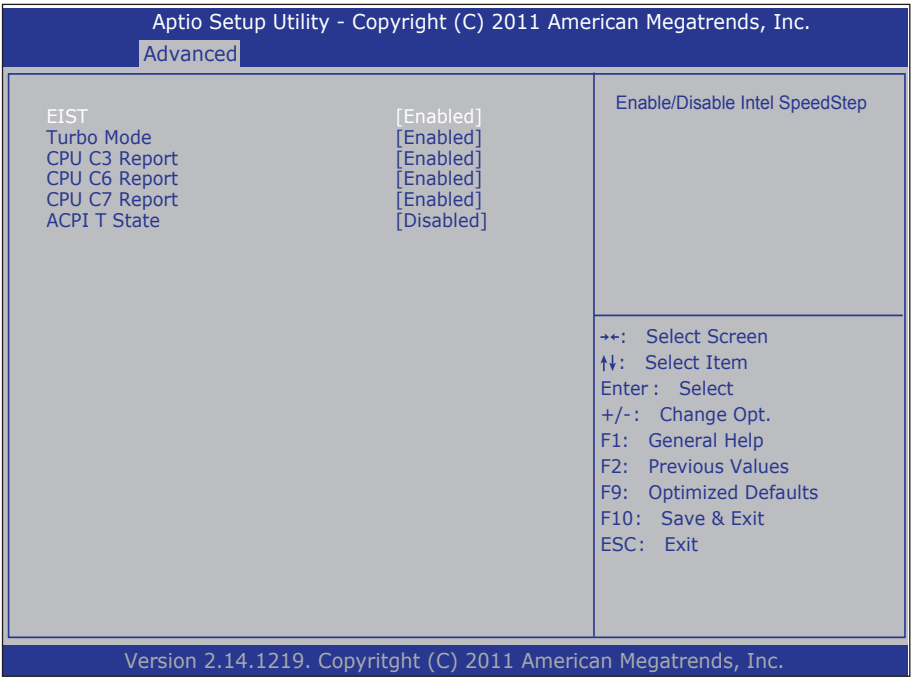
3.2.8. Hardware Monitor

Access this submenu to view the system's hardware health status.



3.2.9. CPU PPM Configuration

Access this submenu to control processor's power management.

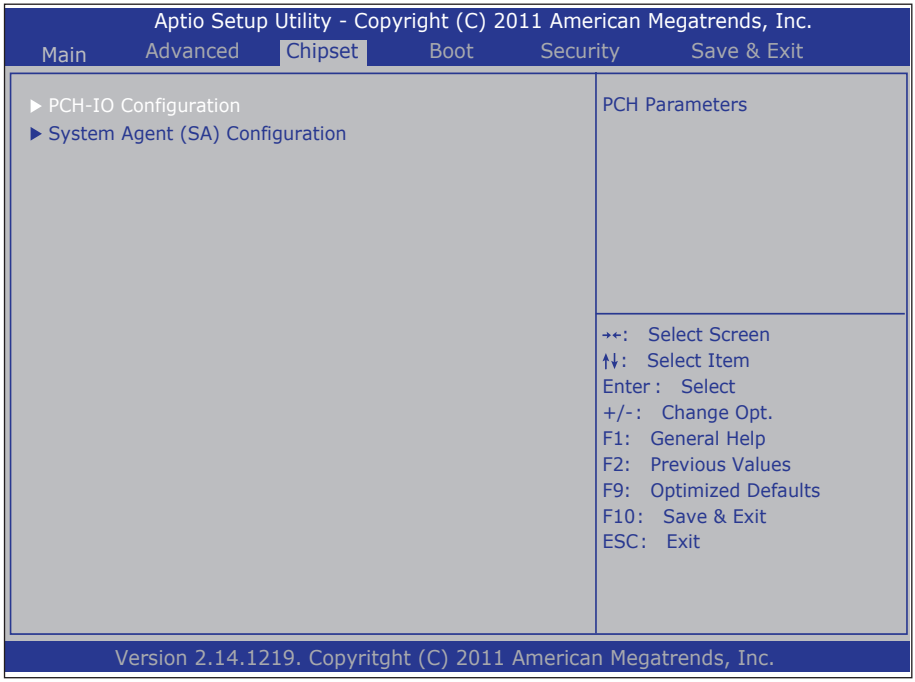


The featured settings are:

Submenu	Description
EIST	Enables/disables EIST (Enhanced Intel SpeedStep® Technology), which allows the system to dynamically adjust processor voltage and core frequency to reduce power consumption and heat production. ▸ **Enabled** is the default.
Turbo Mode	Enables/disables the turbo mode, in which the CPU performance can be boosted without generating extra heat. ▸ **Disabled** is the default.
CPU C3 Report	Enables/disables CPU C3 (ACPI C2) report to the OS. ▸ **Enabled** is the default.
CPU C6 Report	Enables/disables CPU C6 (ACPI C3) report to the OS. ▸ **Enabled** is the default.
CPU C7 Report	Enables/disables CPU C7 (ACPI C3) report to the OS. ▸ **Enabled** is the default.
ACPI T State	Enables/disables ACPI T-state, which allows the CPU driver to receive _TPC change notifications so as to control the processor speed. ▸ **Disabled** is the default.

3.3. Chipset

Access this **Chipset** menu to configure the system's chipset.



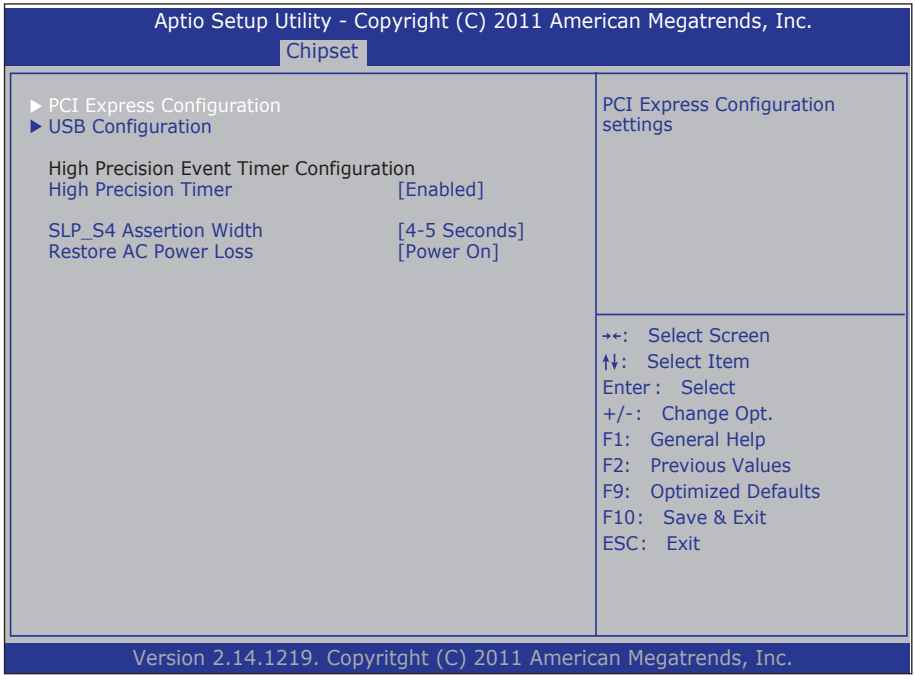
The featured submenu are **System Agent (SA) Configuration** and **PCH-IO Configuration**, which are covered in the following sections:

Submenu	Description
PCH-IO Configuration	Configures the PCH. ▸ See 3.3.1. PCH IO Configuration on page 59 for more details.
System Agent (SA) Configuration	Configures System Agent, i.e. the north bridge. ▸ See 3.3.2. System Agent (SA) Configuration on page 63 for more details.

WARNING: Wrong settings in these submenus may cause system malfunction.

3.3.1. PCH IO Configuration

Access this submenu to configure PCH parameters.



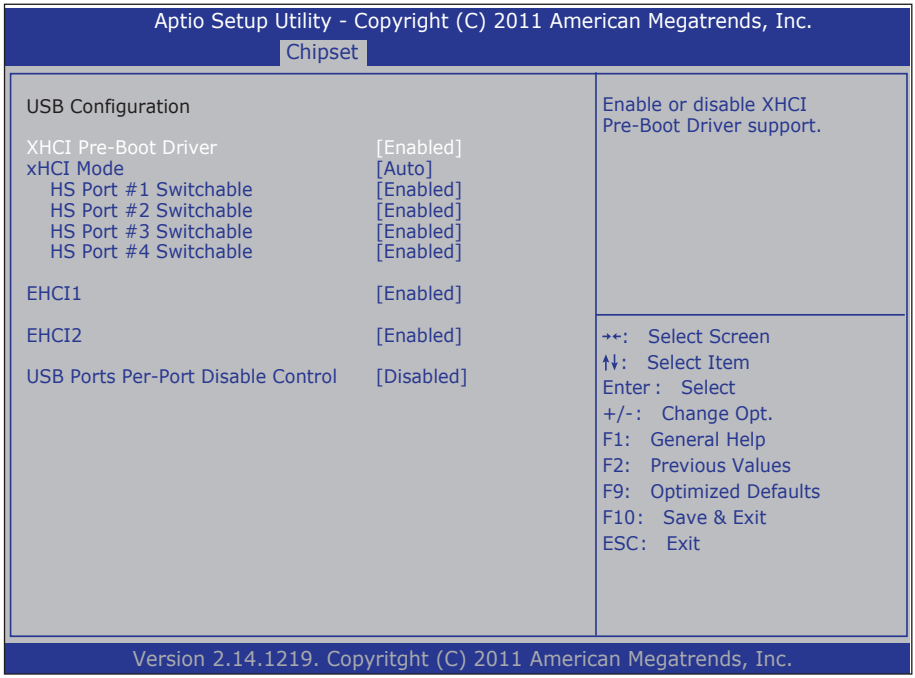
The featured settings are:

<table>
<tr><th>Setting/Submenu</th><th>Description</th></tr>
<tr><td>PCI Express Configuration</td><td>Configures PCI Express by the following settings:
<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>LAN1 Controller</td><td>Enables/disables LAN1 port.
▸ Enabled is the default.</td></tr>
<tr><td>LAN2 Controller</td><td>Enables/disables LAN2 port.
▸ Enabled is the default.</td></tr>
<tr><td>Mini Card Controller</td><td>Enables/disables the mini SIM socket.
▸ Enabled is the default.</td></tr>
</table></td></tr>
<tr><td>USB Configuration</td><td>See 3.3.1.1. USB Configuration on page 61.</td></tr>
<tr><td>High Precision Timer</td><td>Enables/disables the “High Precision Timer”, which delivers more accurate controls for multimedia events.
▸ Enabled is the default.</td></tr>
</table>

SLP_S4 Assertion Width	Sets the minimum assertion width of the SLP_S4# signal. ► Options available are: **1-2 Seconds** **2-3 Seconds** **3-4 Seconds** **4-5 Seconds** (default)
Restore on AC Power Loss	Sets whether the system should power on or power off when the power resumes after accidental power loss. ‣ Options available are **Power On** (default) and **Power Off**.

3.3.1.1. USB Configuration

Access this submenu to configure the system's USB ports.



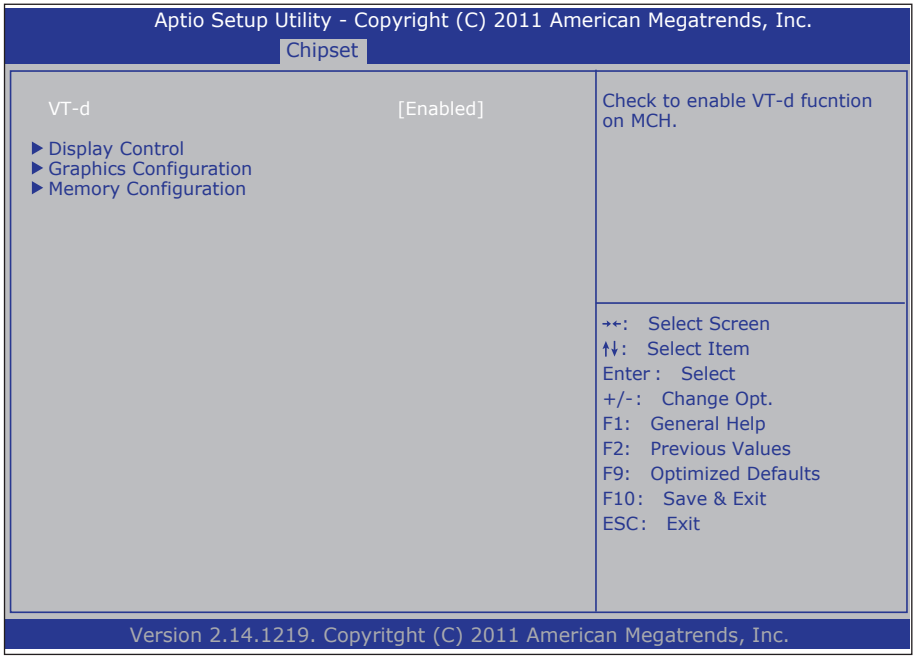
The featured settings are:

Setting	Description
XHCI Pre-Boot Driver	Enables/disables the XHCI driver support before booting to the O.S. ▸ **Enabled** is the default.
xHCI Mode	Configures how the xHCI controller works. ▸ Select **Disabled** to make the onboard USB 3.0 ports function like 2.0 ones, which is optimal for the OS that does not have built-in USB 3.0 driver ▸ Select **Enabled** to make the onboard USB 3.0 ports function like 3.0 ones. ▸ Select **Auto** to have the onboard USB 3.0 port function like 2.0 ports before the O.S. loads USB 3.0 driver, which is the default. ▸ Select **Smart Auto** to have the BIOS avoid downgrading the USB 3.0 ports to 2.0 before the O.S. loads USB 3.0 driver.
HS Port # Switchable	Enables/disables a USB 2.0 port to/from USB 3.0 functionality. ▸ **Enabled** is the default.

EHCI1	Enables/disables the USB EHCI (USB2.0) functions. ▸ **Enabled** is the default. ▸ One EHCI controller must always be enabled.
EHCI2	Enables/disables the USB EHCI (USB2.0) functions. ▸ **Enabled** is the default. ▸ One EHCI controller must always be enabled.
USB Ports Per-Port Disable Control	Respectively enables/disables a USB port. ▸ **Disabled** is the default.

3.3.2. System Agent (SA) Configuration

Access this submenu to configure the south bridge.

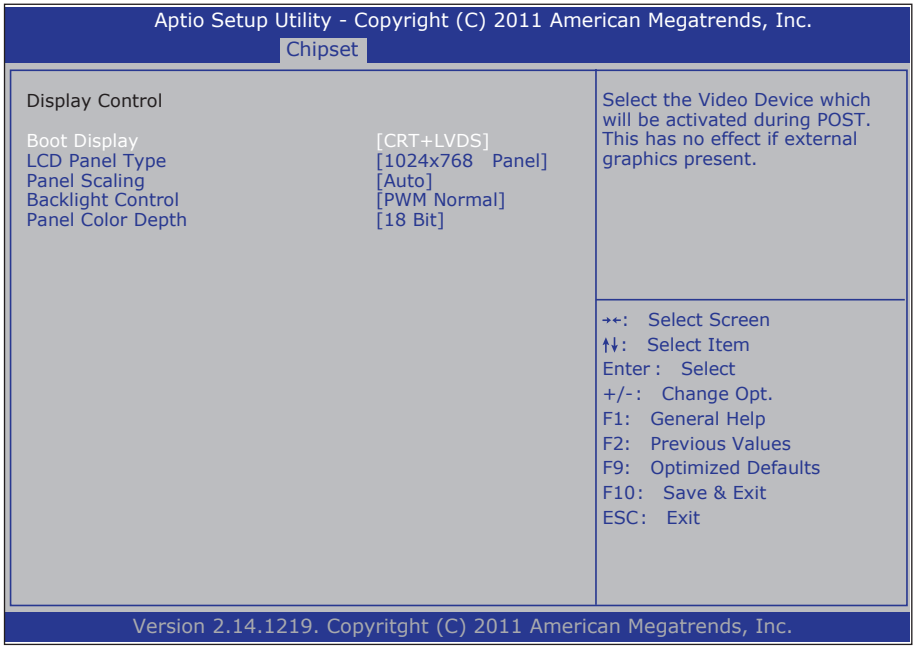


The featured settings are:

Setting / Submenu	Description
VT-d	Enables/disables Intel® virtualization technology for directed I/O on the MCH (memory controller hub). ▸ **Enabled** is the default.
Display Control	Configures the system's display feature. ▸ See 3.3.2.1. Display Control on page 64.
Graphics Configuration	Configures the system's graphics. ▸ See 3.3.2.2. Graphics Configuration on page 66.
Memory Configuration	Views the system's memory configuration. ▸ See 3.3.2.3. Memory Configuration on page 68.

3.3.2.1. Display Control

Access this submenu to configure the system's display feature.



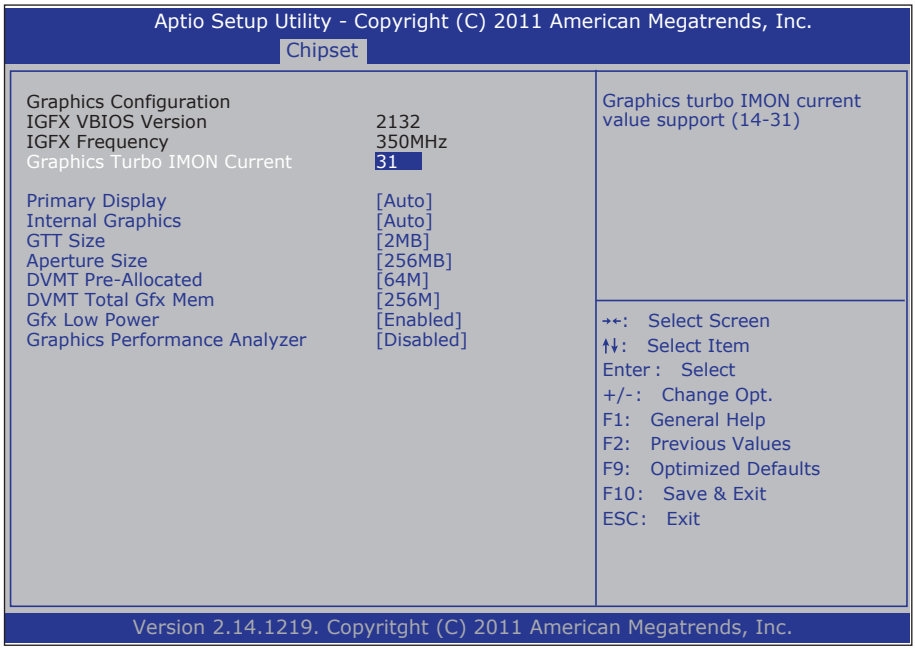
The featured settings are:

Setting	Description
Boot Display	Sets the video device to activate during POST. ▸ Options available are **CRT**, **LVDS**, **CRT + LVDS** (default) and **DVI**. ▸ This setting has no effect if an external graphics card is present.
LCD Panel Type	Sets the LCD panel types. ▸ Options available are: **VBIOS Default**, **640x480 Panel**, **800x600 Panel**, **1024x768 Panel** (default), **1280x1024 Panel**, **1400x1050(RB) Panel**, **1400x1050 Panel2**, **1600x1200 Panel**, **1366x768 Panel**, **1680x1050 Panel**, **1920x1200 Panel**, **1600x900 Panel**, **1024x768 Panel**, **1280x800 Panel**, **1920x1080 Panel**, **2048x1536 Panel**

Panel Scaling	Sets the LCD panel scaling for the internal graphics. ▸ The options available are **Auto** (default), **Off** and **Force Scaling**.
Backlight Control	Configures LCD backlight. ▸ The options available are **PWM Inverted**, **PWM Normal** (default), **GMBus Inverted**, and **GMBus Normal**.
Panel Color Depth	Sets the color depth for the LFP (local flat panel). ▸ Options available are **18 Bit** and **24 Bit** (default)

3.3.2.2. Graphics Configuration

Select **Graphics Configuration** to view graphics info and accesses graphics settings.



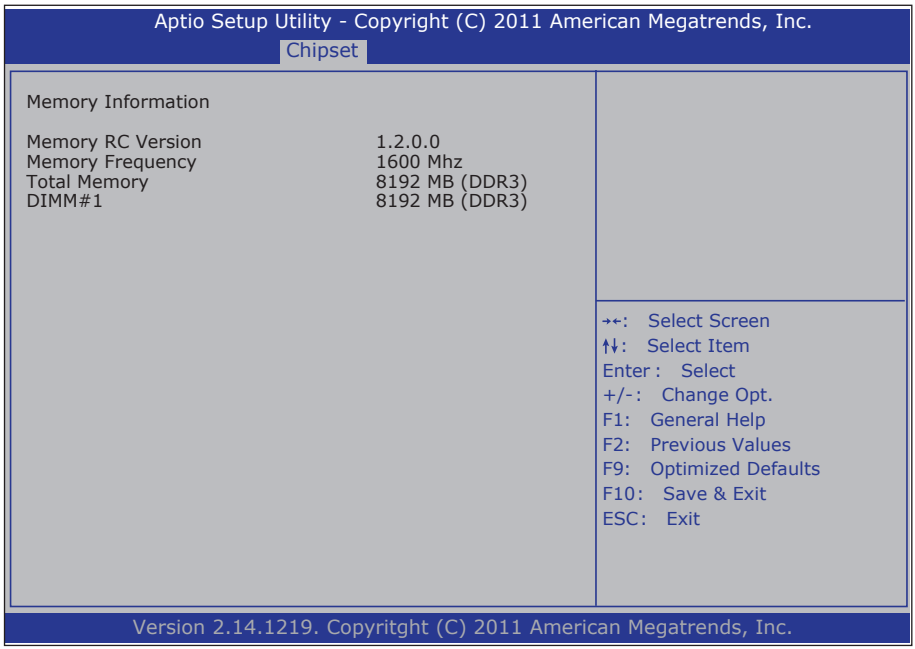
The featured settings are:

Setting	Description
Graphics Turbo IMON Current	Sets the graphics turbo IMON current values. ▸ Options available are **14** to **31**. ▸ **31** is the default.
Primary Display	Sets the primary display or leaves it on BIOS auto-detection. ▸ Options available are: **Auto** (default), **IGFX** (the internal graphics) and **PEG** (PCI Express graphics)
GTT Size	Sets the size of the GTT, which means “graphics translation table”, an I/O memory management unit (IOMMU) used by AGP and PCI Express graphics cards. ▸ Options available are **1MB** and **2MB** (default).
Aperture Size	Sets the aperture size, the maximum amount of system memory available to the graphics port. ▸ Options available are **128MB**, **256MB** (default) and **512MB**.

DVMT Pre-Allocated	Sets the DVMT 5.0 fixed (pre-allocated) memory size for the internal graphics device. ▸ Options available are:0M **32M** **64M** (default) **96M** **128M** **160M** **192M** **224M** **256M** **288M** **320M** **352M** **384M** **416M** **448M** **480M** **512M**
DVMT Total Gfx Memory	Sets the DVMT 5.0 total memory size for the internal graphics device. ▸ Options available are: **128M** **256M** (default) **MAX**
Gfx Low Power Mode	Enables/disables graphics low power mode. ▸ This setting is applicable to SFF (small form factor) only. ▸ **Enabled** is the default.
Graphics Performance Analyzer	Enables/disables **Graphics Performance Analyzer**. ▸ **Disabled** is the default.

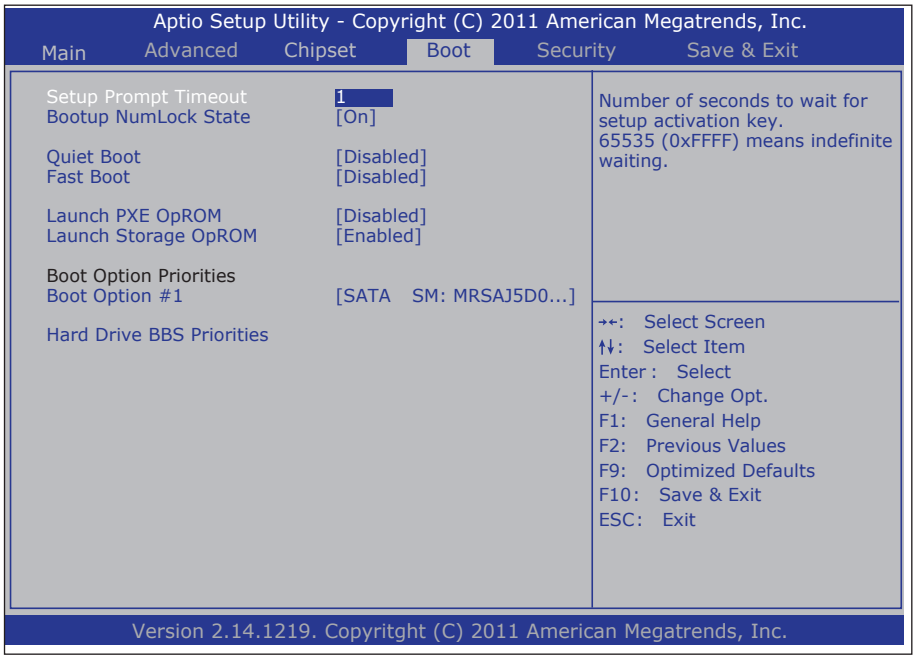
3.3.2.3. Memory Configuration

Access this submenu to view the system's memory information that includes memory RC version, memory frequency, total memory and the presence/ absence of memory module.



3.4. Boot

Access this menu to change system boot settings.



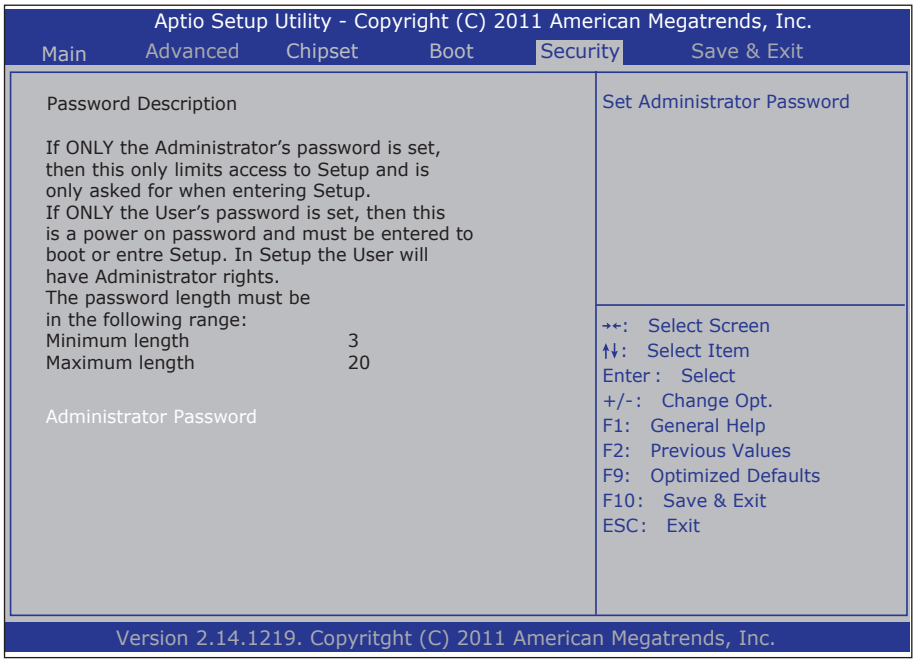
The featured submenu is:

Setting	Description
Setup Prompt Timeout	Sets how long to wait for the prompt for entering BIOS Setup to show. ▸ The default setting is **0** (sec). ▸ Set it to **65535** to wait indefinitely.
Bootup NumLock State	Sets whether to enable or disable the keyboard's NumLock state when the system starts up. ▸ Options available are **On** (default) and **Off**.
Quiet Boot	Sets whether to display the POST (Power-on Self Tests) messages or the system manufacturer's full screen logo during booting. ▸ Leave it as **Disabled**, which is the default, to display the normal POST message.
Launch PXE OpROM	Enables/disables the boot option for legacy network devices. ▸ **Disabled** is the default.
Launch Storage OpROM	Enables/disables the boot option for the legacy mass storage devices with Option ROM. ▸ **Enabled** is the default.

Boot Option Priority	Sets the very 1st boot device among the available device types. ▸ Option(s) available are the available device type(s).
Hard Drive BBS Priorities	Sets the very 1st boot device among the available storage drives. ▸ BBS means “BIOS Boot Specification”.

3.5. Security

The **Security** menu sets up the administrator password. Once an administrator password is set up, this BIOS Setup utility is limited to access and will ask for the password each time any access is attempted.

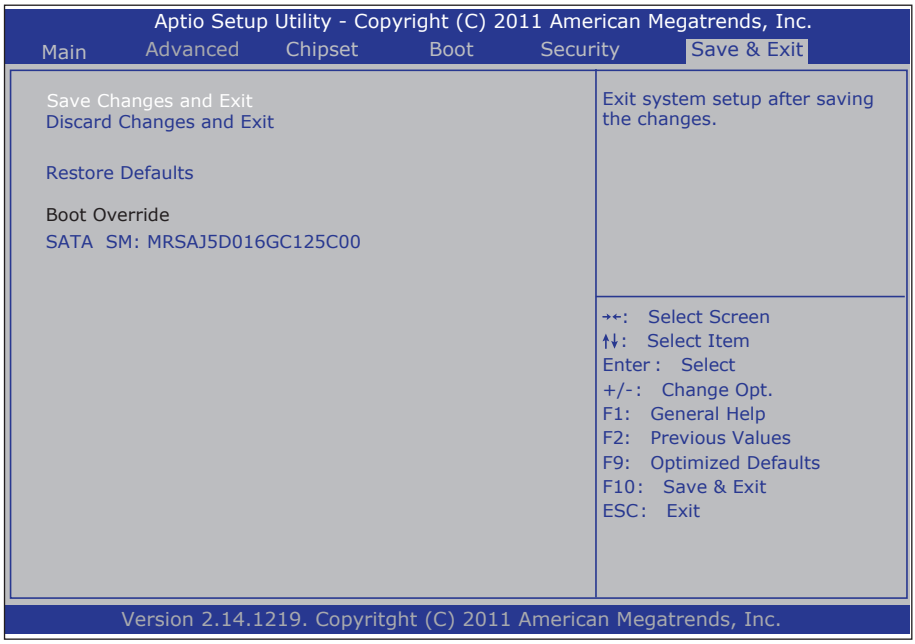


The featured settings are:

Setting	Description
Administrator Password	To set up an administrator password: 1. Select **Administrator Password**. A **Create New Password** dialog then pops up onscreen. 2. Enter your desired password that is no less than 3 characters and no more than 20 characters. 3. Hit [Enter] key to submit.

3.6. Save & Exit

The **Exit** menu features a handful of commands to launch actions from the BIOS Setup utility regarding saving changes, quitting the utility and recovering defaults.



The featured settings are:

Setting	Description
Save Changes and Exit	Saves the changes and quits the BIOS Setup utility. ▸ This is a command to launch an action from the BIOS Setup utility. ▸ When prompted for confirmation, select **OK** to save the changes and quit the BIOS Setup, or select **Cancel** to return to BIOS Setup.
Discard Changes and Exit	Discards the changes and quits the BIOS Setup utility. ▸ This is a command to launch an action from the BIOS Setup utility. ▸ When prompted for confirmation, select **OK** to quit BIOS Setup without saving the change(s), or select **Cancel** to return to the BIOS setup.
Restore Defaults	Loads the defaults to all settings. ▸ This is a command to launch an action from the BIOS Setup utility. ▸ When prompted for confirmation, select **OK** to load the defaults, or select **Cancel** to return to the BIOS setup.

Boot Override	**Boot Override** presents a list in context with the boot devices installed in the system. Select the device to boot up the system regardless of the currently configured boot priority. ▸ This is a command to launch action from the BIOS Setup utility.

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Appendices

Appendix A. AMI BIOS Checkpoints

A.1. Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS (Note):

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency and other CPU critical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is disabled. Perform keyboard controller BAT test. Save power-on CPUID value in scratch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Performs main BIOS checksum and updates recovery status accordingly.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.

Checkpoint	Description
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See POST Code Checkpoints section of document for more information.
DC	System is waking from ACPI S3 state
E1-E8 EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

A.2. Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS (Note):

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

A.3. POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS (Note):

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer.Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache – Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.

Checkpoint	Description
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.

Checkpoint	Description
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Initialization of system management interrupt by invoking all handlers. Please note this checkpoint comes right after checkpoint 20h
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

A.4. DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed (Note):

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:
HIGH BYTE XY
XY The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.
0 = func#0, disable all devices on the BUS concerned.
1 = func#1, static devices initialization on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.
3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.
The lower nibble 'Y' indicates the BUS on which the different routines are being

executed. 'Y' can be from 0 to 5.
0 = Generic DIM (Device Initialization Manager).
1 = On-board System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

A.5. ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events (Note):

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Entering sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Waking from sleep state S1, S2, S3, S4, or S5.

Note:
Please note that checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or option ROMs from add-in PCI devices.

Appendix B. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.
The following table lists the I/O port addresses used.

Address	Device Description
0x0000F060-0x0000F07F	Ethernet Controller
0x00000454-0x00000457	Motherboard resources
0x0000E000-0x0000E01F	Ethernet Controller
0x0000E000-0x0000E01F	PCI standard PCI-to-PCI bridge
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x000004D0-0x000004D1	Motherboard resources
0x0000F040-0x0000F05F	SM Bus Controller
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer
0x0000F130-0x0000F137	Standard Dual Channel PCI IDE Controller
0x0000F120-0x0000F123	Standard Dual Channel PCI IDE Controller
0x0000F110-0x0000F117	Standard Dual Channel PCI IDE Controller

Address	Device Description
0x0000F100-0x0000F103	Standard Dual Channel PCI IDE Controller
0x0000F0F0-0x0000F0FF	Standard Dual Channel PCI IDE Controller
0x0000F0E0-0x0000F0EF	Standard Dual Channel PCI IDE Controller
0x00000000-0x0000001F	Direct memory access controller
0x00000000-0x0000001F	PCI bus
0x00000081-0x00000091	Direct memory access controller
0x00000093-0x0000009F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller
0x00000060-0x00000060	Standard PS/2 Keyboard
0x00000064-0x00000064	Standard PS/2 Keyboard
0x0000F0D0-0x0000F0D7	Standard Dual Channel PCI IDE Controller
0x0000F0C0-0x0000F0C3	Standard Dual Channel PCI IDE Controller
0x0000F0B0-0x0000F0B7	Standard Dual Channel PCI IDE Controller
0x0000F0A0-0x0000F0A3	Standard Dual Channel PCI IDE Controller
0x0000F090-0x0000F09F	Standard Dual Channel PCI IDE Controller
0x0000F080-0x0000F08F	Standard Dual Channel PCI IDE Controller
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x00000D00-0x0000FFFF	PCI bus
0x00000070-0x00000077	System CMOS/real time clock
0x00000070-0x00000077	Motherboard resources
0x00000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000044-0x0000005F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000084-0x00000086	Motherboard resources
0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources

Address	Device Description
0x00000290-0x0000029F	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x00000200-0x0000020F	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x0000FFFF-0x0000FFFF	Motherboard resources
0x00000400-0x00000453	Motherboard resources
0x00000458-0x0000047F	Motherboard resources
0x00000500-0x0000057F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x0000F140-0x0000F147	PCI Serial Port
0x000000F0-0x000000FF	Numeric data processor
0x0000F000-0x0000F03F	Standard VGA Graphics Adapter
0x000003B0-0x000003BB	Standard VGA Graphics Adapter
0x000003C0-0x000003DF	Standard VGA Graphics Adapter

Appendix C. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 5	Ethernet Controller
IRQ 5	Ethernet Controller
IRQ 5	SM Bus Controller
IRQ 22	High Definition Audio Controller
IRQ 12	Microsoft PS/2 Mouse
IRQ 81	Microsoft ACPI-Compliant System
IRQ 82	Microsoft ACPI-Compliant System
IRQ 83	Microsoft ACPI-Compliant System
IRQ 84	Microsoft ACPI-Compliant System
IRQ 85	Microsoft ACPI-Compliant System
IRQ 86	Microsoft ACPI-Compliant System
IRQ 87	Microsoft ACPI-Compliant System
IRQ 88	Microsoft ACPI-Compliant System
IRQ 89	Microsoft ACPI-Compliant System
IRQ 90	Microsoft ACPI-Compliant System
IRQ 91	Microsoft ACPI-Compliant System
IRQ 92	Microsoft ACPI-Compliant System
IRQ 93	Microsoft ACPI-Compliant System
IRQ 94	Microsoft ACPI-Compliant System
IRQ 95	Microsoft ACPI-Compliant System
IRQ 96	Microsoft ACPI-Compliant System
IRQ 97	Microsoft ACPI-Compliant System
IRQ 98	Microsoft ACPI-Compliant System
IRQ 99	Microsoft ACPI-Compliant System
IRQ 100	Microsoft ACPI-Compliant System
IRQ 101	Microsoft ACPI-Compliant System
IRQ 102	Microsoft ACPI-Compliant System
IRQ 103	Microsoft ACPI-Compliant System

Level	Function
IRQ 104	Microsoft ACPI-Compliant System
IRQ 105	Microsoft ACPI-Compliant System
IRQ 106	Microsoft ACPI-Compliant System
IRQ 107	Microsoft ACPI-Compliant System
IRQ 108	Microsoft ACPI-Compliant System
IRQ 109	Microsoft ACPI-Compliant System
IRQ 110	Microsoft ACPI-Compliant System
IRQ 111	Microsoft ACPI-Compliant System
IRQ 112	Microsoft ACPI-Compliant System
IRQ 113	Microsoft ACPI-Compliant System
IRQ 114	Microsoft ACPI-Compliant System
IRQ 115	Microsoft ACPI-Compliant System
IRQ 116	Microsoft ACPI-Compliant System
IRQ 117	Microsoft ACPI-Compliant System
IRQ 118	Microsoft ACPI-Compliant System
IRQ 119	Microsoft ACPI-Compliant System
IRQ 120	Microsoft ACPI-Compliant System
IRQ 121	Microsoft ACPI-Compliant System
IRQ 122	Microsoft ACPI-Compliant System
IRQ 123	Microsoft ACPI-Compliant System
IRQ 124	Microsoft ACPI-Compliant System
IRQ 125	Microsoft ACPI-Compliant System
IRQ 126	Microsoft ACPI-Compliant System
IRQ 127	Microsoft ACPI-Compliant System
IRQ 128	Microsoft ACPI-Compliant System
IRQ 129	Microsoft ACPI-Compliant System
IRQ 130	Microsoft ACPI-Compliant System
IRQ 131	Microsoft ACPI-Compliant System
IRQ 132	Microsoft ACPI-Compliant System
IRQ 133	Microsoft ACPI-Compliant System
IRQ 134	Microsoft ACPI-Compliant System
IRQ 135	Microsoft ACPI-Compliant System
IRQ 136	Microsoft ACPI-Compliant System

Level	Function
IRQ 137	Microsoft ACPI-Compliant System
IRQ 138	Microsoft ACPI-Compliant System
IRQ 139	Microsoft ACPI-Compliant System
IRQ 140	Microsoft ACPI-Compliant System
IRQ 141	Microsoft ACPI-Compliant System
IRQ 142	Microsoft ACPI-Compliant System
IRQ 143	Microsoft ACPI-Compliant System
IRQ 144	Microsoft ACPI-Compliant System
IRQ 145	Microsoft ACPI-Compliant System
IRQ 146	Microsoft ACPI-Compliant System
IRQ 147	Microsoft ACPI-Compliant System
IRQ 148	Microsoft ACPI-Compliant System
IRQ 149	Microsoft ACPI-Compliant System
IRQ 150	Microsoft ACPI-Compliant System
IRQ 151	Microsoft ACPI-Compliant System
IRQ 152	Microsoft ACPI-Compliant System
IRQ 153	Microsoft ACPI-Compliant System
IRQ 154	Microsoft ACPI-Compliant System
IRQ 155	Microsoft ACPI-Compliant System
IRQ 156	Microsoft ACPI-Compliant System
IRQ 157	Microsoft ACPI-Compliant System
IRQ 158	Microsoft ACPI-Compliant System
IRQ 159	Microsoft ACPI-Compliant System
IRQ 160	Microsoft ACPI-Compliant System
IRQ 161	Microsoft ACPI-Compliant System
IRQ 162	Microsoft ACPI-Compliant System
IRQ 163	Microsoft ACPI-Compliant System
IRQ 164	Microsoft ACPI-Compliant System
IRQ 165	Microsoft ACPI-Compliant System
IRQ 166	Microsoft ACPI-Compliant System
IRQ 167	Microsoft ACPI-Compliant System
IRQ 168	Microsoft ACPI-Compliant System
IRQ 169	Microsoft ACPI-Compliant System

Level	Function
IRQ 170	Microsoft ACPI-Compliant System
IRQ 171	Microsoft ACPI-Compliant System
IRQ 172	Microsoft ACPI-Compliant System
IRQ 173	Microsoft ACPI-Compliant System
IRQ 174	Microsoft ACPI-Compliant System
IRQ 175	Microsoft ACPI-Compliant System
IRQ 176	Microsoft ACPI-Compliant System
IRQ 177	Microsoft ACPI-Compliant System
IRQ 178	Microsoft ACPI-Compliant System
IRQ 179	Microsoft ACPI-Compliant System
IRQ 180	Microsoft ACPI-Compliant System
IRQ 181	Microsoft ACPI-Compliant System
IRQ 182	Microsoft ACPI-Compliant System
IRQ 183	Microsoft ACPI-Compliant System
IRQ 184	Microsoft ACPI-Compliant System
IRQ 185	Microsoft ACPI-Compliant System
IRQ 186	Microsoft ACPI-Compliant System
IRQ 187	Microsoft ACPI-Compliant System
IRQ 188	Microsoft ACPI-Compliant System
IRQ 189	Microsoft ACPI-Compliant System
IRQ 190	Microsoft ACPI-Compliant System
IRQ 0	System timer
IRQ 19	Standard Dual Channel PCI IDE Controller
IRQ 19	Standard Dual Channel PCI IDE Controller
IRQ 19	PCI standard PCI-to-PCI bridge
IRQ 23	Standard Enhanced PCI to USB Host Controller
IRQ 1	Standard PS/2 Keyboard
IRQ 16	Standard Enhanced PCI to USB Host Controller
IRQ 16	PCI standard PCI-to-PCI bridge
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 8	System CMOS/real time clock
IRQ 11	Universal Serial Bus (USB) Controller
IRQ 11	PCI Simple Communications Controller

Level	Function
IRQ 17	PCI standard PCI-to-PCI bridge
IRQ 18	PCI standard PCI-to-PCI bridge
IRQ 10	PCI Serial Port
IRQ 13	Numeric data processor

Appendix D. BIOS Memory Map

Address	Device Description
0xF7E00000-0xF7E1FFFF	Ethernet Controller
0xF7E38000-0xF7E38FFF	Ethernet Controller
0xF7E30000-0xF7E33FFF	High Definition Audio Controller
0xFF000000-0xFFFFFFFF	Intel(R) 82802 Firmware Hub Device
0xFF000000-0xFFFFFFFF	Motherboard resources
0xF7D40000-0xF7D5FFFF	Ethernet Controller
0xF7C00000-0xF7CFFFFF	Ethernet Controller
0xF7C00000-0xF7CFFFFF	PCI standard PCI-to-PCI bridge
0xF7D60000-0xF7D63FFF	Ethernet Controller
0xF7E35000-0xF7E350FF	SM Bus Controller
0xFED00000-0xFED003FF	High precision event timer
0xF7E36000-0xF7E363FF	Standard Enhanced PCI to USB Host Controller
0xF7E37000-0xF7E373FF	Standard Enhanced PCI to USB Host Controller
0xA0000-0xBFFFF	PCI bus
0xA0000-0xBFFFF	Standard VGA Graphics Adapter
0xD0000-0xD3FFF	PCI bus
0xD4000-0xD7FFF	PCI bus
0xD8000-0xDBFFF	PCI bus
0xDC000-0xDFFFF	PCI bus
0xE0000-0xE3FFF	PCI bus
0xE4000-0xE7FFF	PCI bus
0xDFA00000-0xFEAFFFFF	PCI bus
0xDFA00000-0xFEAFFFFF	Motherboard resources
0xF7E20000-0xF7E2FFFF	Universal Serial Bus (USB) Controller
0xFED40000-0xFED44FFF	System board
0x20000000-0x201FFFFF	System board
0x40004000-0x40004FFF	System board
0xFED1C000-0xFED1FFFF	Motherboard resources
0xFED10000-0xFED17FFF	Motherboard resources
0xFED18000-0xFED18FFF	Motherboard resources
0xFED19000-0xFED19FFF	Motherboard resources

Address	Device Description
0xF8000000-0xFBFFFFFF	Motherboard resources
0xFED20000-0xFED3FFFF	Motherboard resources
0xFED90000-0xFED93FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFEE00000-0xFEEFFFFF	Motherboard resources
0xF7E3B000-0xF7E3B00F	PCI Simple Communications Controller
0xF7E39000-0xF7E39FFF	PCI Serial Port
0xF7800000-0xF7BFFFFF	Standard VGA Graphics Adapter
0xE0000000-0xEFFFFFFF	Standard VGA Graphics Adapter

Appendix E. Direct Memory Access

Resource	Device
Channel 4	Direct memory access controller

Appendix F. Watchdog Timer (WDT) Setting

WDT is widely used for industrial application to monitor CPU activities. The application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT timeout, the functional normal system will reload the WDT. The WDT never time-out for a normal system. The WDT will not be reloaded by an abnormal system, then WDT will time-out and auto-reset the system to avoid abnormal operation.

This computer supports 255 levels watchdog timer by software programming I/O ports.

Below is an assembly program example to disable and load WDT.

Sample Codes:

```
/*----- Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

#define SIO_INDEX       0x2E            /* or index = 0x4E */
#define SIO_DATA        0x2F            /* or data  = 0x4F */

/*----- routing, sub-routing -----*/
void main()
{
        outportb(sioIndex, 0x87);               /* SIO - Enable */
        outportb(sioIndex, 0x87);

        outportb(sioIndex, 0x07);               /* LDN - WDT */
        outportb(sioData,  0x07);

        outportb(sioIndex, 0x30);               /* WDT - Enable */
        outportb(sioData,  0x01);

        outportb(sioIndex, 0xF0);               /* WDOUT_EN */
        outportb(sioData,  0x80);

        outportb(sioIndex, 0xF6);               /* WDT - Timeout Value */
        outportb(sioData,  0x05);

        outportb(sioIndex, 0xF5);               /* WDT - Configuration */
        outportb(sioData,  0x72);

        outportb(sioIndex, 0xAA);               /* SIO - Disable */
}
```

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