EmCORE-i55M0

3.5" Compact Board

User's Manual

Version 1.2

2012.11

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Contents

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Chapter 1

Introduction

1.1 Copyright Notice

The information in this document is subject to changing without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

1.2 Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

> Warning
> This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:
This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.
The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.
ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

1.3 About this User's Manual

This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this User's Manual, please consult your vendor before further handling.

1.4 Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

1.5 Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

1.6 Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

http://www.arbor.com.tw
E-mail: info@arbor.com.tw

1.7 Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

1.8 Packing List

Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

	1 x EmCORE-i55M0 3.5" Compact Board with heat sink
	1 x Driver CD
	1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

1.9 Ordering Information

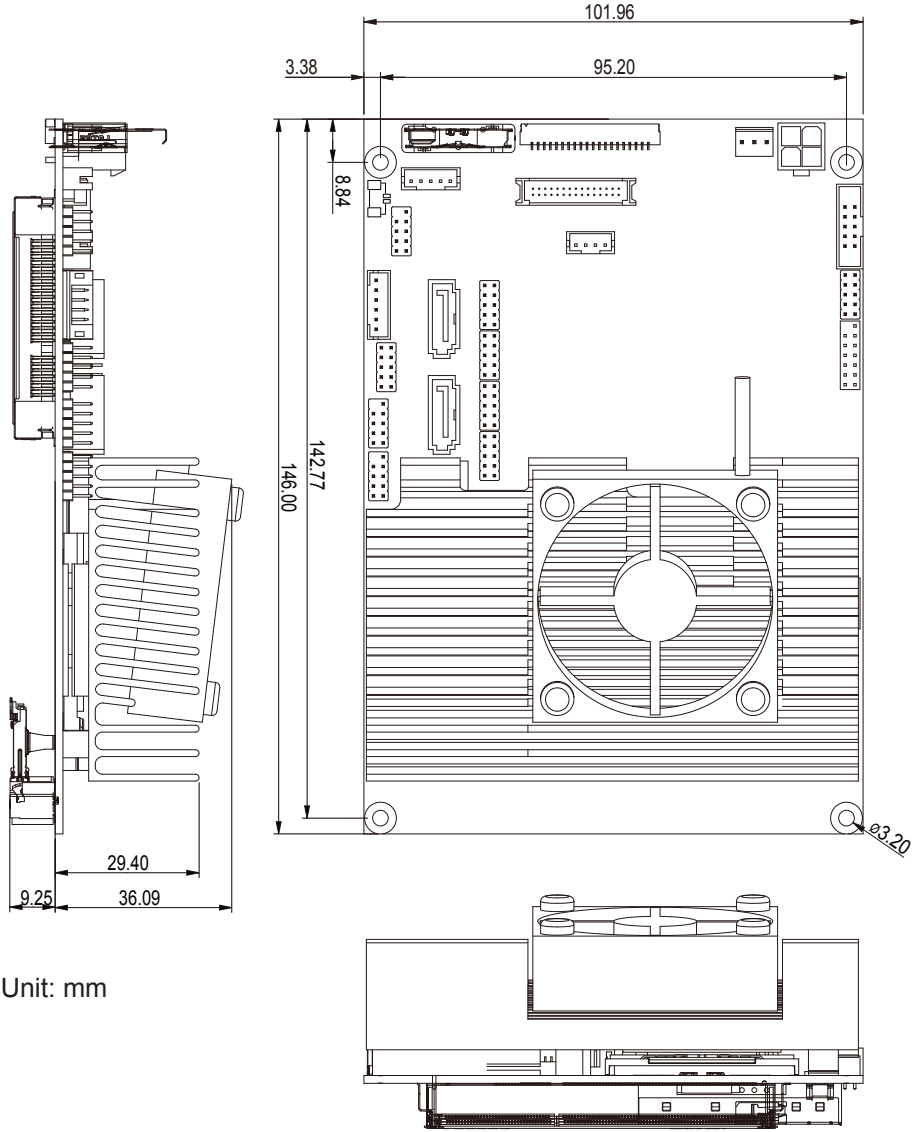
EmCORE-i55M0	Socket-G Intel® i7/i5/ Celeron® 3.5" Compact Board
FCDB-1424	DisplayPort daughter board
FCDB-349R	Digital IO daughter board
CBK-12-57M0-00	Cable Kit 2 x USB cables 1 x Audio cable 1 x PS/2 keyboard & mouse Y-cable 2 x SATA cables 1 x VGA cable 1 x GbE Ethernet cable 4 x COM port cables

1.10 Specifications

Form Factor	3.5” Compact Board
CPU	Socket-G rPGA988A supports Intel® i7-620M at 2.66GHz/ i5-520M at 2.40GHz/ Celeron P4500 at 1.86GHz Processor
Chipset	Intel® PCH HM55
System Memory	1 x 204-pin SO-DIMM socket supporting up to 4GB DDR3 1066/800MHz SDRAM (Bottom side)
Display	Integrated Intel® HD Graphics Controller fifth generation graphic core supporting 24-bit dual channels LVDS/ DisplayPort/ Analog RGB
Ethernet	1 x Intel® 82583V PCIe Gigabit Ethernet controller
I/O Chips	Fintek F71869ED
BIOS	AMI PnP Flash BIOS
Audio	Realtek ALC662 HD Audio CODEC, MIC-in/ Line-In/ Line-Out
Storage	2 x Serial ATA ports with 300MB/s HDD transfer rate 1 x CFast socket
Serial Port	4 x COM ports (COM1, COM3, COM4: RS-232, COM2: RS-232/422/485 selectable)
Keyboard & Mouse	One 6-pin wafer connector (PS/2 interface Keyboard and Mouse via cable)
Universal Serial Bus	4 x USB 2.0 ports
Expansion Interface	LPC interface connector
Operation Temp.	-20ºC ~ 70ºC (-4ºF ~ 158ºF)
Watchdog Timer	1~255 levels Reset
Dimension (L x W)	146 x 102 mm (5.7 ” x 4.0 ”)

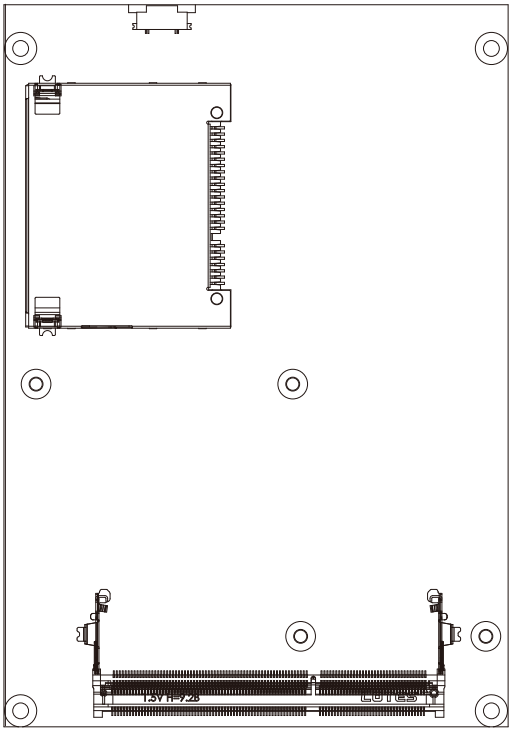
1.11 Board Dimensions

Top View



Unit: mm

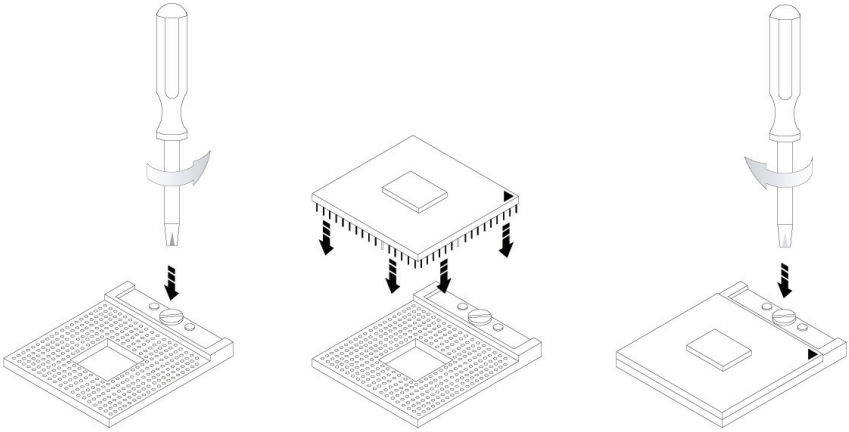
Bottom View



1.12 Installing the CPU

The processor socket comes with a screw to secure the CPU. As showing in the picture as bellow, loose the screw first before inserting the CPU.

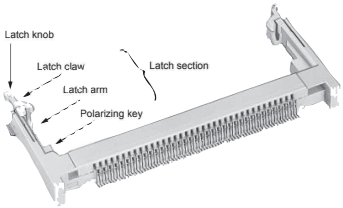
Place the CPU into the socket by making sure the notch on the corner of the CPU corresponding with the notch on the inside of the socket. Once the CPU has slided into the socket, lock the screw.

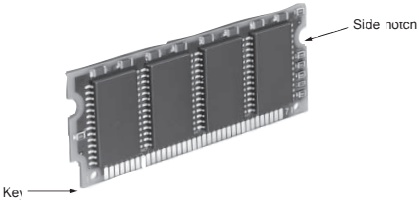


Make sure that heat sink of the CPU top surface is in complete contact to avoid the CPU overheating problem.

If not, it would cause your system or CPU to be hanged, unstable, or damaged.

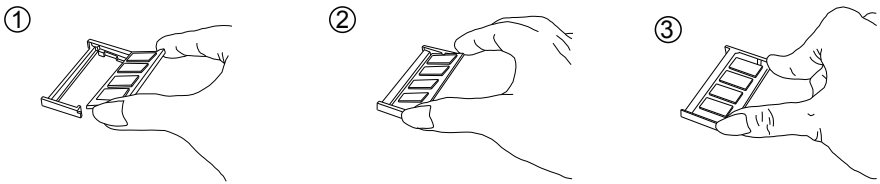
1.13 Installing the Memory





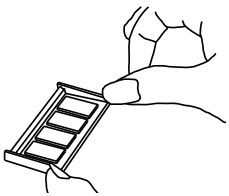
To install the Memory module, locate the Memory SO-DIMM slot on the board and perform as below:

1. Adjust the socket polarizing key and the board key to the same direction.
2. Insert the board obliquely. Moreover, lay the board in parallel to the opening at angle of 20^{o} to 30^{o}, and softly insert the board so as to hit the socket bottom. Stopping insertion halfway will result in improper insertion.
3. Applying the board side notch in parallel to the socket bottom so that the board position cannot be displaced, press the board side notch up, and fix it to the latch portion at both socket edges. Press the board side notch, and release the notch with a snap “click” tone, if the printed board exceeds the latch claw head.



Procedures for board extraction

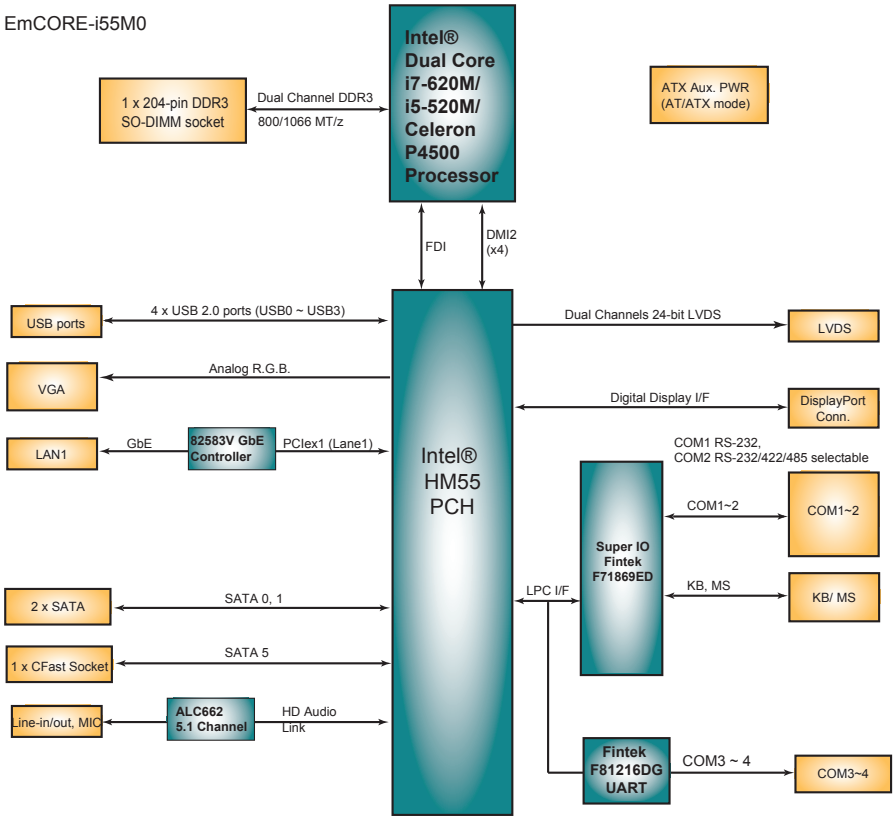
Apply the thumb nail to the latch knob at both socket edges. Forcibly widen the latch knobs to right and left ways, and release the latch. Then draw the board out along an angle where the board is raised.



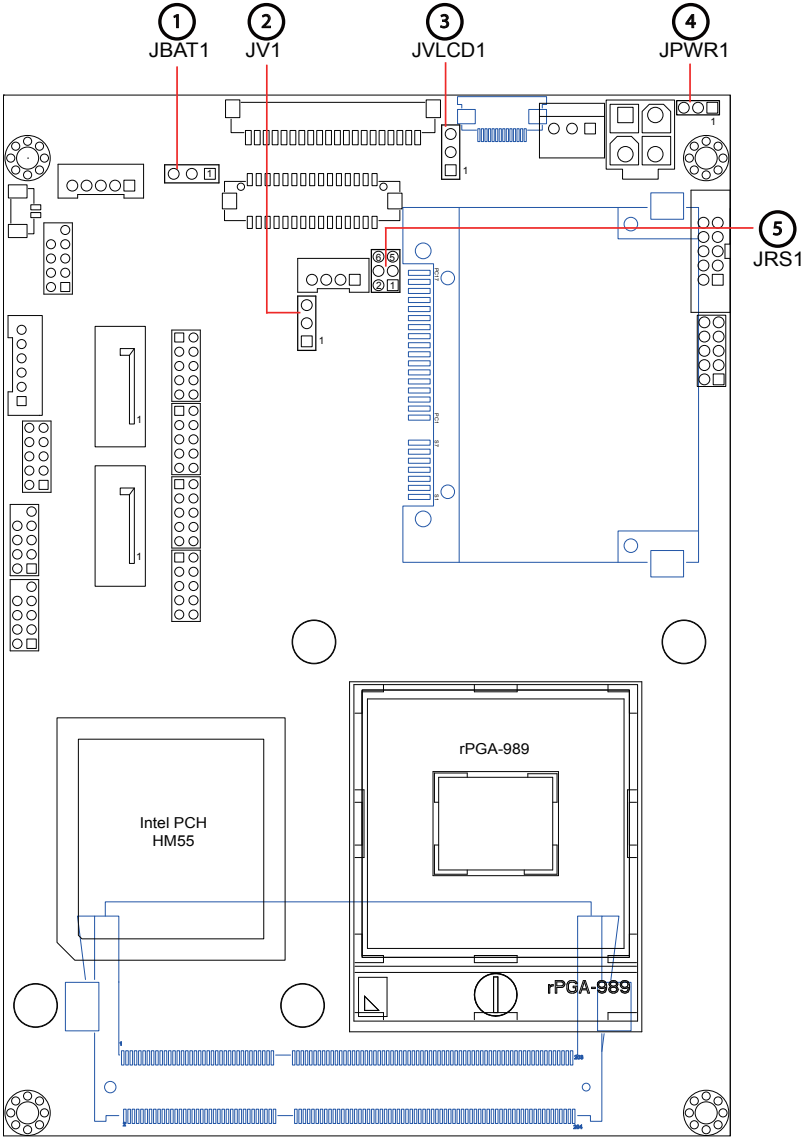
Chapter 2

Installation

2.1 Block Diagram



2.2 Jumpers


1
JBAT1
2
JV1
3
JVLCD1
4
JPWR1
5
JRS1
Intel PCH
HM55
rPGA-989
rPGA-989

JBAT1: Clear CMOS Setting (1)

If the board refuses to boot due to inappropriate CMOS settings here is how to proceed to clear (reset) the CMOS to its default values.
Connector type: 2.54mm pitch 1x3-pin headers

Pin	Mode	
1-2	Keep CMOS (Default)	
2-3	Clear CMOS	

You may need to clear the CMOS if your system cannot boot up because you forgot your password, the CPU clock setup is incorrect, or the CMOS settings need to be reset to default values after the system BIOS has been updated. Refer to the following solutions to reset your CMOS setting:

Solution A:

1. Power off the system and disconnect the power cable.
2. Place a shunt to short pin 2 and pin 3 of JBAT1 for five seconds.
3. Place the shunt back to pin 1 and pin 2 of JBAT1.
4. Power on the system.

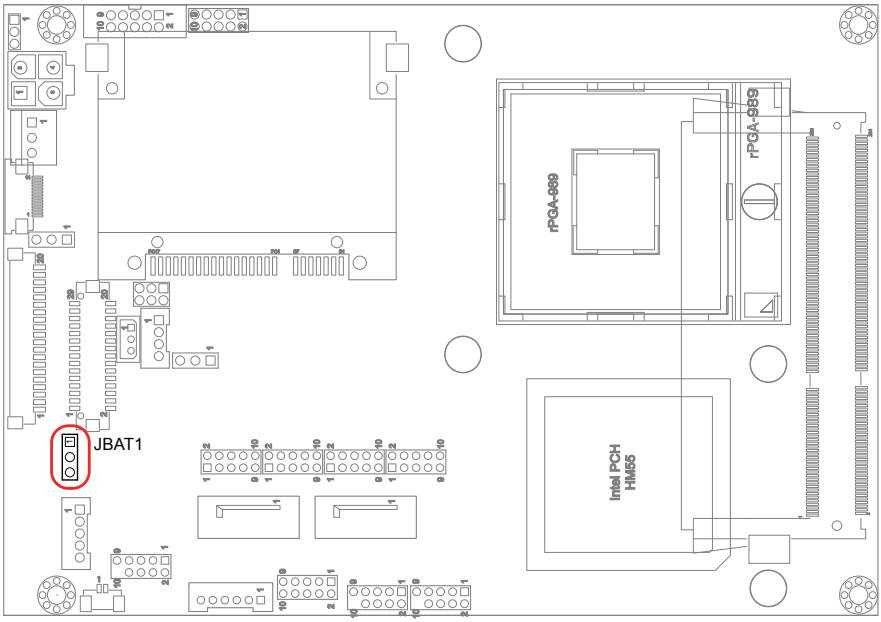
Solution B:

If the CPU Clock setup is incorrect, you may not be able to boot up. In this case, follow these instructions:

1. Turn the system off, then on again. The CPU will automatically boot up using standard parameters.
2. As the system boots, enter BIOS and set up the CPU clock.

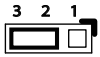
Note:

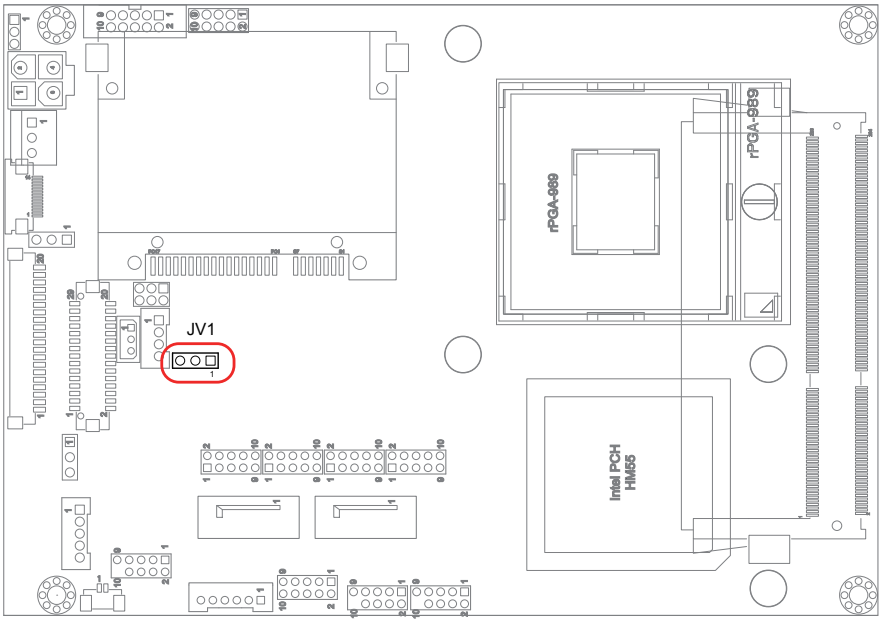
If you are unable to enter BIOS setup, turn the system on and off a few times.


JBAT1
rPGA-989
rPGA-989
Intel PCH
HM55

JV1: COM1 pin-1 signal setting (2)

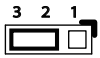
The voltage of pin-1 could be selected by JV1 in +5V or DCD.
Connector type: 2.54 mm pitch 1x3-pin headers

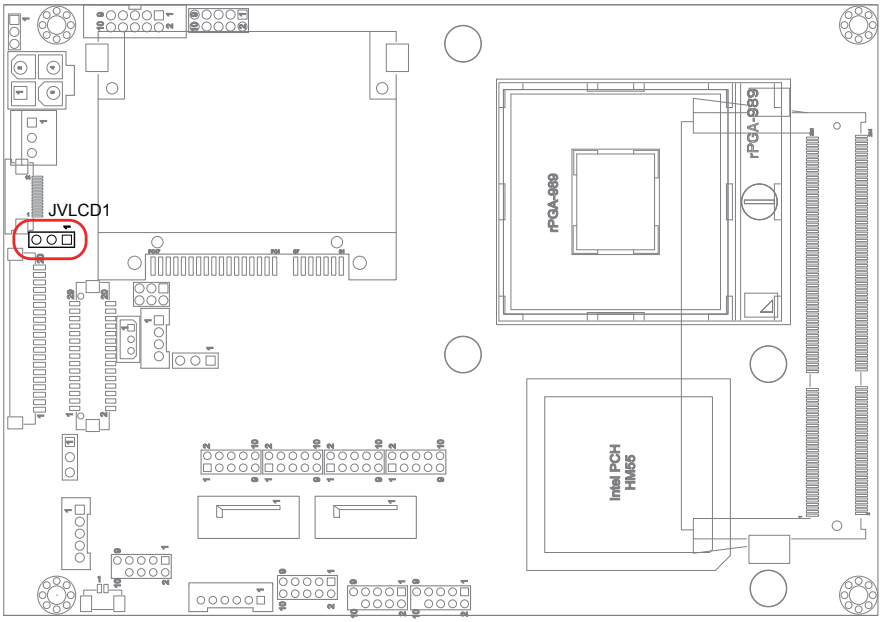
Pin	Voltage	
1-2	+5V	
2-3	DCD (Default)	



JVLCD1: LCD Panel Voltage Selection (3)

The voltage of LCD panel could be selected by JVLCD1 in +5V or +3.3V.
Connector type: 2.54 mm pitch 1x3-pin headers

Pin	Voltage	
1-2	+5V	
2-3	+3.3V (Default)	

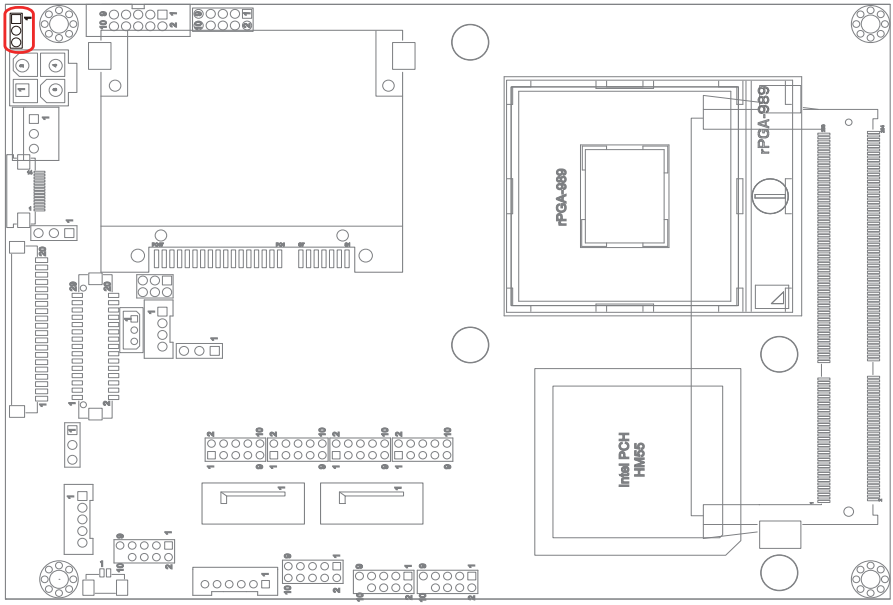


JPWR1: AT/ATX Power Mode Selection (4)

The power mode jumper selects the power mode for the system.
Connector type: 2.00mm pitch 1x3-pin headers.

Pin	Mode	
1-2	ATX Mode (Default)	
2-3	AT Mode	

JPWR1



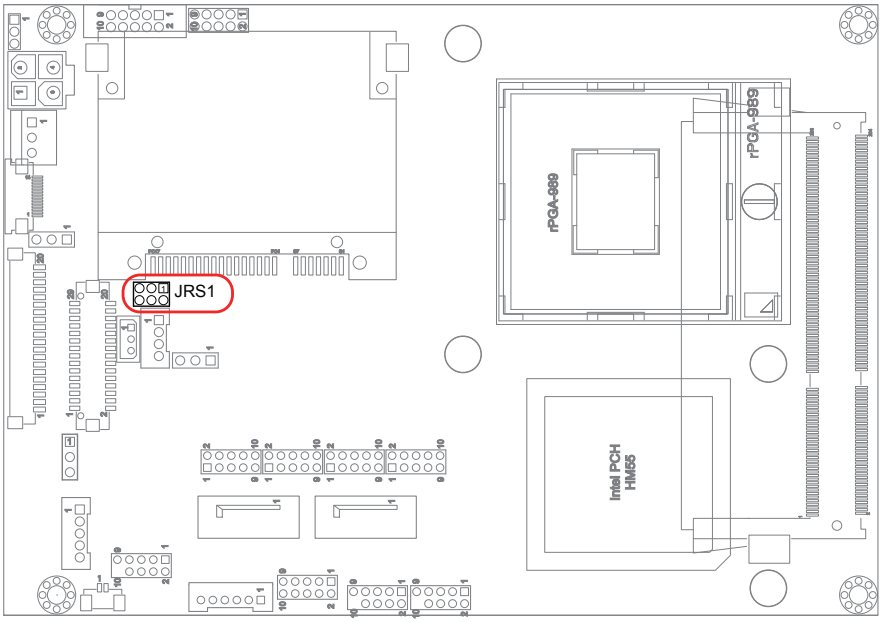
Note:
To activate the ATX power mode, you must turn on the power button switch first (the connector for power button switch is located in JFRT1).

JRS1: COM2 RS-232/422/485 Mode Selection (5)

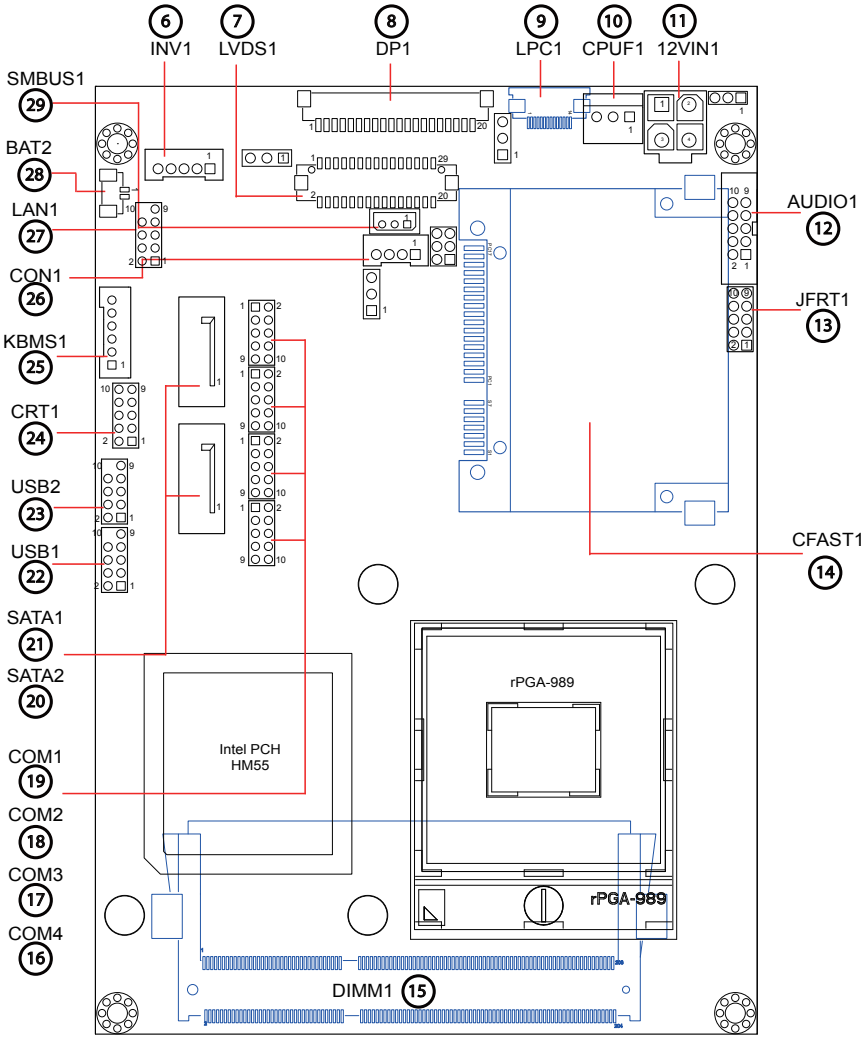
The onboard COM2 port can be configured to operate in RS-422 or RS-485 modes. RS-422 modes differ in the way RX/TX is being handled. Jumper JRS1 switches between RS-232 or RS-422/485 mode. All RS-232/422/482 modes are available on COM2.

Connector type: 2.00mm pitch 2x3-pin headers.

Mode	RS-232 (Default)	RS-422	RS-485
1-2	Short	Open	Open
3-4	Open	Short	Open
5-6	Open	Open	Short
			



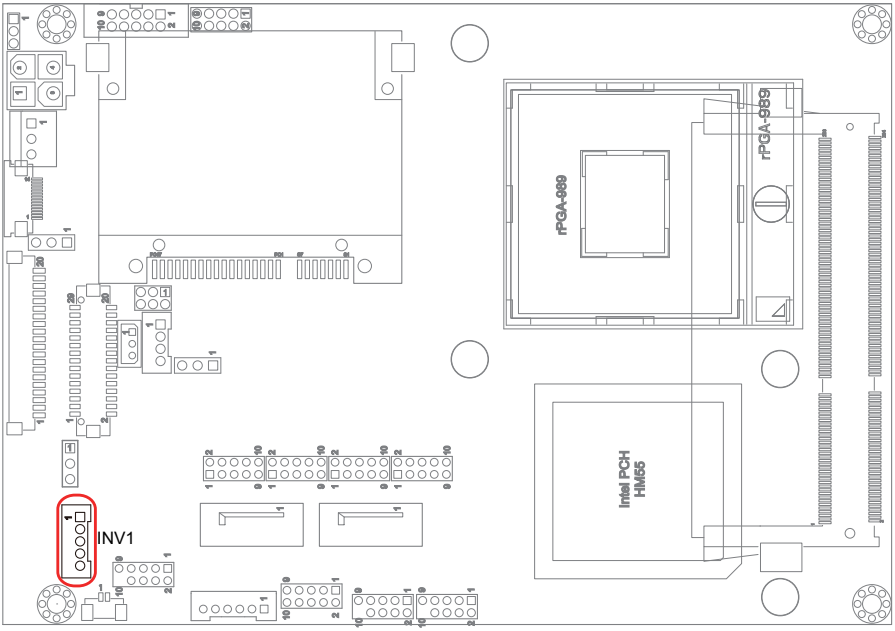
2.3 Connectors



INV1: LCD Inverter Connector (6)

Connector type: 2.00mm pitch 1x5-pin box wafer connector.

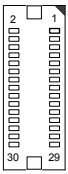
Pin	Description
1	INV_VCC12
2	GND
3	Backlight on
4	Brightness control
5	GND

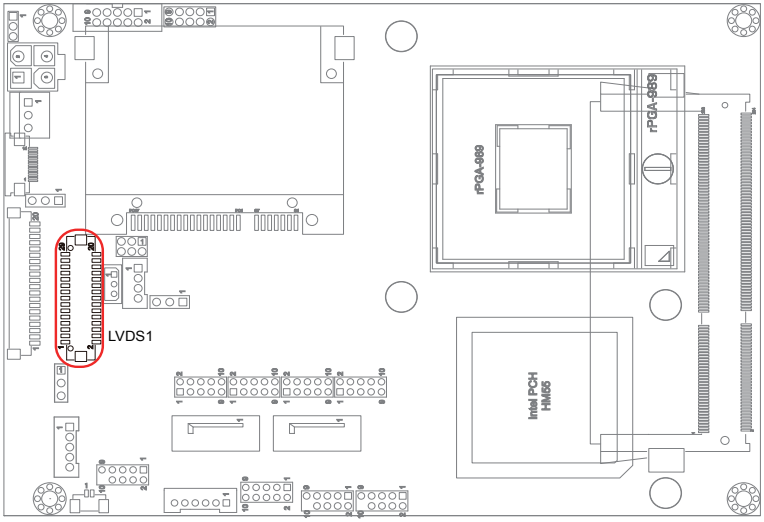


LVDS1: LVDS LCD Connector (7)

Connector type: ACES 1.25mm 87209-304*-06 connector and supports 24-bit dual channels.

Pin	Desc.	Pin	Desc.
2	VDD	1	VDD
4	TX2CLK+	3	TX1CLK+
6	TX2CLK-	5	TX1CLK-
8	GND	7	GND
10	TX2D0+	9	TX1D0+
12	TX2D0-	11	TX1D0-
14	GND	13	GND
16	TX2D1+	15	TX1D1+
18	TX2D1-	17	TX1D1-
20	GND	19	GND
22	TX2D2+	21	TX1D2+
24	TX2D2-	23	TX1D2-
26	GND	25	GND
28	TX2D3+	27	TX1D3+
30	TX2D3-	29	TX1D3-

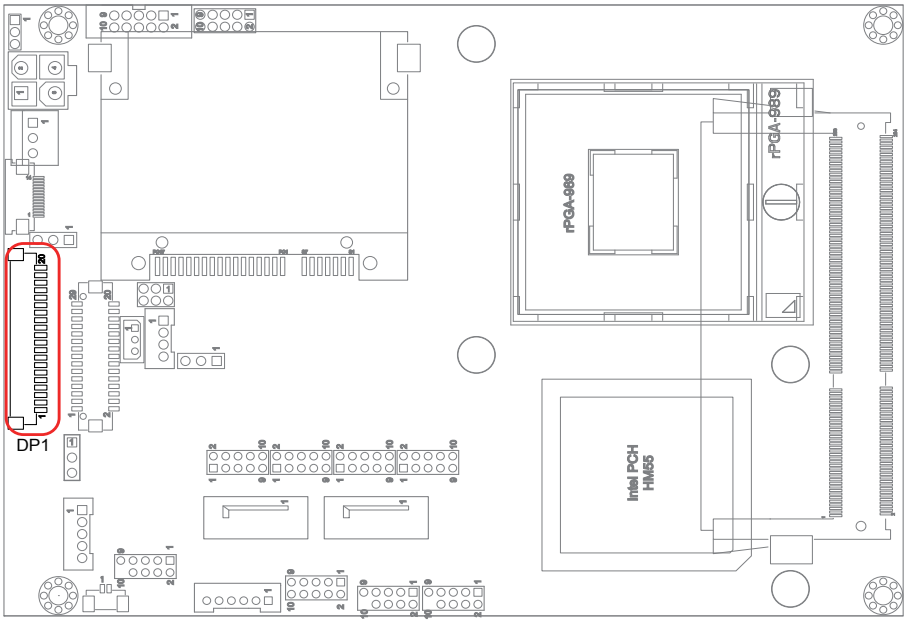




DP1: DisplayPort Connector (8)

Connector type: ACES 1.25mm 87209-304*-06 connector.

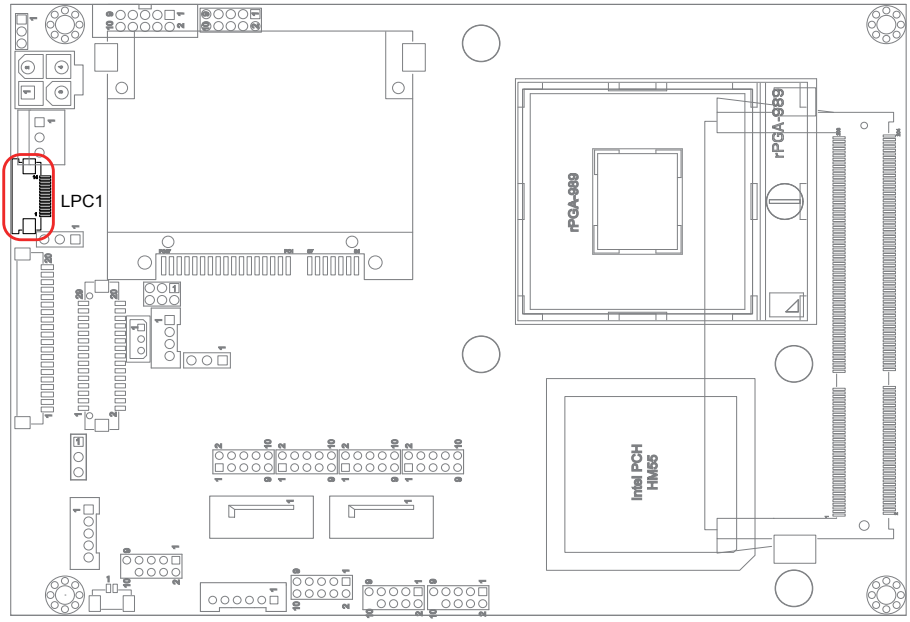
Pin	Desc.	Pin	Desc.
1	LANE_0P	11	LANE_3N
2	LANE_0N	12	GND
3	GND	13	CONF1
4	LANE_1P	14	CONF2
5	LANE_1N	15	AUXP
6	GND	16	AUXN
7	LANE_2P	17	GND
8	LANE_2N	18	HPD
9	GND	19	RTN_PWR
10	LANE_3P	20	PWR(3.3V)



LPC1: Low Pin Count Connector (9)

Connector type: CVILUX 0.5mm CF20141U0*0-LF connector.

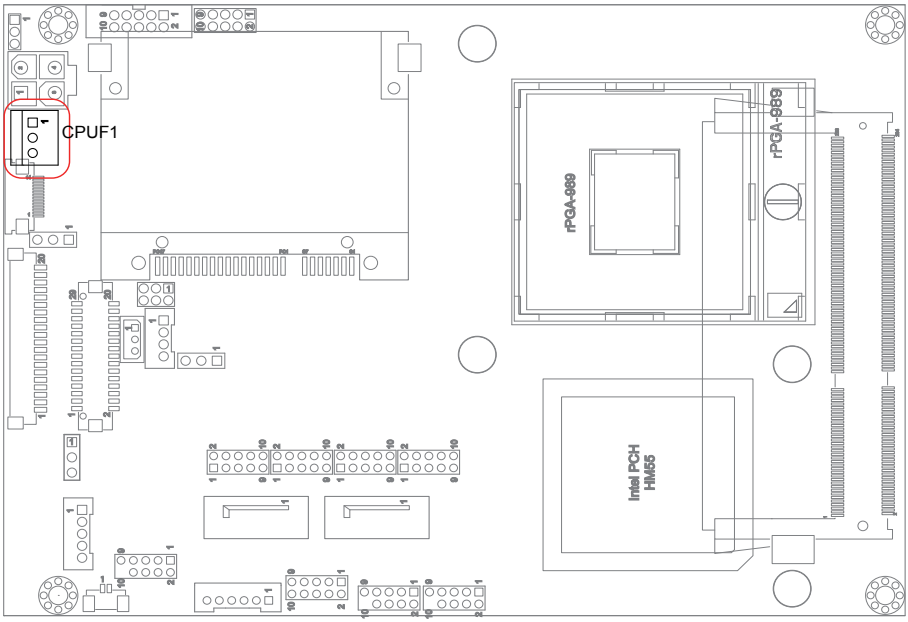
Pin	Desc.	Pin	Desc.
1	LPC_D0	8	LPC_RST#
2	LPC_D1	9	GND
3	LPC_D2	10	LPC_ CLK_33Mhz
4	LPC_D3	11	GND
5	GND	12	GND
6	LPC_FRAME#	13	+3.3V
7	SERIRQ	14	+3.3V



CPUF1: Fan Power Connector (10)

CPUF1 is a 3-pin headers for the CPU fan. The fan must be a +12V fan.

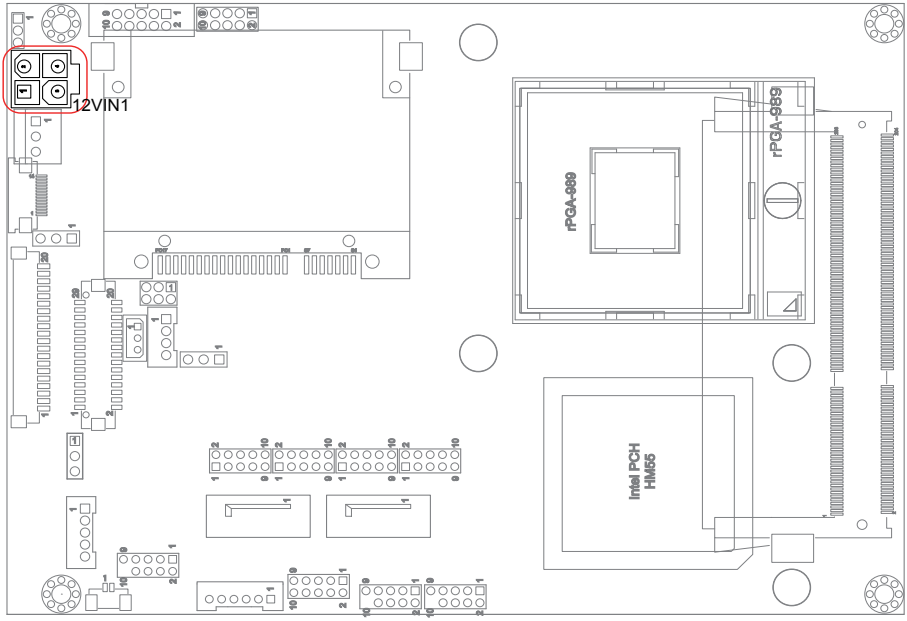
Pin	Description
1	GND
2	+12V
3	FAN_Detect



12VIN1: ATX +12V Connector (11)

PWR1 supplies ATX +12V (Vcore).

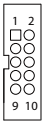
Pin	Description	Pin	Description
2	GND	4	+12V
1	GND	3	+12V

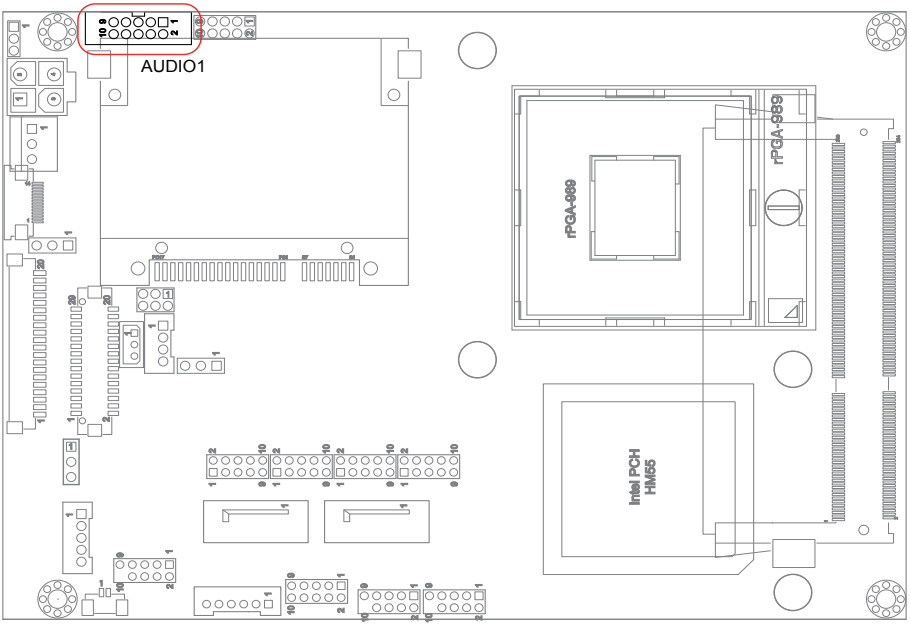


AUDIO1: Audio Connector (12)

Connector type: 2.00mm pitch 2x5-pin box headers.

Pin	Description	Pin	Description
1	Line Left In	2	Line Right In
3	GND	4	GND
5	MIC_L	6	MIC_R
7	GND	8	GND
9	Line-out Left	10	Line-out Right

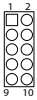


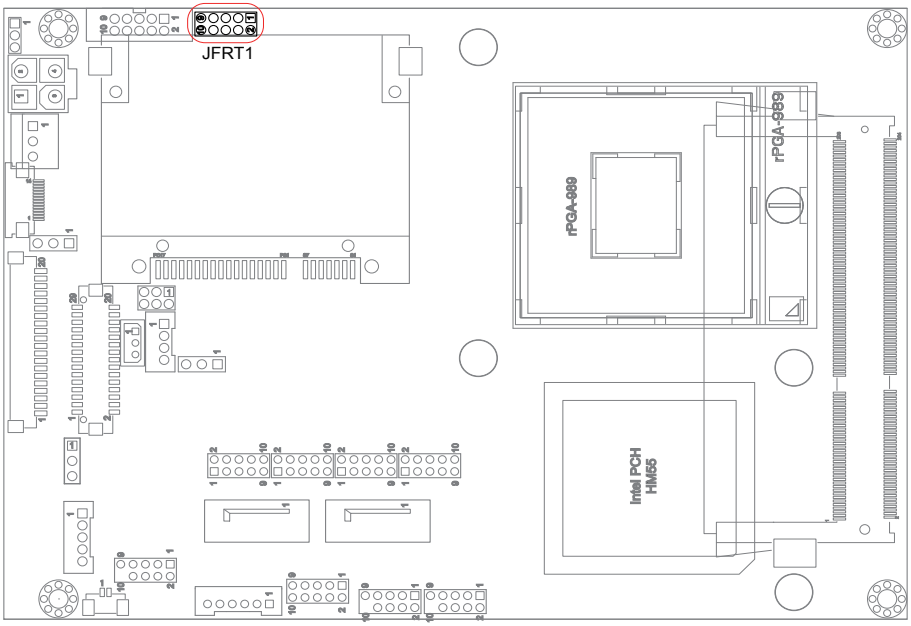


JFRT1: Switches and Indicators (13)

It provides connectors for system indicators that provides light indication of the computer activities and switches to change the computer status.
Connector type: 2.00mm pitch 2x5-pin headers.

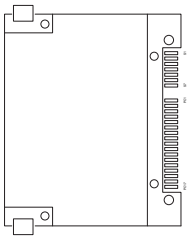
Pin	Description	Pin	Description
1	RESET+	2	RESET-
3	POWER_LED+	4	POWER_LED-
5	HDD_LED+	6	HDD_LED-
7	SPEAKER+	8	SPEAKER-
9	PSON+	10	PSON-

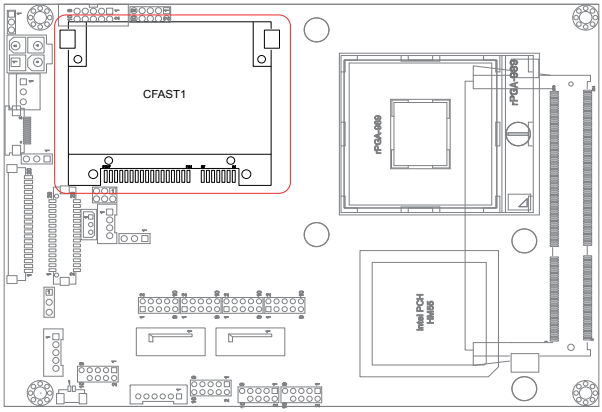




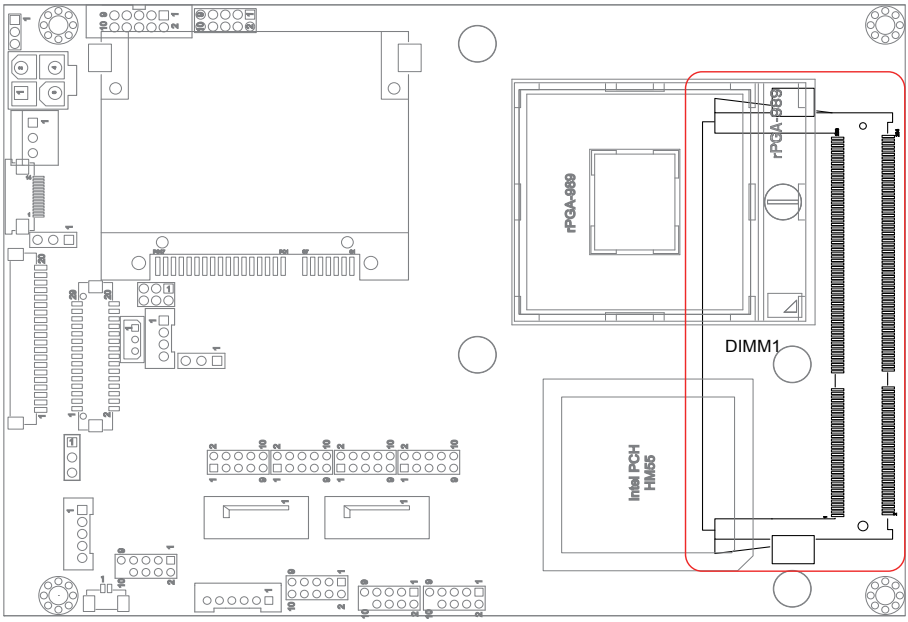
CFAST1: CFAST Socket (14, bottom side)

Pin	Desc.
S1	SGND1
S2	TXP
S3	TXN
S4	SGND2
S5	RXN
S6	RXP
S7	SGND
PC1	CDI
PC2	GND
PC3	TBD
PC4	TBD
PC5	TBD
PC6	TBD
PC7	GND
PC8	LED1
PC9	LED2
PC10	IO1
PC11	IO2
PC12	IO3
PC13	3.3V
PC14	3.3V
PC15	GND
PC16	GND
PC17	CD0





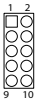
DIMM1: SO-DIMM Socket (15, bottom side)

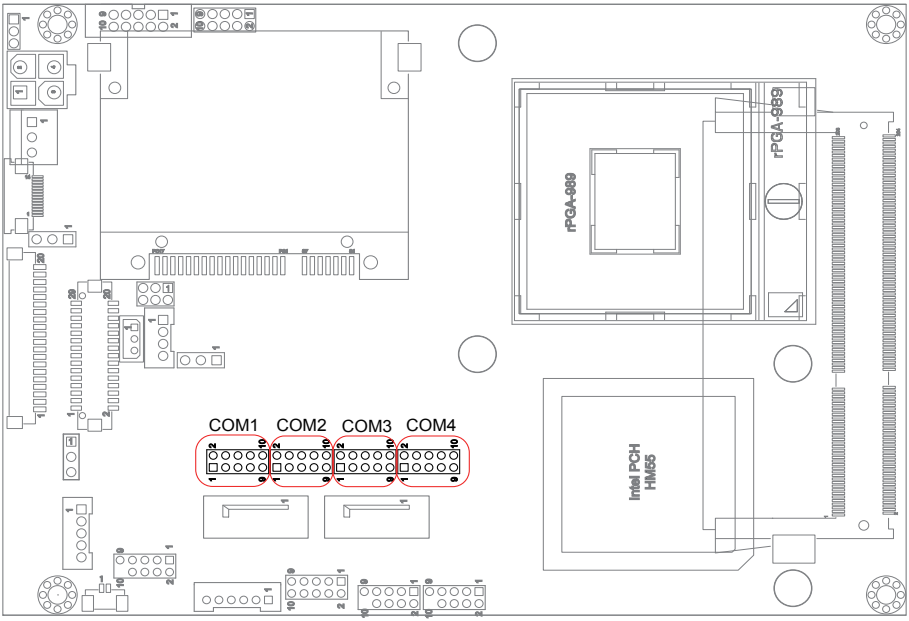


COM1~4: Serial Port Connectors (16, 17, 18, 19)

Connector type: 2.00mm pitch 2x5-pin headers.

Pin	Description	Pin	Description
1	DCD#	2	RXD
3	TXD	4	DTR#
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	N/C

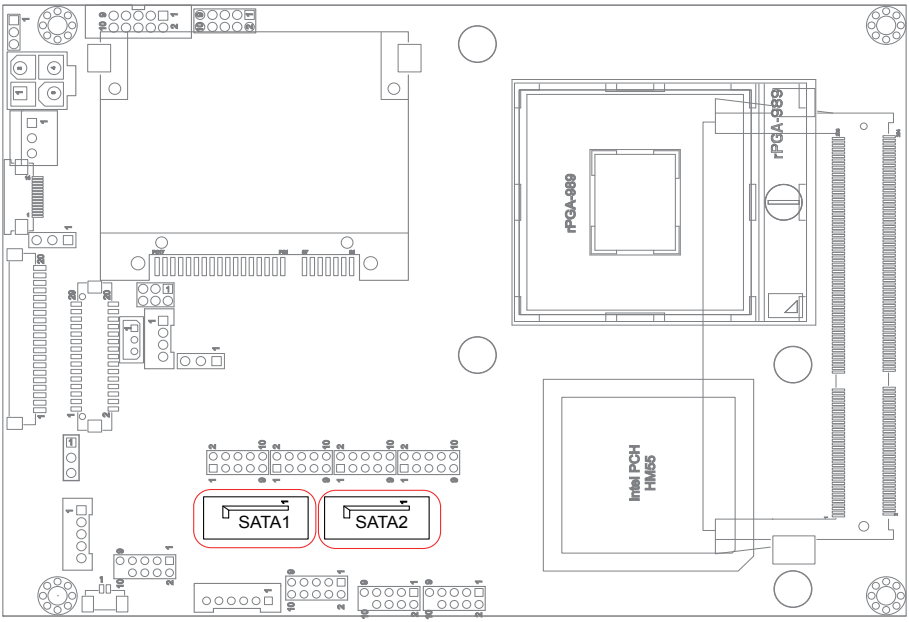




SATA1~2: Serial ATA Connectors (20, 21)

High speed transfer rates (300MB/s).

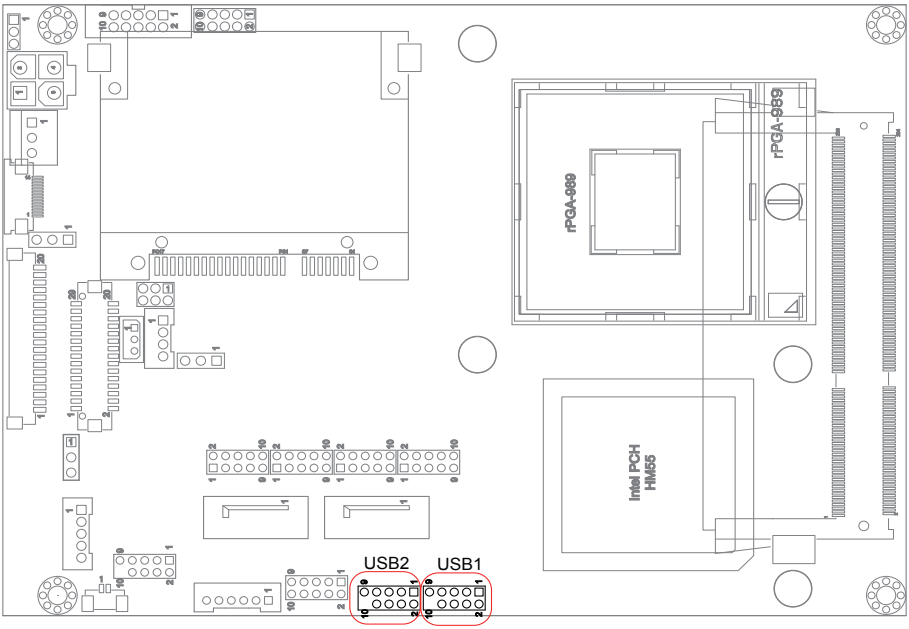
Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND



USB1~2: USB Connectors (22, 23)

Connector type: 2.00mm pitch 2x5-pin headers.

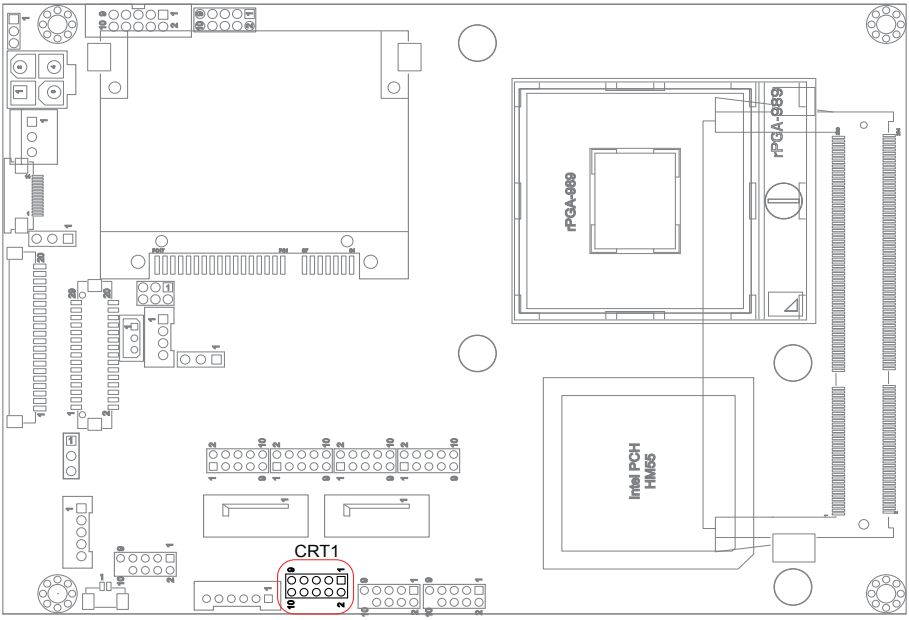
Pin	Description	Pin	Description
1	+5V	2	+5V
3	USBD-	4	USBD-
5	USBD+	6	USBD+
7	GND	8	GND
9	GND	10	N/C (Key)



CRT1: Analog RGB Connector (24)

Connector type: 2.00mm pitch 2x5-pin headers.

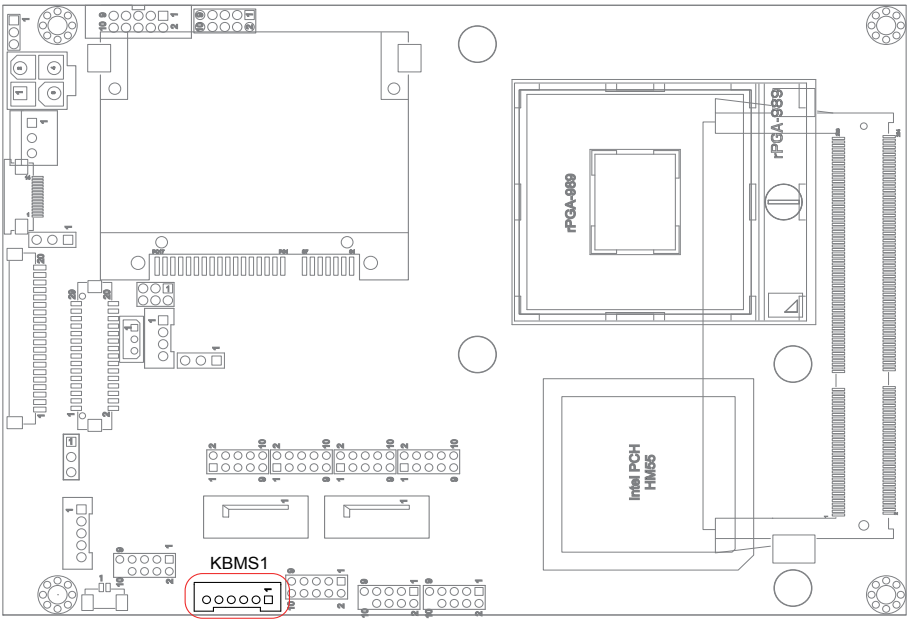
Pin	Description	Pin	Description
1	RED	2	GND
3	GREEN	4	GND
5	BLUE	6	GND
7	H_SYNC	8	GND
9	V_SYNC	10	CRT_DET



KBMS1: Keyboard & Mouse Connector (25)

Connector type: 2.0mm pitch 1x6-pin box wafer connector.

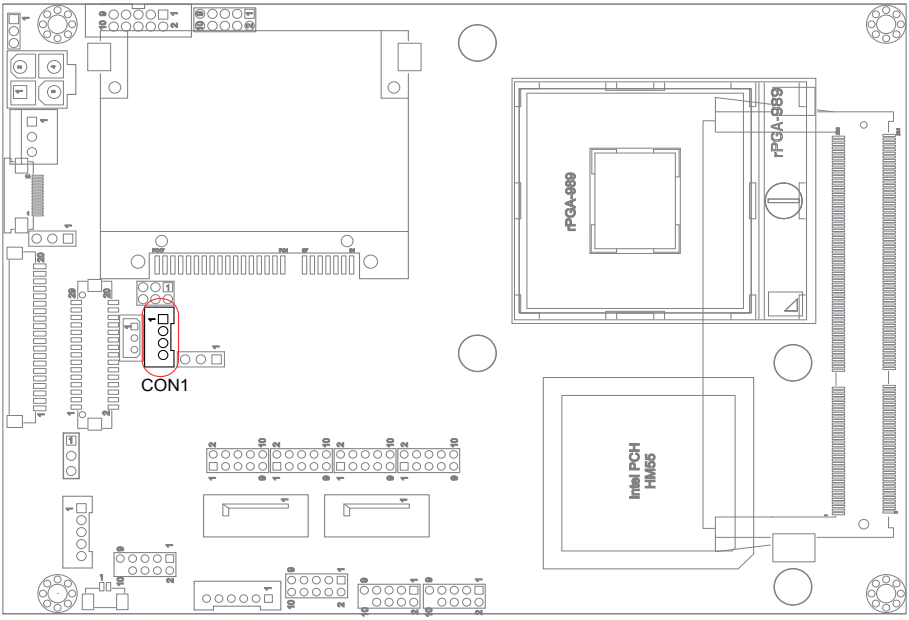
Pin	Description
1	KB_DAT
2	GND
3	MS_DAT
4	KB_CLK
5	VCC
6	MS_CLK



CON1: RS-422/485 Output Connector (26)

Connector type: 2.00mm pitch 1x4-pin box wafer connector.

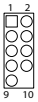
Pin	RS-422	Pin	RS-485
1	TX+	1	DATA+
2	TX-	2	DATA-
3	RX+	3	N/C
4	RX-	4	N/C

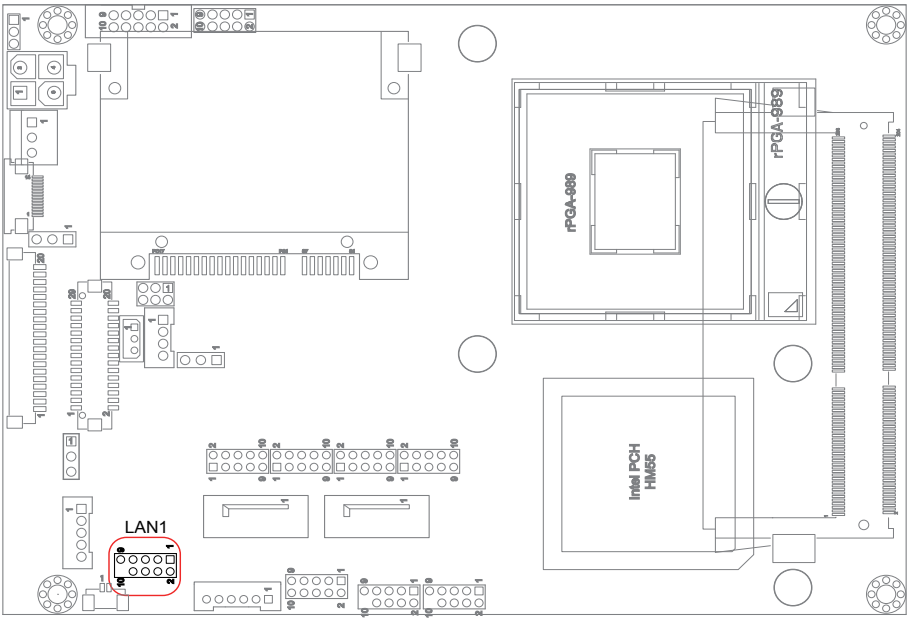


LAN1: GbE Connector (27)

Connector type: 2.00mm pitch 2x5-pin headers.

Pin	Description	Pin	Description
1	TX+/ MDI0+	2	TX/ MDI0-
3	RX+/ MDI1+	4	N/C/ MDI2+
5	N/C/ MDI2-	6	RX-/ MDI1-
7	N/C/ MDI3+	8	N/C/ MDI3-
9	N/C	10	N/C (Key)

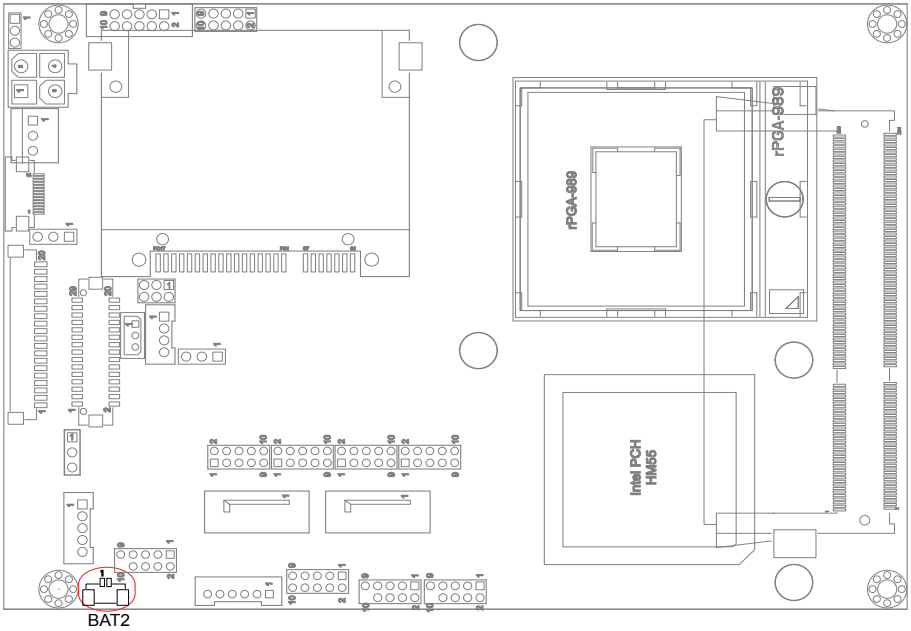




BAT2: External Battery connector (28, Optional)

Connector type: 1.25mm pitch 1x2-pin wafer connector.

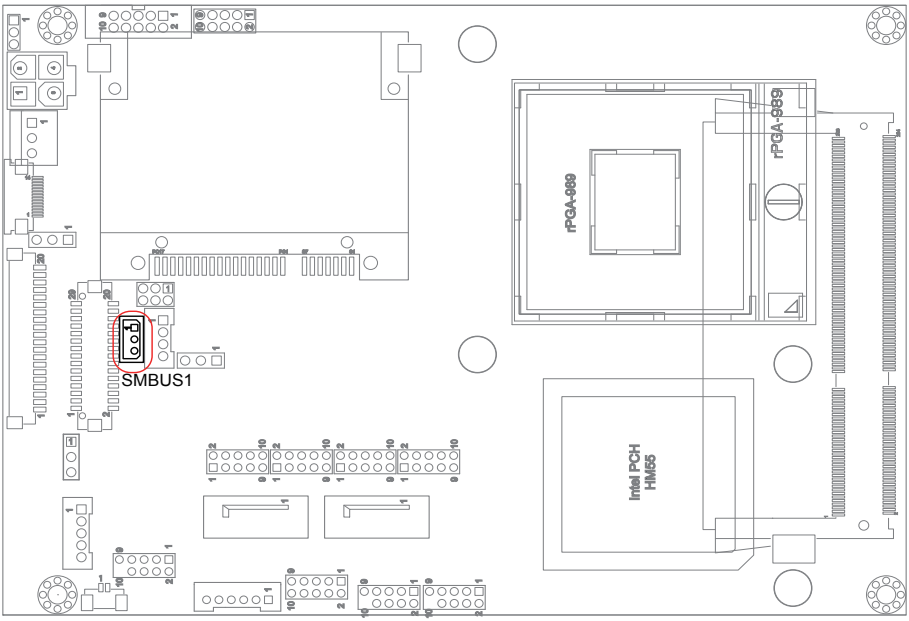
Pin	Description
1	GND
2	3.3 V battery



SMBUS1: External SMBus Connector (29)

Connector type: 2.5mm pitch 1x3-pin box wafer connector.

Pin	Description
1	Data
2	Clock
3	GND



2.4 The Installation Paths of CD Driver

Windows XP

Driver	Path
Management Engine	\ME
CHIPSET	\CHIPSET\INTEL\INF 9.11
NET Framework	\NET Framework
VGA	\GRAPHICS\WINXP_32_14425 \GRAPHICS\WINXP_64_14425
LAN	\ETHERNET\INTEL\82583V\32 \ETHERNET\INTEL\82583V\64
AUDIO	\AUDIO\REALTEK_HD\XP_WDM_R255

Windows 7

Driver	Path
Management Engine	\ME
CHIPSET	\CHIPSET\INTEL\INF 9.11
VGA	\GRAPHICS\Win7_32_15179 \GRAPHICS\Win7_64_15179
LAN	\ETHERNET\INTEL\82583V\32 \ETHERNET\INTEL\82583V\64
AUDIO	\AUDIO\REALTEK_HD\Win7_R255

Note: Before install the Management Engine driver, please copy the MEI_ALLOS_6.1.0.1042_PV.exe into a writable storage device and then execute the driver from the storage device.

Chapter 3

BIOS

3.1 BIOS Introduction

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility and configurations.

When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILILTY, press “Delete” once the power is turned on.

When the computer is shut down, the battery on the motherboard supplies the power for BIOS RAM.

The Main Setup screen lists the following information

BIOS Information

BIOS Vendor: displays the vendor name

Core Version: displays the current version information of the core

Project Version

Build Date: the date when the project was made/updated

Memory Information: displays the total memory

Access Level: shows user’s access level

Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

"←""→"	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
"↓" "↑"	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and discard changes saved into CMOS (a message screen will display and ask you to select "OK" or "Cancel" for exiting and discarding changes. Use "←" and "→" to select and press "Enter" to confirm) On the Sub Menu – Exit current page and return to main menu
Page Up / +	Increase the numeric value on a selected setup item / make change
Page Down -	Decrease the numeric value on a selected setup item / make change
F2	Recover to previous values in setup
F3	Recover to optimized defaults automatically
F1	Activate "General Help" screen
F10	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select "OK" or "Cancel" for exiting and saving changes. Use "←" and "→" to select and press "Enter" to confirm)

System Date

Set the system date. Note that the "Day" automatically changes when you set the date.

The date format is:
Day : Sun to Sat
Month : 1 to 12
Date : 1 to 31
Year : 1999 to 2099

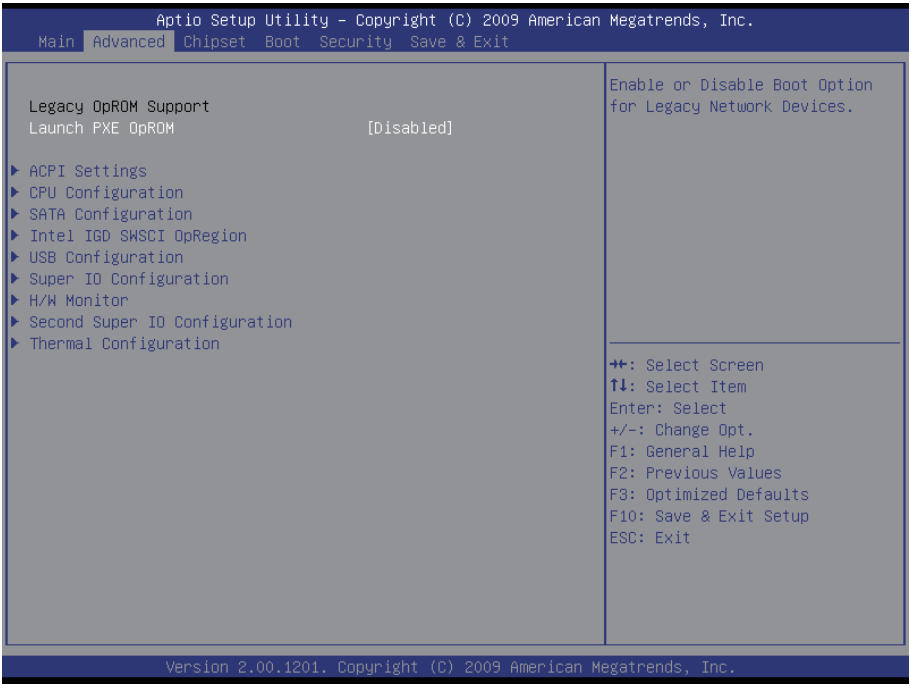
System Time

Set the system time.

The time format is:
Hour : 00 to 23
Minute : 00 to 59
Second : 00 to 59

3.2 Advanced Settings

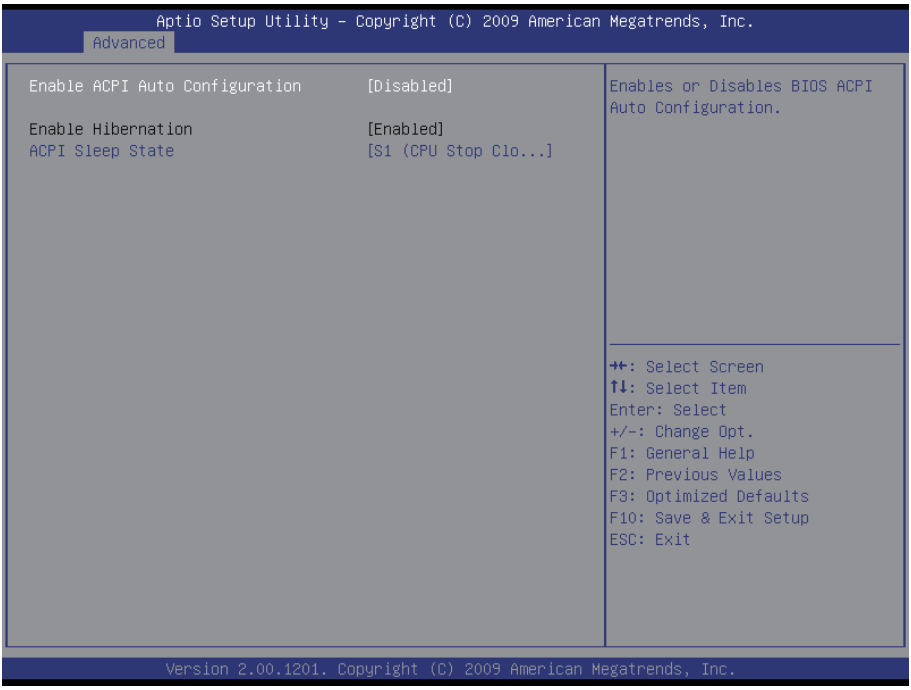
The “Advanced” screen provides setting options to configure ACPI, CPU, SATA, USB, Super IO and other peripherals. You can use “←” and “→” keys to select “Advanced” and use the “↓” and “↑” to select a setup item.



Note: please pay attention to the instructions at the upper-right frame before you decide to configure any setting of an item.

3.2.1 ACPI Settings

Press “Enter” on “ACPI Settings” and you will be able to set up ACPI configuration.



Enable ACPI Auto Configuration

Allow you to enable or disable BIOS ACPI Auto Configuration.

Enable Hibernation

Allow you to enable or disable system hibernation (OS/S4 Sleep State). This option may not be effective in some OSes.

ACPI Sleep State

Provide 3 options, Suspend Disable, S1 (CUP Stop Clock), and S3 (Suspend to RAM) in order. Suspend ranks the highest ACPI sleep state.

3.2.2 CPU Configuration

Press “Enter” on “CPU Configuration” to configure the CPU on the “CPU Configuration” screen.

CPU Details

Detail information including CPU manufacturer name, Processor Speed, Processor Stepping, Microcode Revision, Processor Core number, etc.

Hyper-Threading Technology

Enabled: activates the Hyper-Threading Technology for higher CPU threading speed. (Recommended)
Disabled: deactivates the Hyper-Threading Technology.

Active Processor Cores
Number of cores to enable in each processor package.
The choice: All, 1, 2

Limit CPUID Maximum
Disable for Windows XP.
The choice: Disabled, Enabled

Hardware Prefetcher
To turn on/off the MLC streamer prefetcher.
The choice: Disabled, Enabled

Adjacent Cache Line Prefetch
To turn on/off prefetching of adjacent cache lines.
The choice: Disabled, Enabled

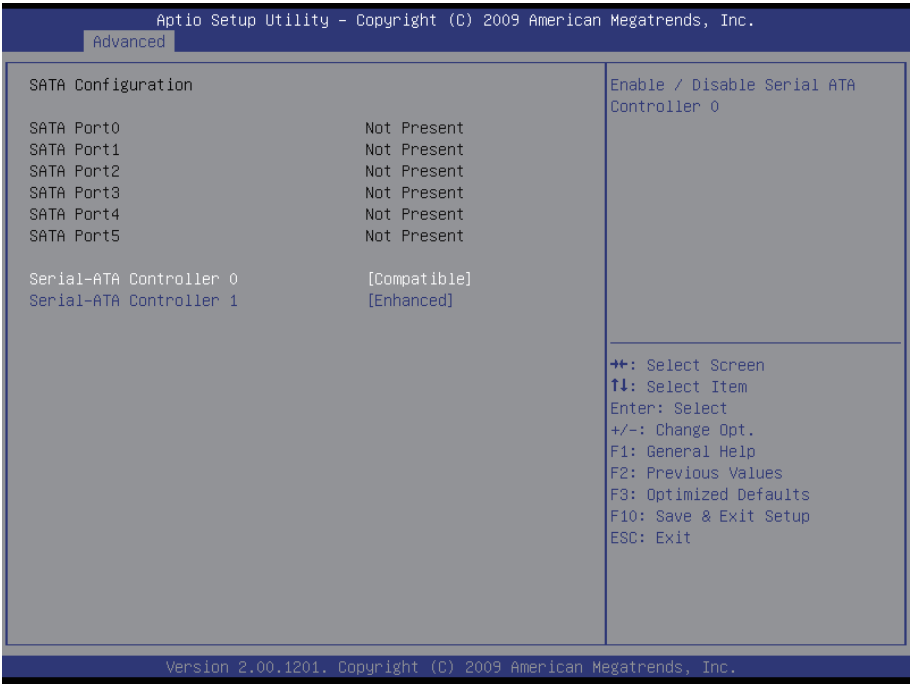
Power Technology
Enable the power management features.
The choice: Disabled, Energy Efficient, Custom

TDC Limit
Turbo-XE Mode Processor TDC Limit in 1/8 A granularity. 0 means using the factory-configured value.

TDP Limit
Turbo-XE Mode Processor TDP Limit in 1/8 A granularity. 0 means using the factory-configured value.

3.2.3 SATA Configuration

It allows you to select the operation mode for SATA controller.



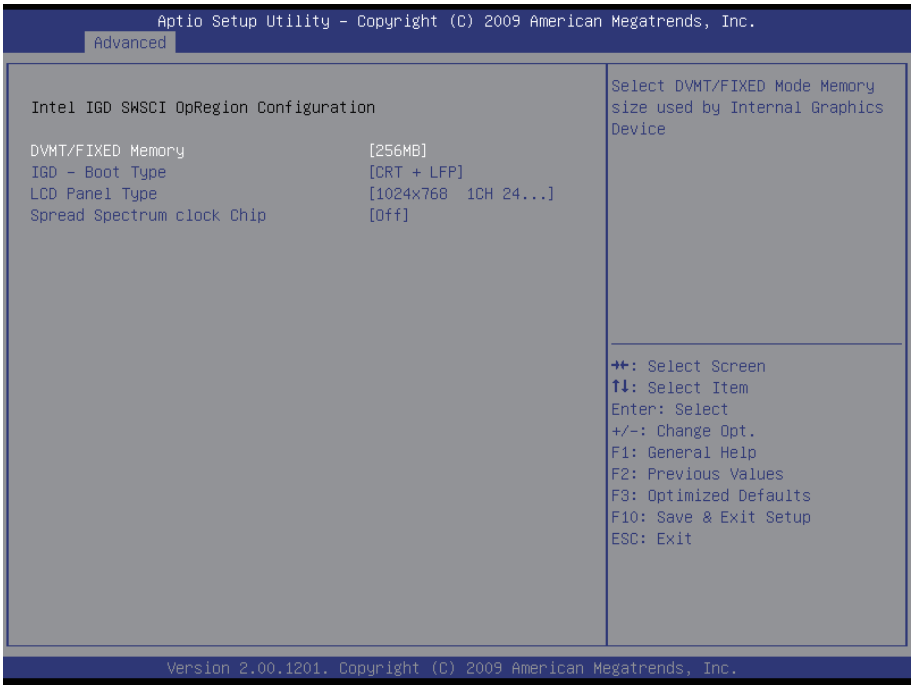
Serial-ATA Controller 0

Enable/ Disable Serial ATA Controller 0.
The choice: Disable, Enhanced, Compatible

Serial-ATA Controller 1

Enable/ Disable Serial ATA Controller 0.
The choice: Disable, Enhanced

3.2.4 Intel IGD SWSCI OpRegion



DVMT/ Fixed Memory

This feature allows you to select the memory size of DVMT/BOTH operating mode.

The choice: 256MB, 128MB, Maximum

IGD – Boot Type

This feature allows you to select the display device when you boot up the system.

The choice: VBIOS Default, CRT, LVDS, CRT+LVDS, DVI, CRT+DVI

LCD Panel Type

This feature allows you to select displayed Panel Resolution in accordance with LCD Panel.

The choice:

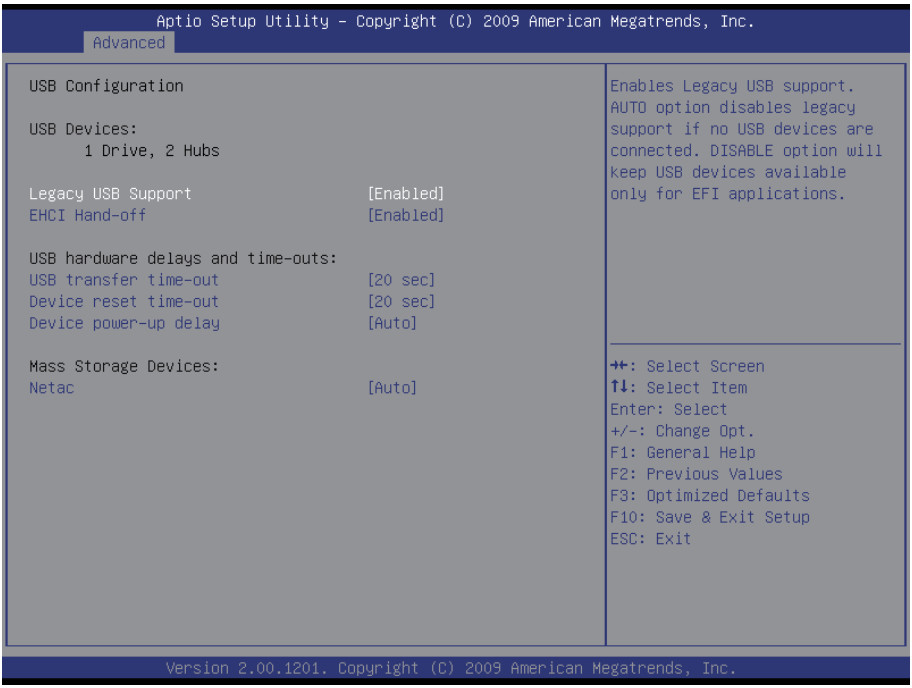
VBIOS Default, 640x480 18/1, 800x600 18/1, 1024x768 18/1, 1280x1024 24/2, 1024x600 18/2, 1400x900 24/2, 1600x1200 18/2, 1280x768 18/1, 1680x1050 24/2, 1920x1080 24/2, 1024x768 24/1, 1366x768 24/1, 800x400 18/1, 1280x800 18/1, 1280x720 24/1, 2048x1536 24/2

Spread Spectrum Clock Chip

Allow you to select Off, Hardware or Software. Hardware uses chip to control spread. Software uses BIOS.

3.2.5 USB Configuration

The menu is used to read USB configuration information and configure the USB setting.



Legacy USB Support
Enable support for legacy USB. Normally if this option is not enabled, any attached USB mouse or USB keyboard won't be accessible until a USB compatible operating system is fully booted with all loaded USB drivers. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.
The choice: Enabled, Disabled, Auto (AUTO option disables legacy support if no USB devices are connected.)

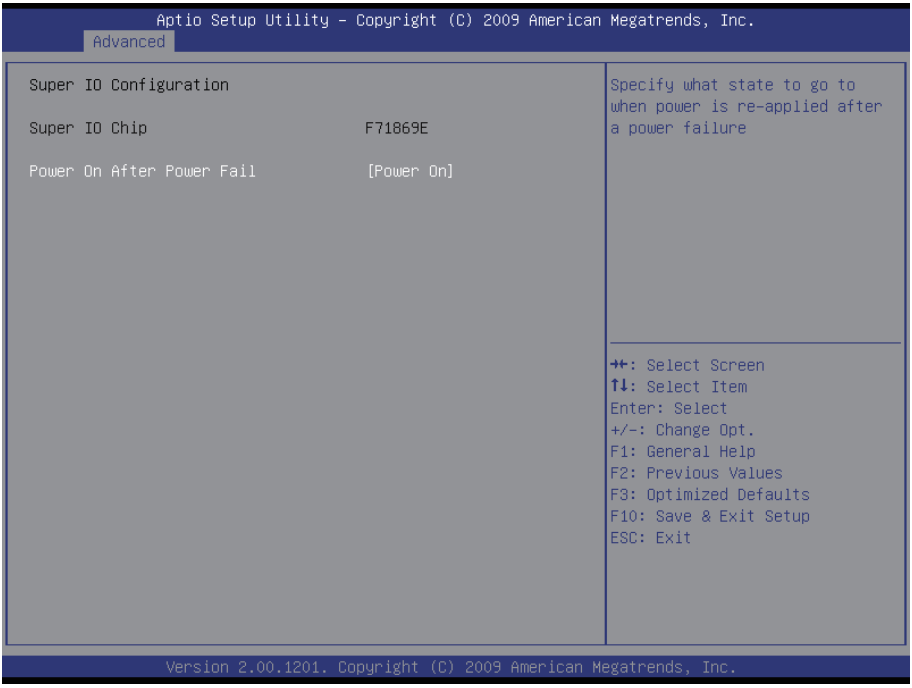
EHCI Hand-Off
This option allows you to enable EHCI Hand-Off function by BIOS if your computer operating system does not support it. EHCI is the abbreviation for Enhanced Host Controller Interface, which is necessary for high speed USB operation.
The choice: Enabled, Disabled

USB hardware delays and time-outs
The choice: 10, 20, 30, 40 sec.

Mass Storage Devices
This item allows you to set up mass storage devices.
The choice: Auto, Floppy, Forced FDD, Hard-Disk, CD-ROM

3.2.6 Super IO Configuration

You can use this item to set up or change the Super IO configuration for FDD controllers, parallel ports and serial ports.

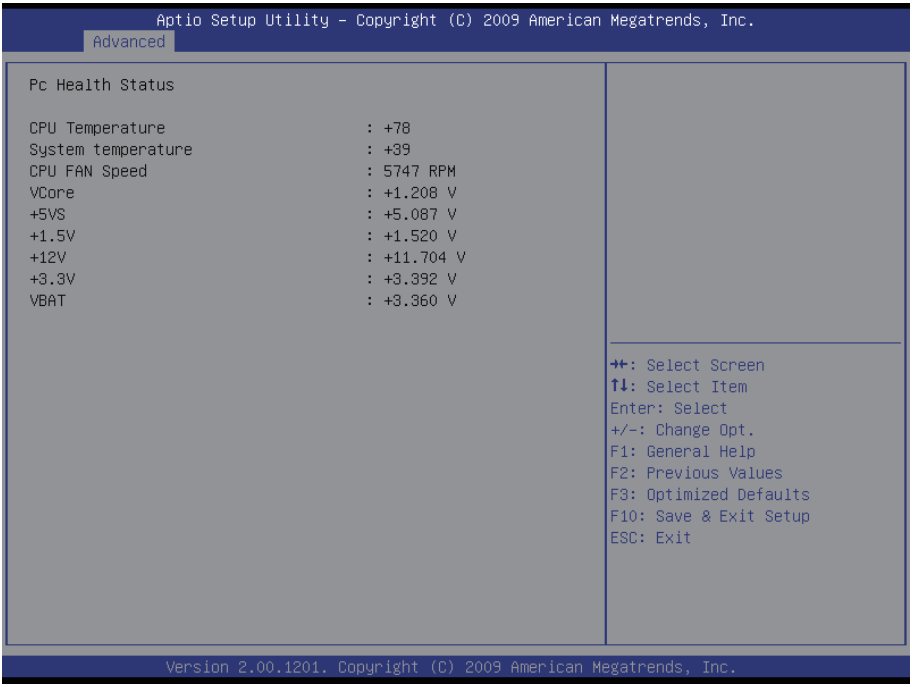


Power On After Power Fail

After Power Failure is a power management option that will set the mode of operation if a power loss occurs.
Settings:
Power Off: Keep the power off until the power button is pressed.
Power On: Restore power to the computer.

3.2.7 H/W Monitor

The H/W Monitor lists out the temperature and voltage information that is being monitored.



System/ CPU Temperature

Show you the current System / CPU fan temperature.

CPU Fan Speed

Show you the current CPU Fan operating speed.

Vcore

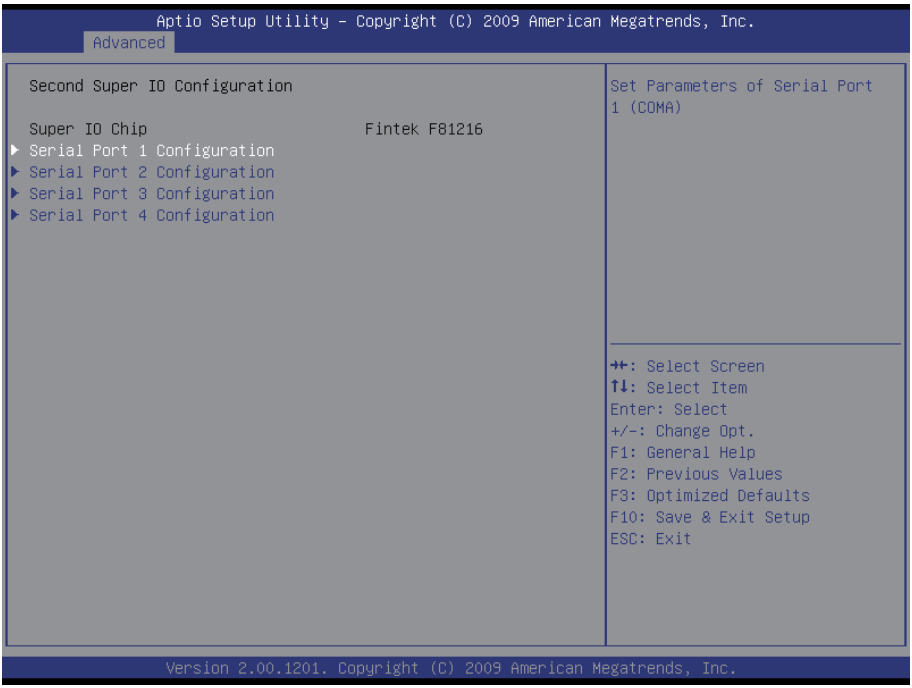
Show you the voltage level of CPU (Vcore).

+5VS / +1.5V / +3.3Vin / +12Vin / VBAT

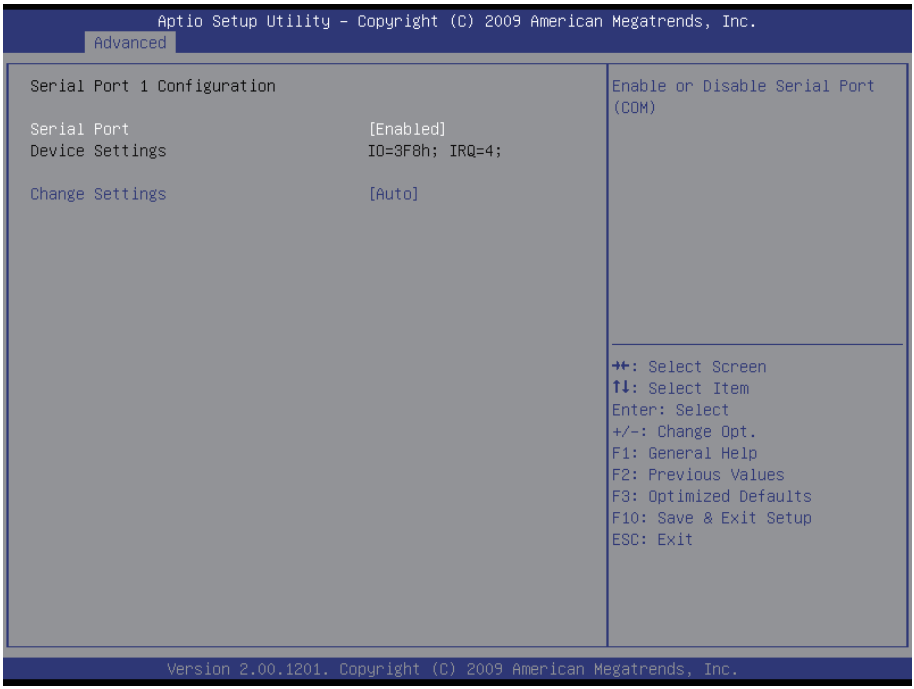
Show you the voltage level of +5VS, +1.5V, +3.3Vin, +12Vin, and battery.

3.2.8 Second Super IO Configuration

You can use this item to set up or change the Second Super IO configuration for FDD controllers, parallel ports and serial ports.



Serial Port 1~4 Configuration



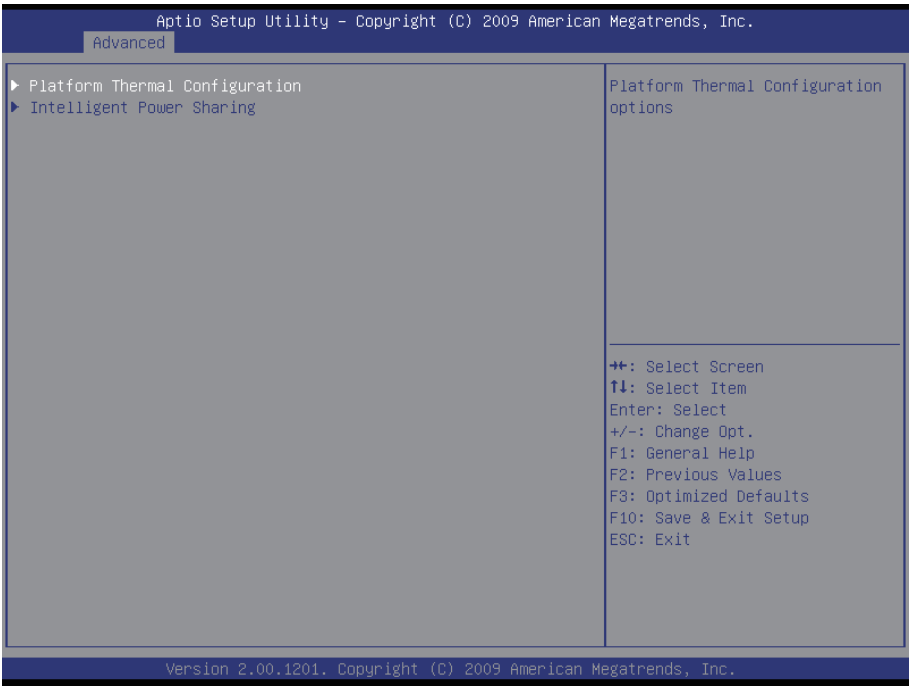
Serial Port

Use the Serial port option to enable or disable the serial port.
The choice: Enabled, Disabled

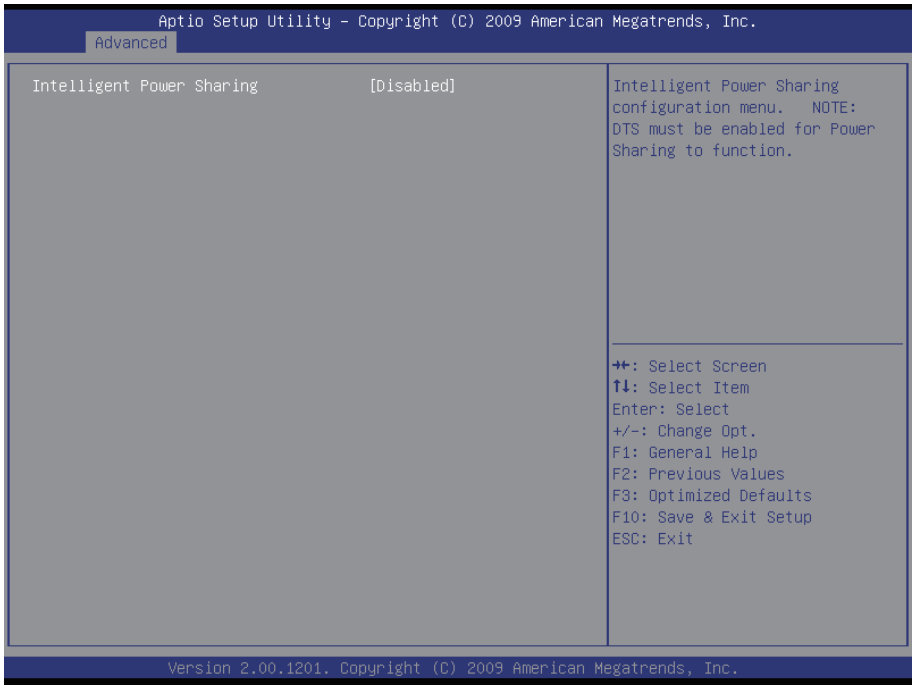
Change Settings

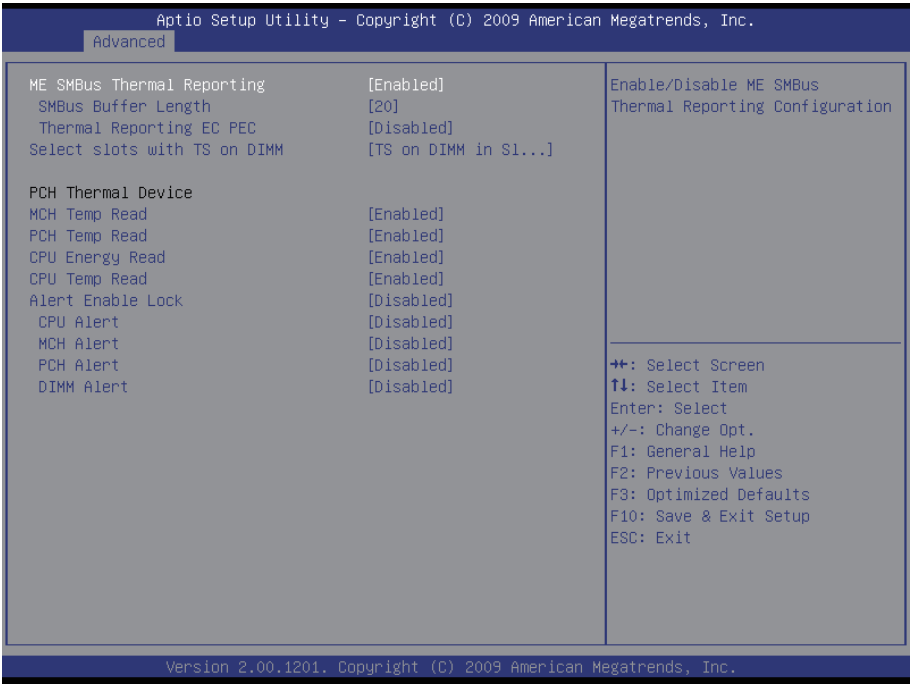
Use the Change Settings option to change the serial port's IO port address and interrupt address.
The choice:
IO=3F8h; IRQ=4,
IO=3F8h; IRQ=3,4,5,6,7,10,11,12
IO=2F8h; IRQ=3,4,5,6,7,10,11,12
IO=3E8h; IRQ=3,4,5,6,7,10,11,12
IO=2E8h; IRQ=3,4,5,6,7,10,11,12

3.2.9 Thermal Configuration



Select “Platform Thermal Configuration” or “Intelligent Power Sharing“ to access the submenus showing below.





ME SMBus Thermal Reporting

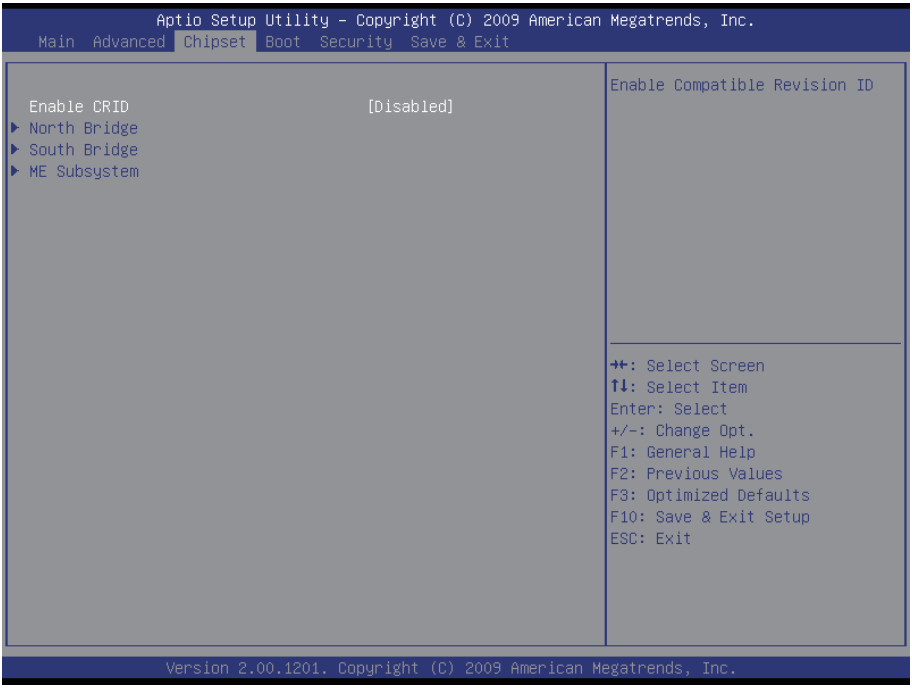
Enable/Disable ME SMBus Thermal Reporting Configuration.

PCH Thermal Device

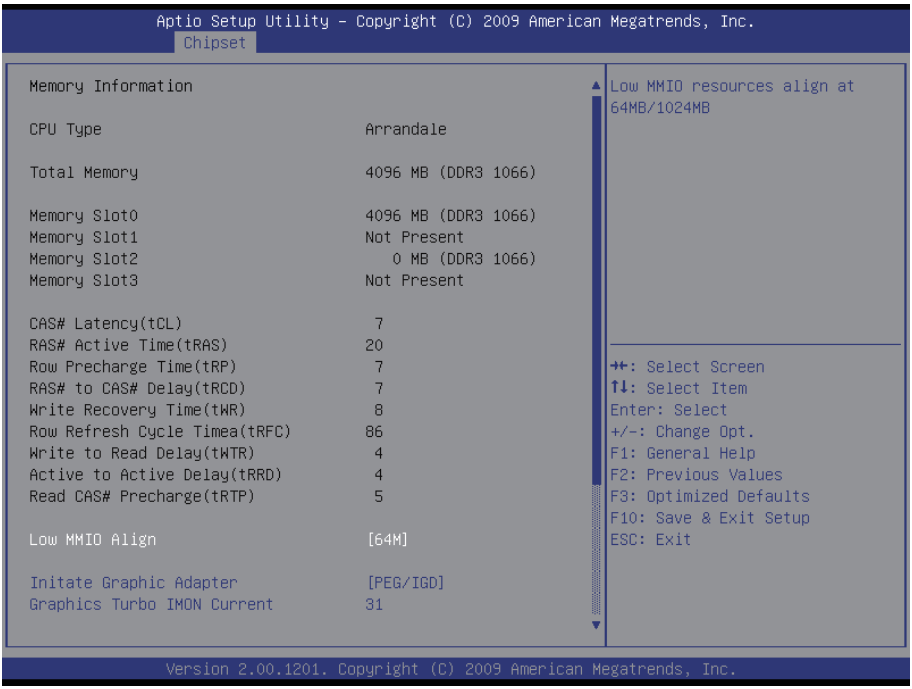
Enable/Disable MCH Temp Read, PCH Temp Read, CPU Energy Read, CPU Temp Read, Alert Enable Lock functions.

3.3 Advanced Chipset Settings

Select “Chipset” to enable CRID, access “North Bridge”, “South Bridge” and “ME Subsystem”.



3.3.1 North Bridge



Low MMIO Align

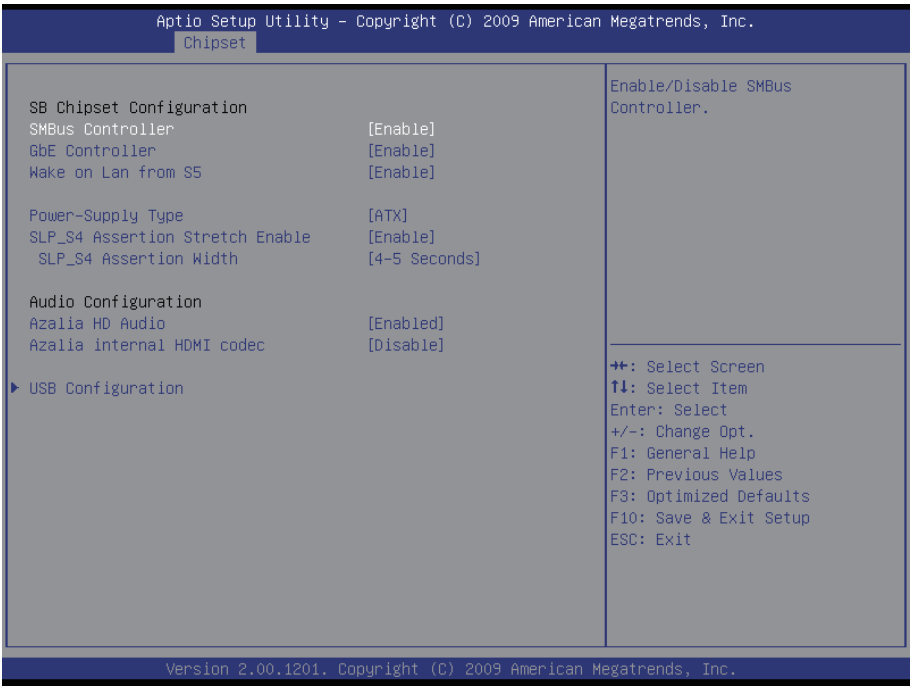
This option aligns Low MMIO resources together.
The choice: Enabled, Disabled

Initate Graphic Adapter

This item allows you to select which graphics controller to use and set it as the primary boot device.
The choice: IGD, PCI/IGD, PCI/PEG, PEG/IGD, PEG/PCI

3.3.2 South Bridge

Normally, the south bridge controls the basic I/O functions, such as USB and audio. This screen allows you to access the configurations of I/Os.



SMBus Controller

SMBus Controller help
The choice: Enabled, Disabled

GbE Controller

GbE Controller help
The choice: Enabled, Disabled

Wake on Lan from S5

Wake on Lan from S5 help
The choice: Enabled, Disabled

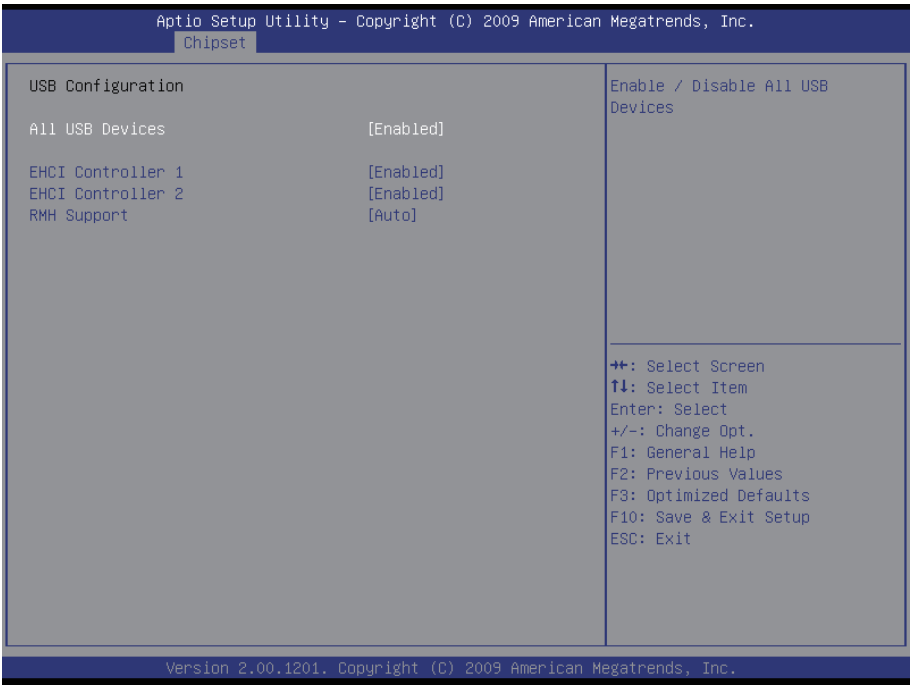
Azalia HD Audio

Use the Azalia HD Audio option to enable or disable the High Definition Audio controller.

The choice: Enabled, Disabled

USB Configuration

Select “USB Configuration“ to enter the following screen.

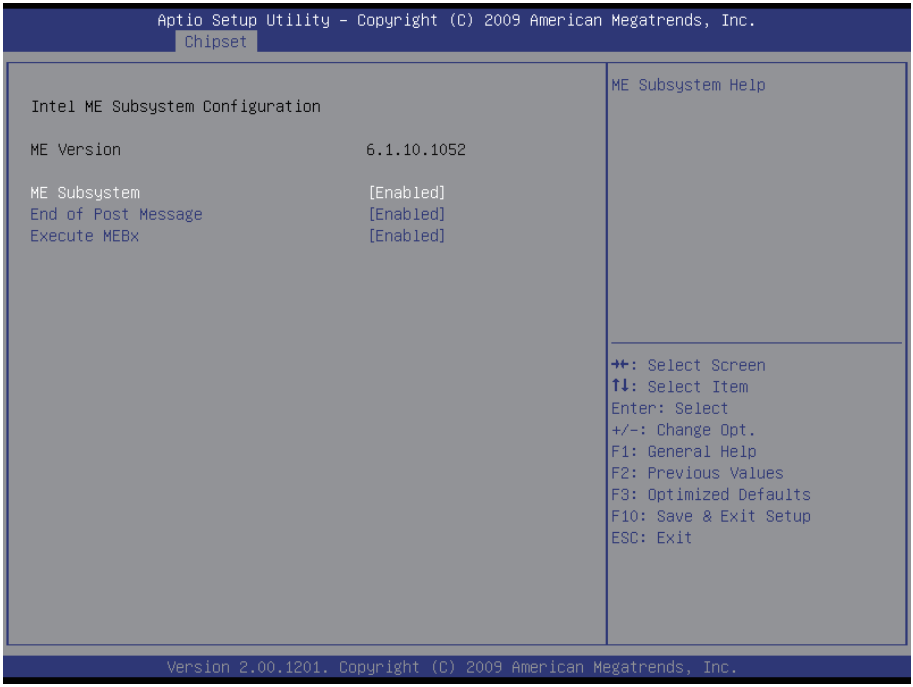


The USB Configuration menu is used to read USB configuration information and configure the USB settings.

The choice: Disable, Enable

3.3.3 ME Subsystem

Use the ME Subsystem menu to configure the Intel® Management Engine (ME) configuration options.



ME Subsystem

Use the ME Subsystem option to enable or disable the Intel® ME subsystem.

The choice: Enabled, Disabled

End of Post Message

Use the End of Post Message option to enable or disable the end of post message of the ME Subsystem.

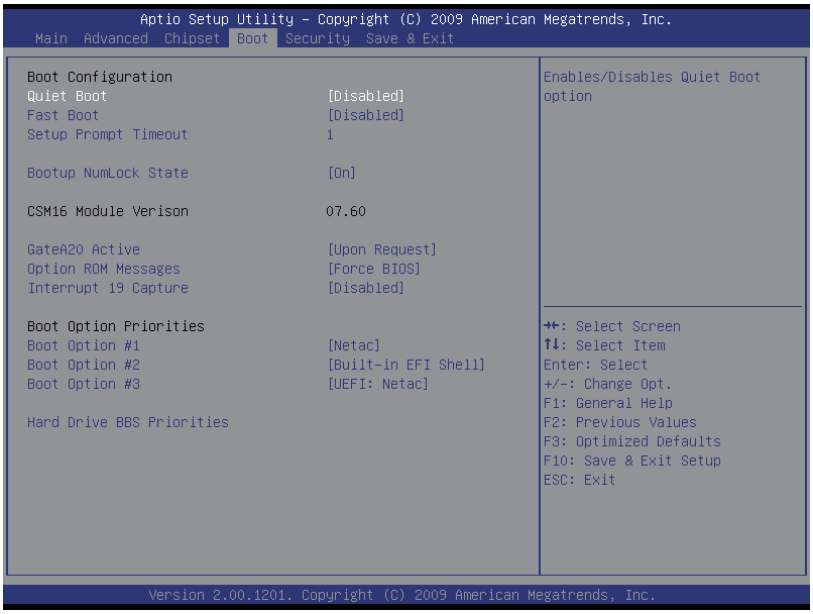
The choice: Enabled, Disabled

Execute MEBx

Use the Execute MEBx option to enable or disable the Intel® Management Engine BIOS extension (MEBx).

The choice: Enabled, Disabled

3.4 Boot Settings



Quiet Boot

This item can helps to select screen display when the system boots.
The choice: Enabled, Disabled

Fast Boot

Enable/Disable boot with initialization of a minimal set of devices required to launch active boot option. Ineffective for BBS boot options.
The choice: Enabled, Disabled

Setup Prompt Timeout

Seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

GateA20 Active

UPON REQUEST: GA20 can be disabled using BIOS services.
ALWAYS: disallow to disable GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages

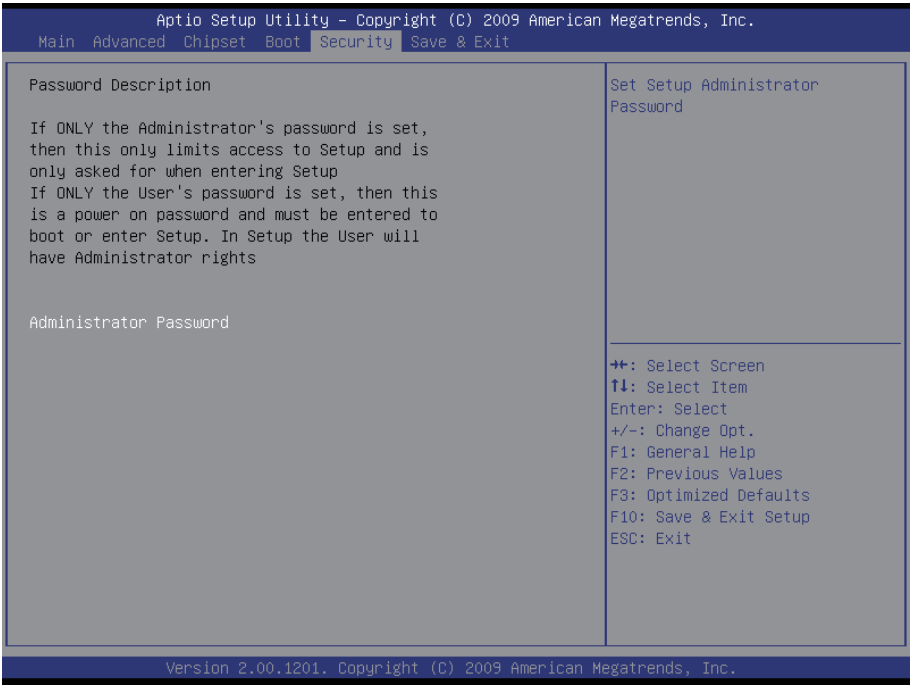
Set up display mode for Option ROM.
The choice: Force BIOS, Keep Current

Interrupt 19 Capture

Allow Option ROMs to trap int 19.
The choice: Enabled, Disabled

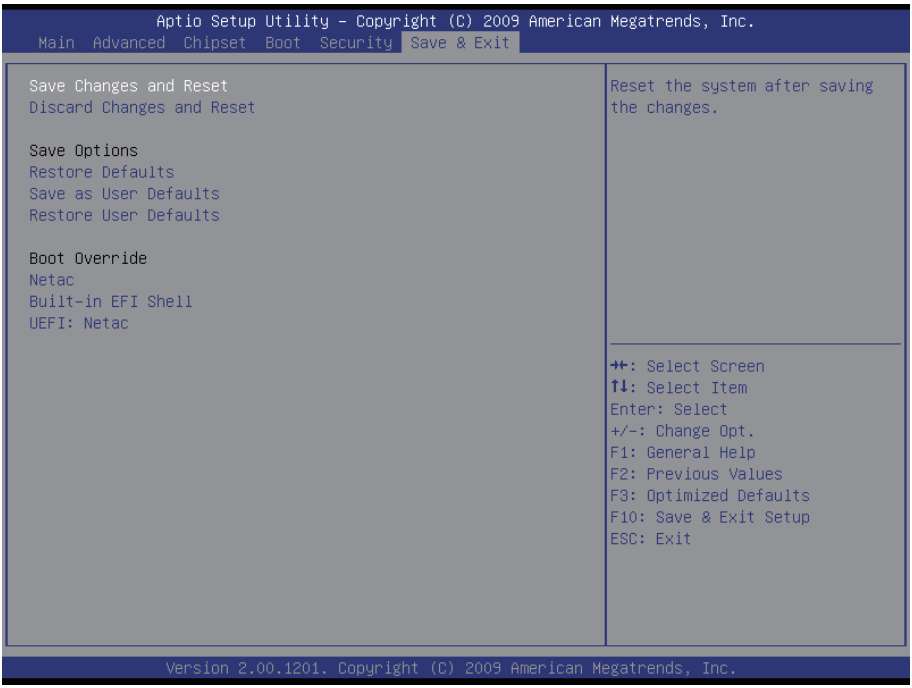
3.5 Security

You can set administrator password by Security menu.



3.6 Exit Options

Use the option to exit BIOS settings, and save/discard any changes you made.



3.7 Beep Sound codes list

3.7.1 Boot Block Beep codes

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

3.7.2 POST BIOS Beep codes

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

3.7.3 Troubleshooting POST BIOS Beep codes

Number of Beeps	Description
1, 2 or 3	Reseat the memory, or replace known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem is solved.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

3.8 AMI BIOS Checkpoints

3.8.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS *(Note)*:

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency and other CPU critical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done, including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is disabled. Perform keyboard controller BAT test. Save power-on CPUID value in scratch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module is not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enabled CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Perform main BIOS checksum and update recovery status accordingly.

D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0. See *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and given control to it. Determine whether in memory.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leave all RAM below 1MB Read-Write, including E000 and F000 shadow areas, but close SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POS (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.
DC	System is waking from ACPI S3 state.
E1 - E8 EC - EE	OEM memory detection / configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from platform next to it.

3.8.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS *(Note)*:

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L2 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration in line with the current configuration of the flash part.
FB	Set flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals to the recovery file size.
F4	The recovery file size does not equal to the found flash part size.

FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Set flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

3.8.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS *(Note)*:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also, initialize BIOS modules on POST entry and GPNV area. Initialize CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initialize data variables based on CMOS setup questions. Initialize both 8259 compatible PICs in the system.
05	Initialize the interrupt controlling hardware (generally, PIC) and interrupt vector table.
06	Do R/W test for CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Trap INT1Ch vector in "POSTINT1ChHandlerBlock."
07	Fix CPU POST interface calling pointer.
08	Initialize the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte after Auto detection of KB/MS uses AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor

C7	Early CPU Init Exit
0A	Initialize the 8042 compatible Key Board Controller.
0B	Detect the presence of PS/2 mouse.
0C	Detect the presence of Keyboard in KBC port.
0E	Test and initialize different input devices. Also, update the Kernel Variables. Trap the INT09h vector, so that the POST INT09h handler gets control over IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform of specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initialize different devices through DIM. See DIM Code Checkpoints section in document for more information.
2C	Initialize different devices. Detect and initialize the video adapter installed in the system that has optional ROMs.
2E	Initialize all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initialize the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any specific OEM information.
38	Initialize different devices through DIM. See DIM Code Checkpoints section in document for more information. USB controllers are initialized at this point.

39	Initialize DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, check for DEL keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…, etc.
52	Update CMOS memory size from memory found in memory test. Allocate memory for Extended BIOS Data Area from base memory. Program the memory hole or any kind of implementation that needs adjustment in system RAM size if needed.
60	Initialize NUM-LOCK status and program the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initialize IPL devices controlled by BIOS and optional ROMs.
7C	Generate and write contents for ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to user and get user's error response.
87	Execute BIOS setup if needed/requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disalbe NMI as selected.
90	Initialization of system management interrupted by invoking all handlers.
A1	Line-up work needed before booting to OS.
A2	Take care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initialize the Microsoft IRQ Routing Table. Prepare the runtime language module. Disable the system configuration display if needed.

A4	Initialize runtime language module. Display boot option's popup menu.
A7	Display the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initialize the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot, including final MTRR values.
00	Pass control to OS Loader (typically INT19h).

3.8.4 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST tries to initialize different system buses. The following table describes the main checkpoints where the DIM module is accessed *(Note)*:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and non-compliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set as automatic configuration and configures all remaining PnP and PCI devices.

While controlling in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble “X” indicates the function number that is being executed. “X” can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.

3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = On-board System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

3.8.5 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events *(Note)*:

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Enter sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Wake from sleep state S1, S2, S3, S4, or S5.

Note:
Please note that checkpoints may differ between different platforms based on system configuration. Checkpoints may change due to vendor requirements, system chipset or optional ROMs from add-in PCI devices.

Appendix

Appendix-A I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses, which is the identity for the device.
The following table lists the I/O port addresses used.

Address	Device Description
00000000 - 0000000F	DMA Controller
00000000 - 00000CF7	PIC bus
00000010 - 0000001F	Motherboard Resource
00000020 - 00000021	Programmable Interrupt Controller
00000022 - 0000003F	Motherboard Resource
00000040 - 00000043	System Timer
00000044 - 0000005F	Motherboard Resource
00000060 - 00000060	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
00000061 - 00000061	System Speaker
00000062 - 00000063	Motherboard Resource
00000064 - 00000064	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
00000065 - 0000006F	Motherboard Resource
00000070 - 00000071	System CMOS/Real Time Clock
00000072 - 0000007F	Motherboard Resource
00000080 - 00000080	Motherboard Resource
00000081 - 00000083	DMA Controller
00000084 - 00000086	Motherboard Resource
00000087 - 00000087	DMA Controller
00000088 - 00000088	Motherboard Resource
00000089 - 0000008B	DMA Controller
0000008C - 0000008E	Motherboard Resource
0000008F - 0000008F	DMA Controller
00000090 - 0000009F	Motherboard Resource
000000A0 - 000000A1	Programmable Interrupt Controller
000000A2 - 000000BF	Motherboard Resource

000000C0 - 000000DF	DMA Controller
000000E0 - 000000EF	Motherboard Resource
000000F0 - 000000FF	Math Co-processor
00000170 - 00000177	Secondary IDE Channel
000001F0 - 000001F7	Primary IDE Channel
00000274 - 00000277	ISAPNP Read Data Port
00000279 - 00000279	ISAPNP Read Data Port
00000290 - 0000029F	Motherboard Resource
000002E8 - 000002EF	Communications Port (COM4, If use)
000002F8 - 000002FF	Communications Port (COM2, If use)
00000376 - 00000376	Secondary IDE Channel
000003B0 - 000003BB	Intel(R) HD Graphics
000003C0 - 000003DF	Intel(R) HD Graphics
000003E8 - 000003EF	Communications Port (COM3, If use)
000003F6 - 000003F6	Secondary IDE Channel
000003F8 - 000003FF	Communications Port (COM1, If use)
00000400 - 0000047F	System Board
000004D0 - 000004D1	Motherboard Resource
00000500 - 0000057F	System Board
00000A79 - 00000A79	ISAPNP Read Data Port
00000D00 - 0000FFFF	PCI bus
00001180 - 0000119F	System Board
0000E000 - 0000E01F	Intel(R) 82583V Gigabit Network Connection
0000E000 - 0000EFFF	Intel(R) 5 Series/3400 Series Chipset Family PCI Express Root Port 6 - 3B4C
0000F000 - 0000F01F	Intel(R) 5 Series/3400 Series Chipset Family SMBus Controller - 3B30
0000F020 - 0000F02F	Intel(R) 5 Series/3400 Series Chipset Family 2 port Serial ATA Storage Controller
0000F030 - 0000F03F	Intel(R) 5 Series/3400 Series Chipset Family 2 port Serial ATA Storage Controller

0000F040 - 0000F043	Intel(R) 5 Series/3400 Series Chipset Family 2 port Serial ATA Storage Controller
0000F050 - 0000F057	Intel(R) 5 Series/3400 Series Chipset Family 2 port Serial ATA Storage Controller
0000F060 - 0000F063	Intel(R) 5 Series/3400 Series Chipset Family 2 port Serial ATA Storage Controller
0000F070 - 0000F077	Intel(R) 5 Series/3400 Series Chipset Family 2 port Serial ATA Storage Controller
0000F080 - 0000F08F	Intel(R) 5 Series/3400 Series Chipset Family 4 port Serial ATA Storage Controller
0000F090 - 0000F09F	Intel(R) 5 Series/3400 Series Chipset Family 4 port Serial ATA Storage Controller
0000F0E0 - 0000F0E7	Intel(R) HD Graphics

Appendix-B Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System Timer
IRQ 1	Keyboard Controller
IRQ 2	VGA and Link to Secondary PIC
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 5	PCI Device
IRQ 6	Standard Floppy Disk Controller
IRQ 7	Parallel Port
IRQ 8	System CMOS/real time clock
IRQ 9	Microsoft ACPI-Compliant System
IRQ 10	PCI Device
IRQ 11	PCI Device
IRQ 12	PS/2 Compatible Mouse
IRQ 13	FPU Exception
IRQ 14	IDE Controller
IRQ 15	PCI Device

Appendix-C BIOS memory mapping

Address	Device Description
000A0000 - 000BFFFF	Intel(R) HD Graphics
000A0000 - 000BFFFF	PCI bus
D0000000 - DFFFFFFF	Intel(R) HD Graphics
E0000000 - EFFFFFFF	System Board
FE000000 - FE3FFFFF	Intel(R) HD Graphics
FE400000 - FE4FFFFF	Intel(R) 82583V Gigabit Network Connection
FE400000 - FE5FFFFF	Intel(R) 5 Series/3400 Series Chipset Family PCI Express Root Port 6 - 3B4C
FE500000 - FE51FFFF	Intel(R) 82583V Gigabit Network Connection
FE520000 - FE523FFF	Intel(R) 82583V Gigabit Network Connection
FE600000 - FE603FFF	Microsoft UAA Bus Driver for High Definition Audio
FE605000 - FE6050FF	Intel(R) 5 Series/3400 Series Chipset Family SMBus Controller - 3B30
FE606000 - FE6063FF	Intel(R) 5 Series/3400 Series Chipset Family USB Enhanced Host Controller - 3B34
FE607000 - FE6073FF	Intel(R) 5 Series/3400 Series Chipset Family USB Enhanced Host Controller - 3B3C
FE608000 - FE60800F	Intel(R) Management Engine Interface
FEC00000 - FECFFFFF	System Board
FED08000 - FED08FFF	System Board
FED14000 - FED19FFF	System Board
FED1C000 - FED1FFFF	System Board
FED20000 - FED3FFFF	System Board
FED90000 - FED93FFF	System Board
FEE00000 - FEE0FFFF	System Board
FF000000 - FFFFFFFF	System Board

Appendix-D Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitor the activity of CPU. Application software depends on its own requirement to trigger WDT with adequate timer setting. Before WDT time-out, the functional normal system will reload the WDT. The WDT never times out for a normal system. Then, WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255-level watchdog timer by software programming. Below are the source codes written in assembly & C, please take them as WDT application examples.

Assembly Code

```
;-- Initial W83627 --
mov AX, 2Eh
mov DX, AX
mov AL, 87h
out DX, AX ;
out DX, AX ; initial W83627 start
;--
mov AX, 2Eh
mov DX, AX
mov AL, 2Bh
out DX, AL ; Select CR2B
mov AL, 00h
inc DX
out DX, AL ; Set CR2B bit 4=0, PIN89=WDTO
;--
mov AX, 2Eh
mov DX, AX
mov AL, 07h
out DX, AL ; Point to Logical Device Selector
mov AL, 08h
inc DX
out DX, AL ; Select Logical Device 8
;--
mov AX, 2Eh
mov DX, AX
mov AL, 30h
out DX, AL ; select CR30
mov AL, 01h
inc DX
out DX, AL ; update CR30 to 01h
```

```
;--
mov AX, 2Eh
mov DX, AX
mov AL, 0F0h
out DX, AL ; select CRF0
mov AL, 00h
inc DX
out DX, AL ; set CRF0=00h, output
;--
mov AX, 2Eh
mov DX, AX
mov AL, 0F5h
out DX, AL ; select CRF5, WDT Timer unit
mov AL, 00h ; bit2 =0 ->second ; bit2 =1 -> minute
inc DX
out DX, AL ; update CRF5 bit2 to 00h
;--
mov AX, 2Eh
mov DX, AX
mov AL, 0F6h
out DX, AL ; select CRF6, WDT Timer
mov AL, 05h
inc DX
out DX, AL ; update CRF6 to 5 unit
;---
mov AX, 2Eh
mov DX, AX
mov AL, AAh
out DX, AX
;-- end
```

C Language Code

```
/*-----      Include Header Area -----*/
#include “math.h”
#include “stdio.h”
#include “dos.h”

/*-----      routing, sub-routing -----*/

void main()
{
/*-------- index port 0x4e ---------*/
            outportb(0x4e, 0x87);          /* initial IO port */
```

```
        outportb(0x4e, 0x87);          /* twice,  */

        outportb(0x4e, 0x07);          /* point to logical device */
        outportb(0x4e+1, 0x07);          /* select logical device 7 */
        outportb(0x4e, 0xf5);         /* select offset f5h */
        outportb(0x4e+1, 0x40);          /* set bit5 = 1 to clear bit5 */
        outportb(0x4e, 0xf0);         /* select offset f0h */
        outportb(0x4e+1, 0x81);          /* set bit7 =1 to enable WDTRST# */
        outportb(0x4e, 0xf6);         /* select offset f6h */
        outportb(0x4e+1, 0x05);          /* update offset f6h to 0ah :10sec */
        outportb(0x4e, 0xf5);         /* select offset f5h */
        outportb(0x4e+1, 0x20);          /* set bit5 = 1 enable watch dog time */

        outportb(0x4e, 0xAA);          /* stop program F71869E, Exit */
}
```