EmCORE-a55E1

3.5” Compact Board

User’s Manual

Version 1.1

2014.02

Revision History

Version	Date	Description
1.0	2013/03/21	initial release
1.0	2013/04/10	change cover month
		Correct description in Appendix D.
1.0	2013/04/18	change operating temp. in section 1.3
1.1	2014/02/06	P.5 Add AMD Windows 8 driver path

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Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

Declaration of Conformity

CE

The CE symbol on your product indicates that it is in compliance with the directives of the Union European (EU). A Certificate of Compliance is available by contacting Technical Support.

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from ARBOR. Please contact your local supplier for ordering information.

This product has passed the CE test for environmental specifications. Test conditions for passing included the equipment being operated within an industrial enclosure. In order to protect the product from being damaged by ESD (Electrostatic Discharge) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

> Warning
>
> This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC Class A

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received, including interference that may cause undesired operation.

NOTE:

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

RoHS

ARBOR Technology Corp. certifies that all components in its products are in compliance and conform to the European Union's Restriction of Use of Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2002/95/EC.

The above mentioned directive was published on 2/13/2003. The main purpose of the directive is to prohibit the use of lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE) in electrical and electronic products. Member states of the EU are to enforce by 7/1/2006.

ARBOR Technology Corp. hereby states that the listed products do not contain unintentional additions of lead, mercury, hex chrome, PBB or PBDB that exceed a maximum concentration value of 0.1% by weight or for cadmium exceed 0.01% by weight, per homogenous material. Homogenous material is defined as a substance or mixture of substances with uniform composition (such as solders, resins, plating, etc.). Lead-free solder is used for all terminations (Sn(96-96.5%), Ag(3.0-3.5%) and Cu(0.5%)).

SVHC / REACH

To minimize the environmental impact and take more responsibility to the earth we live, Arbor hereby confirms all products comply with the restriction of SVHC (Substances of Very High Concern) in (EC) 1907/2006 (REACH --Registration, Evaluation, Authorization, and Restriction of Chemicals) regulated by the European Union.

All substances listed in SVHC < 0.1 % by weight (1000 ppm)

Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside.

2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry.

3. Use a grounded wrist strap when handling computer components.

4. Place components on a grounded antistatic pad or on the bag that comes with the Single Board Computer, whenever components are separated from the system.

Replacing the Lithium Battery

Incorrect replacement of the lithium battery may lead to a risk of explosion.

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Do not throw lithium batteries into the trash-can. It must be disposed of in accordance with local regulations concerning special waste.

Technical Support

If you have any technical difficulties, please consult the user's manual first at: ftp://ftp.arbor.com.tw/pub/manual
Please do not hesitate to call or e-mail our customer service when you still cannot find out the answer.

http://www.arbor.com.tw
E-mail:info@arbor.com.tw

Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantability and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

Chapter 1

Introduction

1.1 The Product

EmCORE-a55E1, the Compact Board is an embedded board based on the Industry standardized 3.5” form factor. The board is highly integrated, with inbuilt powerful Core logic. EmCORE-a55E1 features a number of designs, including additional expansion buses, fanless cooling and the CPU supplied by AMD to answer the needs ranging from high performance to low power consumption. The compact form makes EmCORE-a55E1 the best choice for high-density systems with these features:

- Soldered Onboard AMD Fusion G-Series Processor
- Dual Gigabit Ethernet Ports
- HDMI, Analog RGB and Dual Channel 24-bit LVDS
- Dual Independent Displays
- Integrated SIM Socket to Support Mobile Telecommunication

1.2 About This Manual

This user’s manual provides general information and installation instructions about the product. This User’s Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this booklet. please consult your vendor before further handling.

1.3 Specifications

Form Factor	3.5" Compact Board
CPU	Soldered onboard AMD Fusion G-T56N 1.65GHz, or G-T40N 1.0GHz processor
Chipset	AMD FCH A55E
System Memory	1 x 204-pin DDR3 SO-DIMM socket, supporting 800/1066/1333MHz SDRAM up to 4GB
Graphics	Integrated AMD Radeon HD 6320 w/ G-T56N, HD 6250 w/ G-T40N
Graphics Interface	Analog RGB supports up to 2560 x 1600 @60Hz
	LCD : Dual Channel supports 18/24-bit LVDS, resolution up to 1920 x 1600
	Support HDMI 1.3a
Ethernet	2 x Intel® 82583V PCIe Gigabit Ethernet controllers
I/O Chip	Fintek F81866
BIOS	AMI UEFI BIOS
Audio	Realtek ALC662 5.1 Channel HD Audio Codec, Mic-in/ Line-in/ Line-out
Storage	2 x Serial ATA ports with 600MB/s HDD transfer rate
	1 x CFast socket
Serial Port	6 x COM ports (5 x RS-232, 1 x RS-232/422/485 selectable)
Parallel Port	1 x LPT port
Digital I/O	8-bit programmable Digital Input/Output, shared with LPT port connector
Keyboard & Mouse	1 x 6-pin wafer connector for Keyboard and Mouse (PS/2 interface via Y-cable)
Universal Serial Bus	6 x USB 2.0 ports
Expansion Bus	1 x Mini-card socket
	1 x SIM socket
Power Connector	12VDC single input, with small 4-pin power connector
Operation Temp.	0 ~ 70°C (32 ~158°F)
Operating Humidity	0 ~ 90% (non-condensing)
Watchdog Timer	1~255 levels reset
Dimension (L x W)	146 x 102 mm (5.75” x 4.00”)

1.4 Inside the Package

Before you begin installing your Compact Board, please make sure that the following materials have been shipped:

1 x EmCORE-a55E1 3.5" AMD Fusion G-Series Compact Board

1 x Driver CD

1 x Quick Installation Guide

If any of the above items is damaged or missing, contact your vendor immediately.

1.5 Ordering Information

EmCORE-a55E1-T56N	AMD G-T56N 3.5” Compact Board
EmCORE-a55E1-T40N	AMD G-T40N 3.5” Compact Board
CBK-14-55E1-00 P/N: 6911455010000P	Cable kit 1 x Audio cable 5 x COM port cables 2 x USB cables 1 x VGA cable 1 x LPT port cable 2 x SATA cables 1 x PS/2 KB/MS cable 1 x SATA power cable

1.6 The Installation Paths of CD Driver

Windows 7

Device	Driver Path
CHIPSET & VGA	\EmCORE-a55E1\CHIPSET\Win7
AUDIO	\EmCORE-a55E1\AUDIO\Win7\32-bit
	\EmCORE-a55E1\AUDIO\Win7\64-bit
LAN	\EmCORE-a55E1\ETHERNET\Win7\32-bit
	\EmCORE-a55E1\ETHERNET\Win7\64-bit

Windows XP

Device	Driver Path
CHIPSET & VGA	\EmCORE-a55E1\CHIPSET\WinXP
AUDIO	\EmCORE-a55E1\AUDIO\WinXP
LAN	\EmCORE-a55E1\ETHERNET\WinXP\32-bit
	\EmCORE-a55E1\ETHERNET\WinXP\64-bit

Windows 8

Device	Driver Path
ALL	EmCORE-a55E1\Win8\AMD G-series 13.151-EDG_ Direct\130819a-161838C-EDG_Direct

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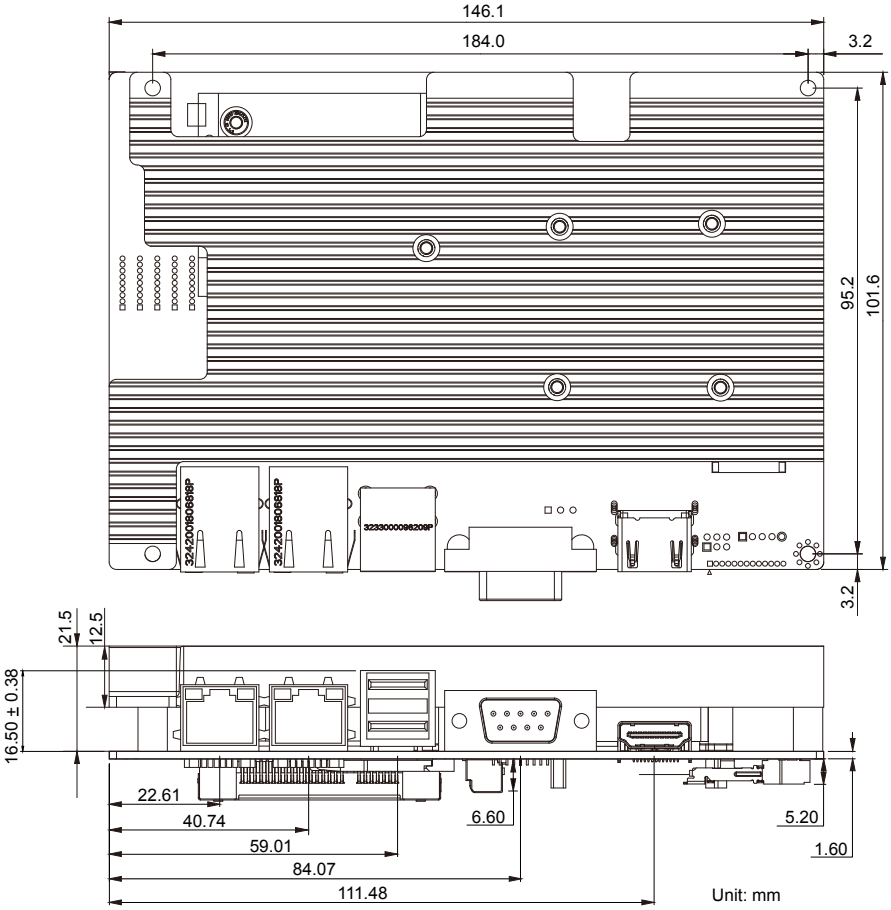
Chapter 2

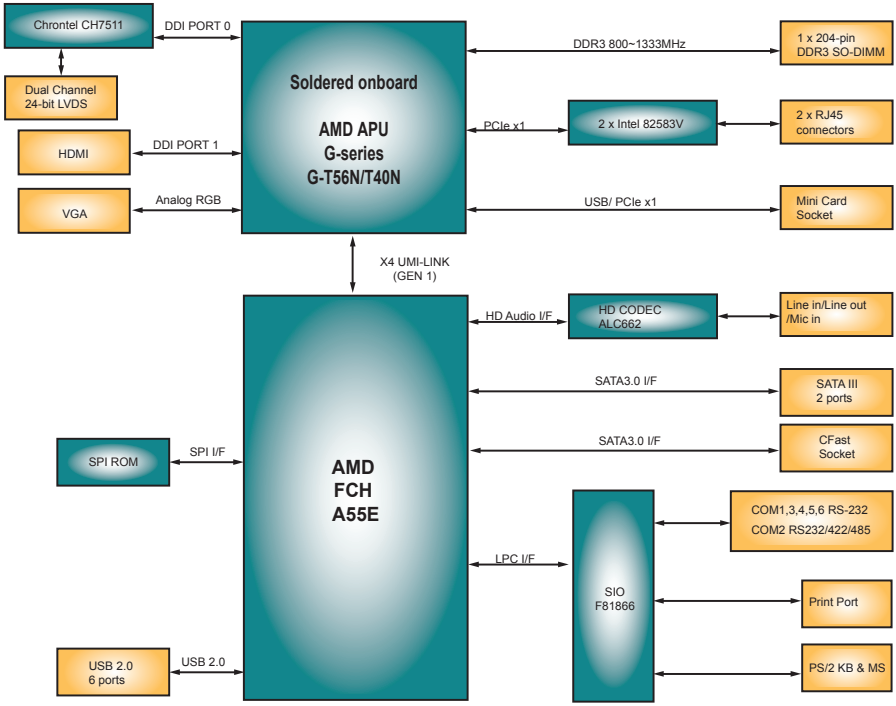
Board Overview

2.1 Board Dimensions

The following illustration shows the dimension of EmCORE-a55E1, with the measurements in width, depth, and height called out.



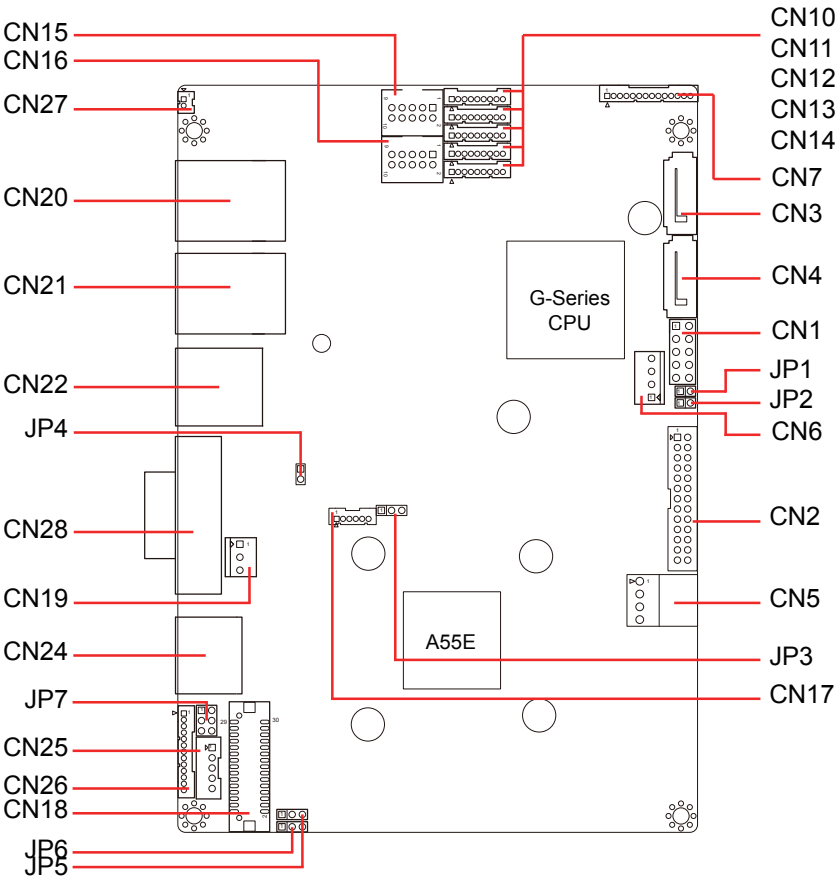
2.2 Block Diagram



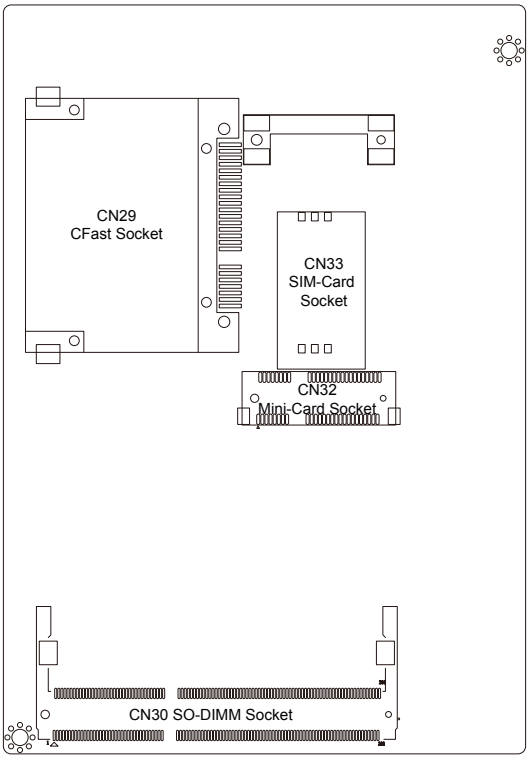
2.3 Jumpers and Connectors

2.3.1 Location

Top Side



Bottom Side



2.3.2 Quick Reference

Jumpers	Function
JP1, 2	Power Selection for SATA DOM (for CN3, CN4's Pin7)
JP3	Clear CMOS
JP4	AT/ATX Power Mode Selection
JP5	LCD Backlight Voltage Selection
JP6	LCD Panel Voltage Selection
JP7	COM2 Ring/+5V/+12V Selection

Connectors	Function
CN1	Front Panel Connector
CN2	LPT Connector
CN3~4	SATA Connectors
CN5	Small 4-pin Power Connector
CN6	SATA Power Connector
CN7	Audio Connector
CN10~14	COM1/5/6/3/4 Connectors
CN15~16	USB Connectors
CN17	KB/MS Connector
CN18	LVDS Connector
CN19	FAN Connector
CN20~21	GbE RJ-45 Connectors
CN22	USB Connector
CN24	HDMI Connector
CN25	Backlight Connector
CN26	VGA Connector
CN27	Battery Connector
CN28	COM2 Connector
CN29	CFast Socket
CN30	DDR3 SO-DIMM Socket
CN32	Mini-Card Socket
CN33	SIM Card Socket

2.3.3 Jumpers

The jumper is “short” (closed) when the jumper cap is placed on pins. If not, that means the jumper is “open.” The following in this section will explicate each of the components one-by-one.


Pin open


Pin short (closed)

Pin 2-3 short (closed)

Pin 1-2 short (closed)

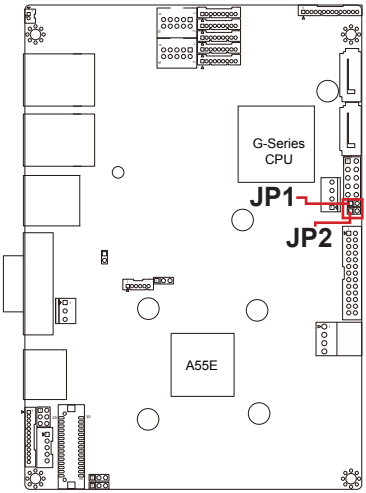
JP1, 2

Function: Power Selection for SATA DOM (for CN3, CN4’s Pin7)

Jumper Type: 2.00mm pitch 1x2-pin header

Setting:

Pin	Mode	
Short	+5V Power ON	
Open	+5V Power OFF (default)	



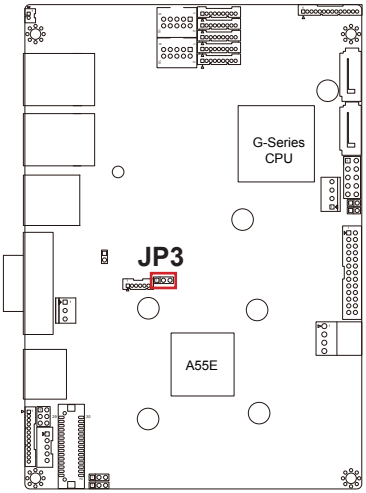
JP3

Function: Clear CMOS

Jumper Type: 2.00mm pitch 1x3-pin header

Setting:

Pin	Mode	
1-2	Keep CMOS (default)	
2-3	Clear CMOS	



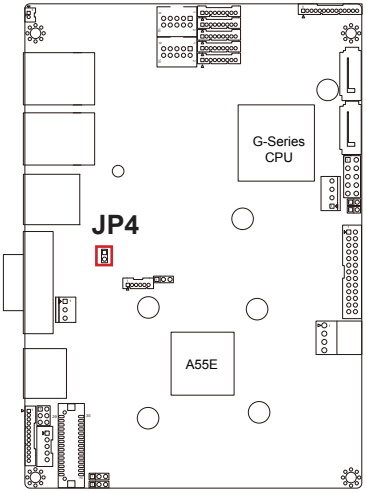
JP4

Function: AT/ATX Power Mode Selection

Jumper Type: 2.00mm pitch 1x2-pin header

Setting:

Pin	Mode	
Short	AT	
Open	ATX (default)	



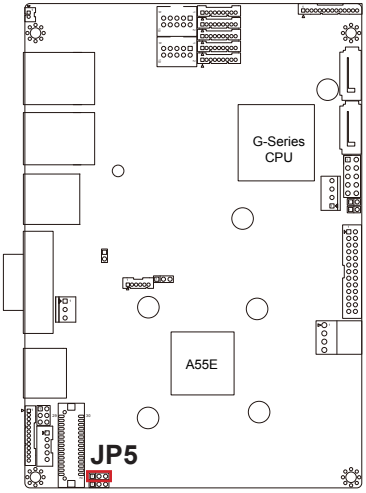
JP5

Function: LCD Backlight Voltage Selection

Jumper Type: 2.00mm pitch 1x3-pin header

Setting:

Pin	Mode	
1-2	+5V	
2-3	+12V (default)	



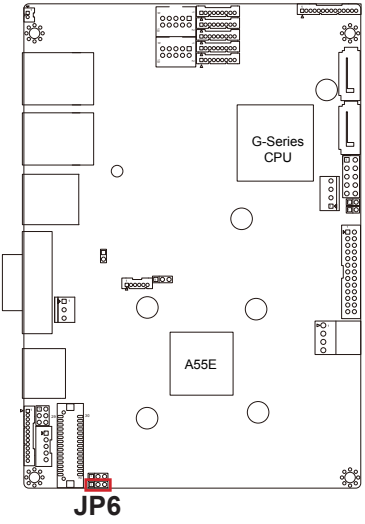
JP6

Function: LCD Panel Voltage Selection

Jumper Type: 2.00mm pitch 1x3-pin header

Setting:

Pin	Mode	
1-2	+5V	
2-3	+3.3V (default)	



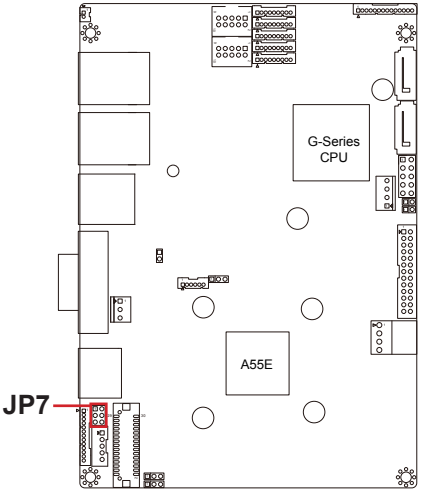
JP7

Function: COM2 Ring/+5V/+12V Selection

Jumper Type: 2.00mm pitch 2x3-pin header

Setting:

Pin	Mode	
1-2	+12V	
3-4	RI2#_SEL (default)	
5-6	+5V	



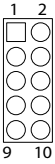
2.3.4 Connectors

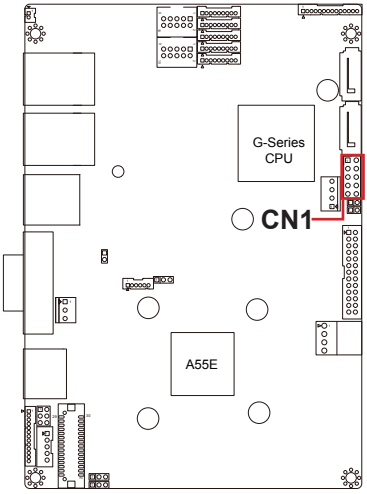
CN1

Function: Front Panel Connector

Jumper Type: 2.54mm pitch 2x5-pin header

Pin	Description	Pin	Description
1	Power Button-	2	Power Button+
3	HDD_LED-	4	HDD_LED+
5	External Buzzer-	6	External Buzzer+
7	Power LED-	8	Power LED+
9	Reset Switch-	10	Reset Switch+



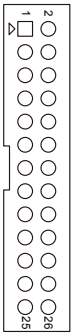


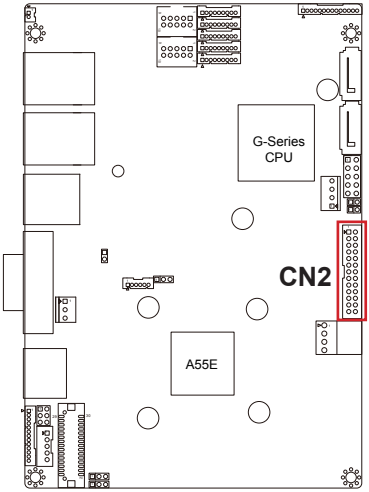
CN2

Function: LPT Connector

Jumper Type: 2.00mm pitch 2x13-pin header

Pin	Description	Pin	Description
1	STB#	2	AFD#
3	PTD0 / *DIO0	4	ERROR#
5	PTD1 / *DIO1	6	INIT#
7	PTD2 / *DIO2	8	SLIN#
9	PTD3 / *DIO3	10	GND
11	PTD4 / *DIO4	12	GND
13	PTD5 / *DIO5	14	GND
15	PTD6 / *DIO6	16	GND
17	PTD7 / *DIO7	18	GND
19	ACK#	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SELECT	26	N/C





*Note: The LPT connector is shared with 8-bit programmable Digital Input/ Output. To use that, please change LPT Transfer Function to GPIO Mode in Super IO Configuration in BIOS first. Refer to 4.2.5 F81866 Super IO Configuration on page 37 for how to do that.

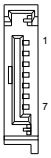
CN2 Pin	Description	Correspond to
3	DIO0	GPIO80
5	DIO1	GPIO81
7	DIO2	GPIO82
9	DIO3	GPIO83
11	DIO4	GPIO84
13	DIO5	GPIO85
15	DIO6	GPIO86
17	DIO7	GPIO87

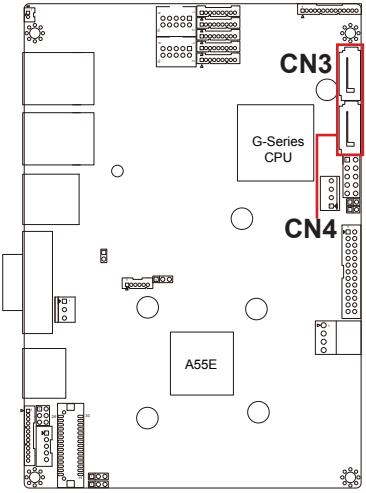
CN3~4

Function: SATA Connectors

Jumper Type: High speed transfer rates (600MB/s). Pin-7 is set to +5V by JP1/ JP2.

Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	+5V (default)



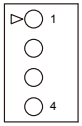


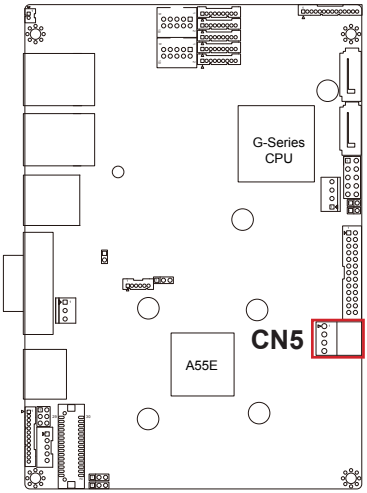
CN5

Function: Small 4-pin Power Connector

Jumper Type: 2.54mm pitch 1x4-pin wafer one wall right angle connector.

Pin	Description
1	+5V
2	GND
3	GND
4	+12V



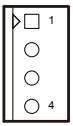


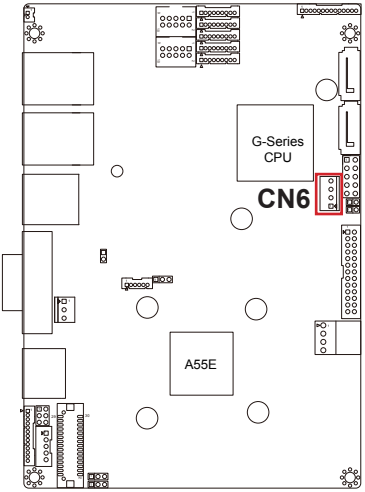
CN6

Function: SATA Power Connector

Jumper Type: 2.54mm pitch 1x4-pin wafer one wall connector.

Pin	Description
1	+5V
2	GND
3	GND
4	+12V



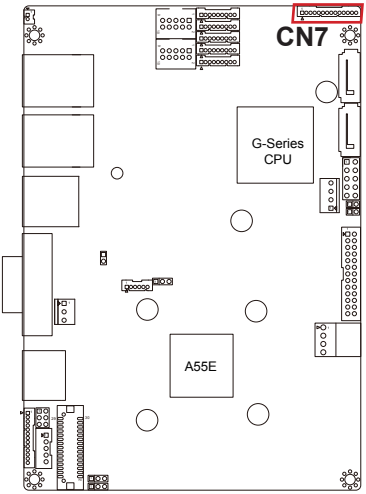


CN7

Function: Audio Connector

Jumper Type: 1x14-pin ACES 1.25mm 86801-14 4-wall connector.

Pin	Description
1	MIC
2	MIC_VREF
3	GND
4	CD_GND
5	LINEIN_L
6	CD_IN_L
7	LINEIN_R
8	CD_GND
9	GND
10	CD_IN_R
11	LINEOUT_L
12	LINEOUT_R
13	GND
14	GND

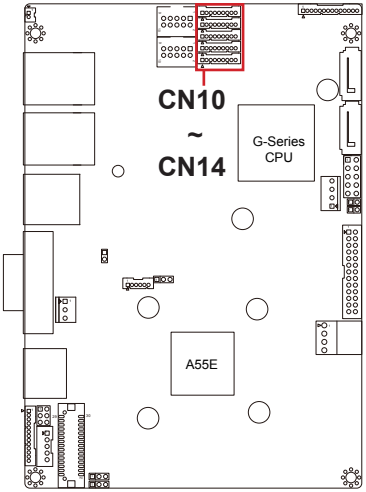


CN10~14

Function: COM1/5/6/3/4 Connectors

Jumper Type: 1x9-pin ACES 1.25mm 86801-09 4-wall connector.

Pin	Description
1	DCD#
2	DSR#
3	RXD
4	RTS#
5	TXD
6	CTS#
7	DTR#
8	RI#
9	GND

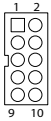


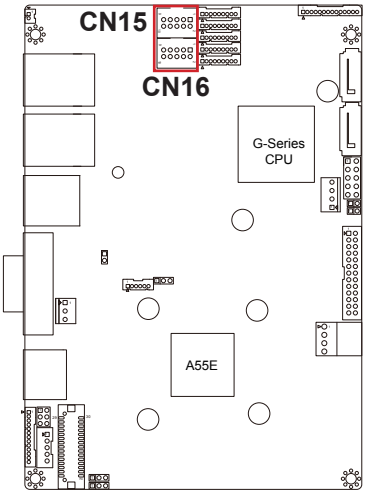
CN15~16

Function: USB Connectors

Jumper Type: 2.00mm pitch 2x5-pin box header.

Pin	Description	Pin	Description
1	+5V	2	GND
3	DATA0-	4	GND
5	DATA0+	6	DATA1+
7	GND	8	DATA1-
9	GND	10	+5V



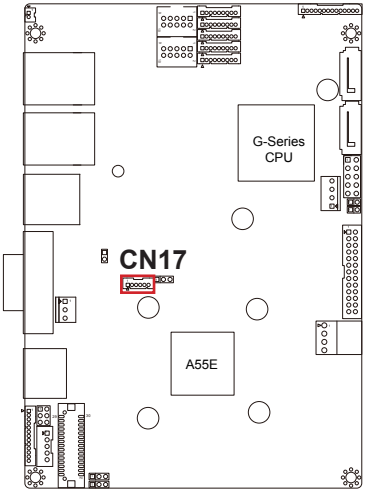


CN17

Function: Keyboard/Mouse Connector

Jumper Type: 1x6-pin CVILUX 1.25mm CI4406P1V00-LF 4-wall connector.

Pin	Description
1	KB_DATA
2	KB_CLK
3	GND
4	+5V
5	MS_DATA
6	MS_CLK

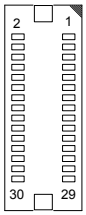


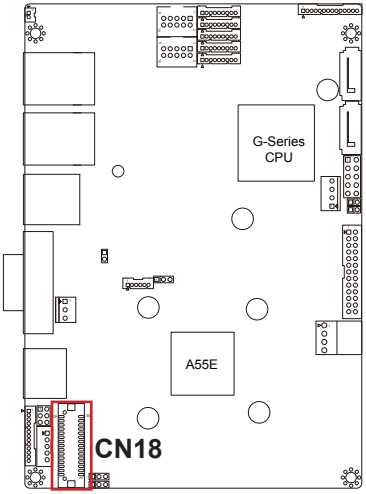
CN18

Function: LVDS Connector

Jumper Type: ACES 1.25mm 87209-3040-06 connector, supporting 24-bit dual channels.

Pin	Description	Pin	Description
2	LVDS_BKLCTL	1	LVDS_BKLEN
4	GND	3	PPVCC
6	LVDS_TXLCLK	5	LVDS_TXLCLK#
8	GND	7	PPVCC
10	LVDS_TXL0	9	LVDS_TXL0#
12	LVDS_TXL1	11	LVDS_TXL1#
14	LVDS_TXL2	13	LVDS_TXL2#
16	LVDS_TXL3	15	LVDS_TXL3#
18	LVDS_DDCPCLK	17	LVDS_DDCPDATA
20	LVDS_TXU0	19	LVDS_TXU0#
22	LVDS_TXU1	21	LVDS_TXU1#
24	LVDS_TXU2	23	LVDS_TXU2#
26	LVDS_TXU3	25	LVDS_TXU3#
28	GND	27	PPVCC
30	LVDS_TXUCLK	29	LVDS_TXUCLK#

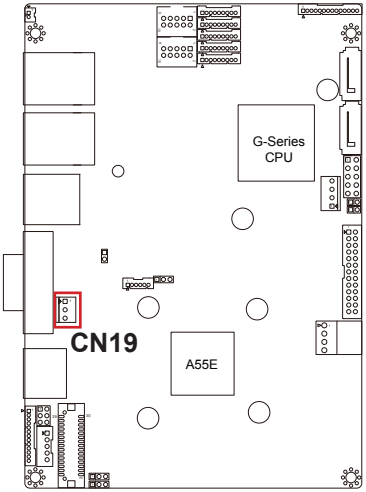




CN19

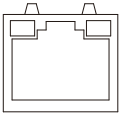
Function: FAN Connector

Pin	Description
1	GND
2	Fan control
3	Fan tachometer



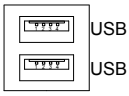
CN20~21

Function: GbE RJ-45 Connectors
Jumper Type: These connectors support Gigabit Ethernet.



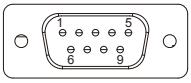
CN22

Function: USB Connector
Jumper Type: double stack USB type A connector



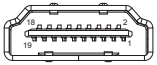
CN28

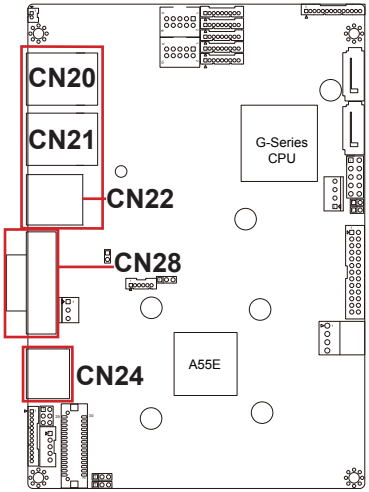
Function: COM2 Connector
Jumper Type: external 9-pin D-sub male connector



CN24

Function: HDMI Connector
Jumper Type: HDMI 19-pin female



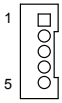


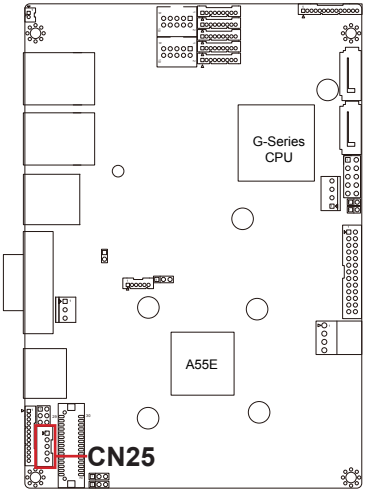
CN25

Function: Backlight Connector

Jumper Type: 2.00mm pitch 1x5-pin box wafer connector

Pin	Description
1	LVDS Voltage Select
2	LVDS Backlight Control
3	GND
4	GND
5	LVDS Backlight Enable



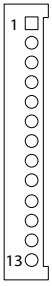


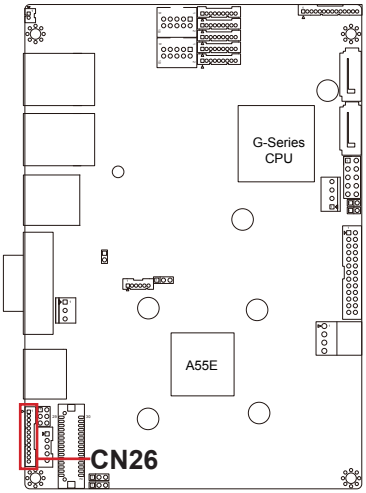
CN26

Function: VGA Connector

Jumper Type: 1x13-pin ACES 1.25mm 86801-13 4-wall connector.

Pin	Description
1	VSYNC
2	HSYNC
3	GND
4	DDC_SCL
5	DDC_SDA
6	GND
7	BLUE
8	GND
9	GREEN
10	GND
11	RED
12	GND
13	+5V



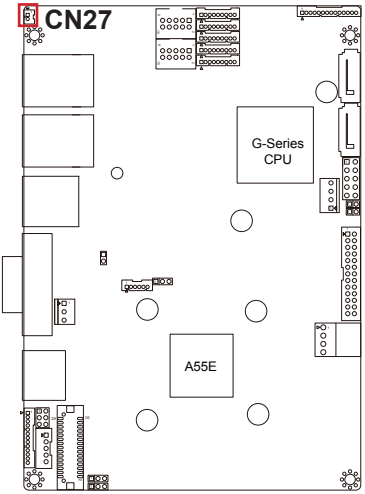


CN27

Function: Battery Connector

Jumper Type: 1x2-pin 1.25mm 85205-02X01 4-wall connector.

Pin	Description
1	RTCBAT
2	GND

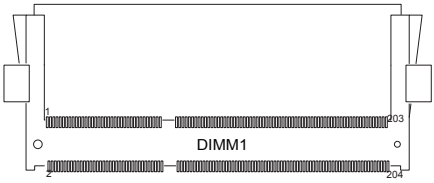


CN32

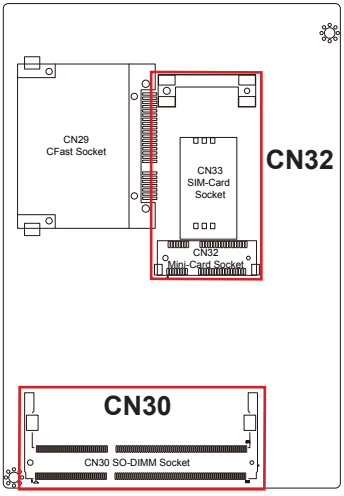
Function: Mini-Card Socket

CN30

Function: DDR3 SO-DIMM Socket



Bottom Side

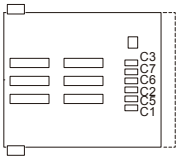


CN33

Function: SIM Card Socket

Jumper Type: Foxconn WL618E2-U05-7F CX1 socket.

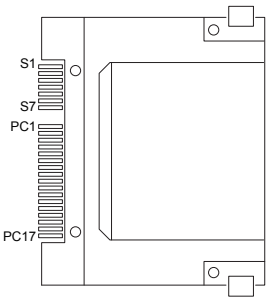
Pin	Description
C1	VCC
C2	RST
C3	CLK
C5	GND
C6	VPP
C7	I/O



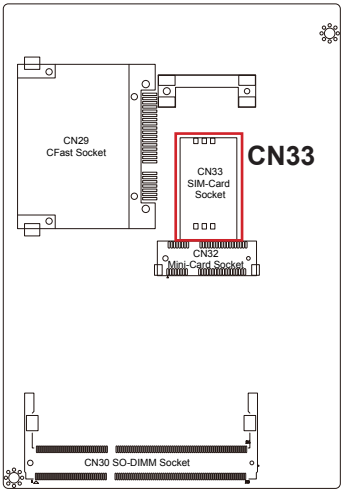
CN29

Function: CFast Socket

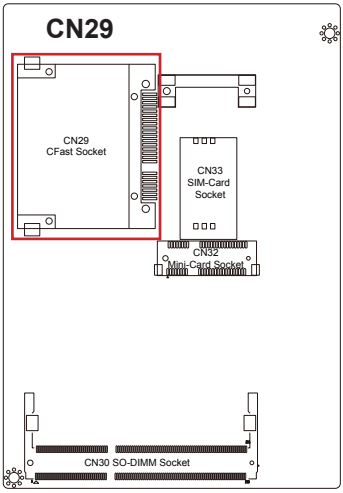
Pin	Description	Pin	Description
S1	SGND1	PC1	CDI
S2	TXP	PC2	GND
S3	TXN	PC3	TBD
S4	SGND2	PC4	TBD
S5	RXN	PC5	TBD
S6	RXP	PC6	TBD
S7	SGND	PC7	GND
		PC8	LED1
		PC9	LED2
		PC10	IO1
		PC11	IO2
		PC12	IO3
		PC13	3.3V
		PC14	3.3V
		PC15	GND
		PC16	GND
		PC17	CD0



Bottom Side



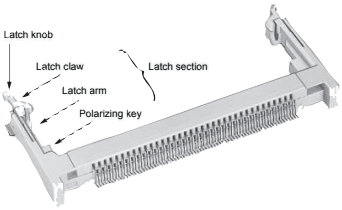
Bottom Side

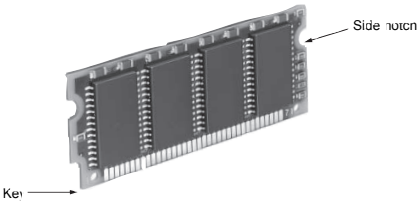


Chapter 3

Installation & Maintenance

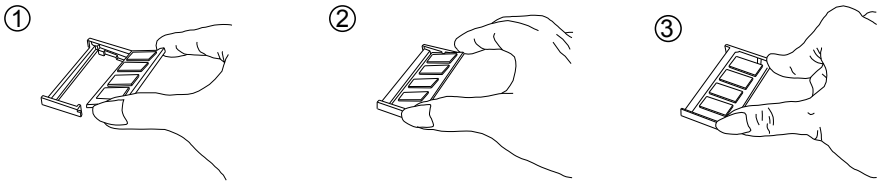
3.1 Installing the Memory





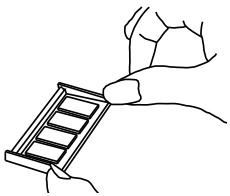
To install the memory module, locate the SO-DIMM slot on bottom side and perform as below:

1. Adjust the socket polarizing key and the memory key to the same direction.
2. Insert the memory obliquely. Moreover, lay the memory in parallel to the opening at angle of 20° to 30°, and softly insert the memory so as to hit the socket bottom. Stopping insertion halfway will result in improper insertion.
3. Applying the memory side notch in parallel to the socket bottom so that the memory position cannot be displaced, press the memory side notch up, and fix it to the latch portion at both socket edges. Press the memory side notch, and release the notch with a snap “click” tone, if the printed memory exceeds the latch claw head.



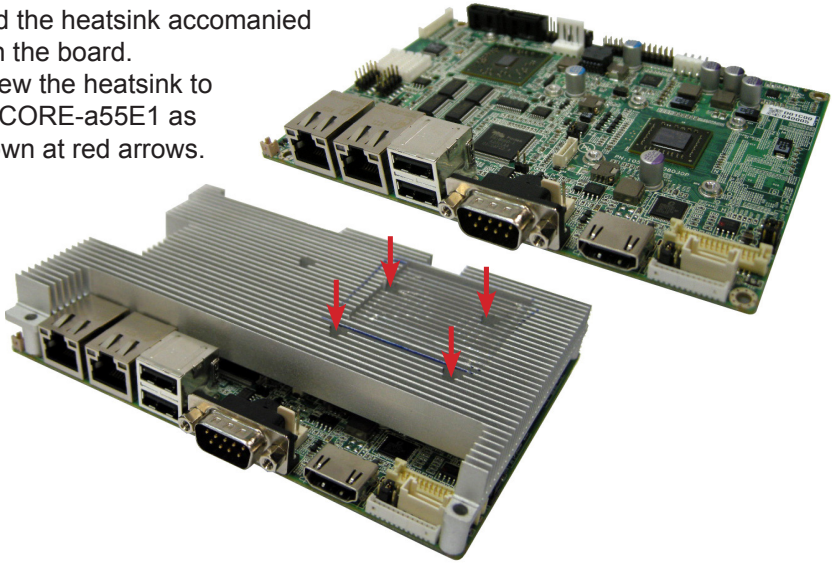
Procedures for memory extraction

Apply the thumb nail to the latch knob at both socket edges. Forcibly widen the latch knobs to right and left ways, and release the latch. Then draw the memory out along an angle where the memory is raised.



3.2 Installing the Heatsink

1. Find the heatsink accomanied with the board.
2. Screw the heatsink to EmCORE-a55E1 as shown at red arrows.

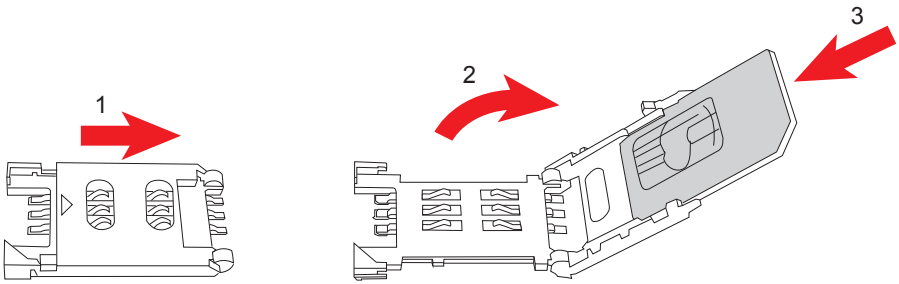


3.3 Installing CFast Card

1. Position CFast card slot on bottom side.
2. Push a CFast card into the slot until it's fixed.
3. Push the card again to eject it.

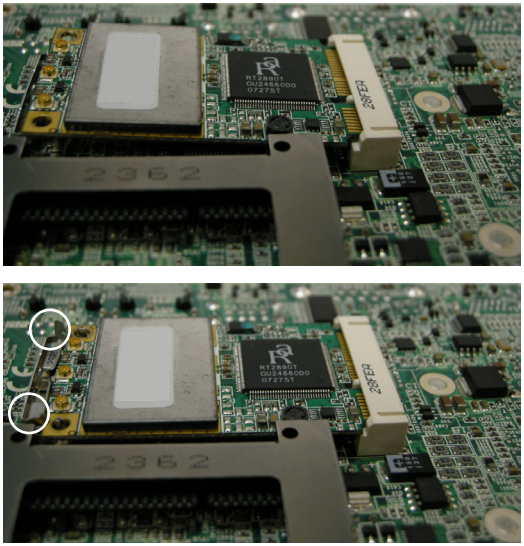
3.4 Installing SIM Card

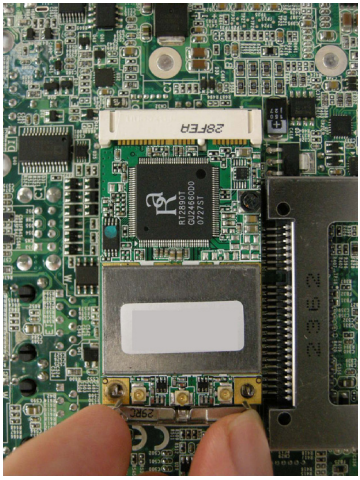
1. Position SIM card on bottom side.
2. Slightly press SIM socket lid and move it rightards. Lift socket lid.
3. Slip SIM card along grooves on lid's inside as below, close it and move leftwards.



3.5 Installing Mini-card

1. Locate Mini-card socket on bottom side.
2. Insert a Mini-card into the slot at an angle. Remember to align the notch with the break on slot.
3. Press down another end of the Mini-card to have it fixed by two latches at the corner. To take off the card, pinch latches inwards before unpluging it.





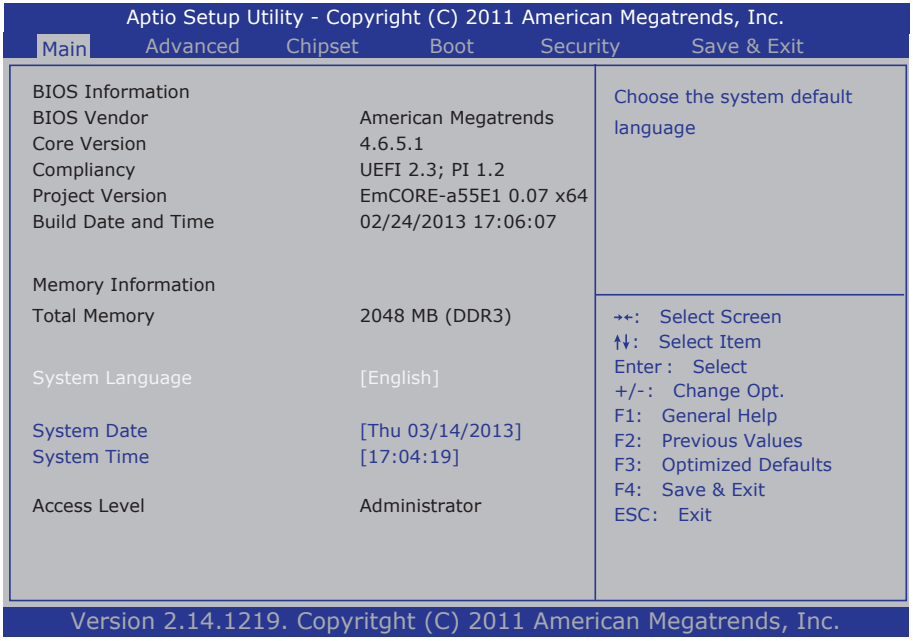
Chapter 4

BIOS

4.1 Main

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS RAM of the system stores the Setup utility and configurations. When you turn on the computer, the AMI BIOS is immediately activated. To enter the BIOS SETUP UTILITY, press **"Delete"** once the power is turned on. When the computer is shut down, the battery on the motherboard supplies the power for BIOS RAM.

The **Main Setup** screen lists the following information:



Item	Description
System Language	Choose the system default language
System Date	Set the system date. Use Tab to switch between Data elements. Note that the 'Day' automatically changes when you set the date. ► The date format is: **Day:** Sun to Sat **Month:** 1 to 12 **Date:** 1 to 31 **Year:** 1998 to 2099

System Time	Set the system time. Use Tab to switch between Time elements. ► The time format is: **Hour:** 00 to 23 **Minute:** 00 to 59 **Second:** 00 to 59

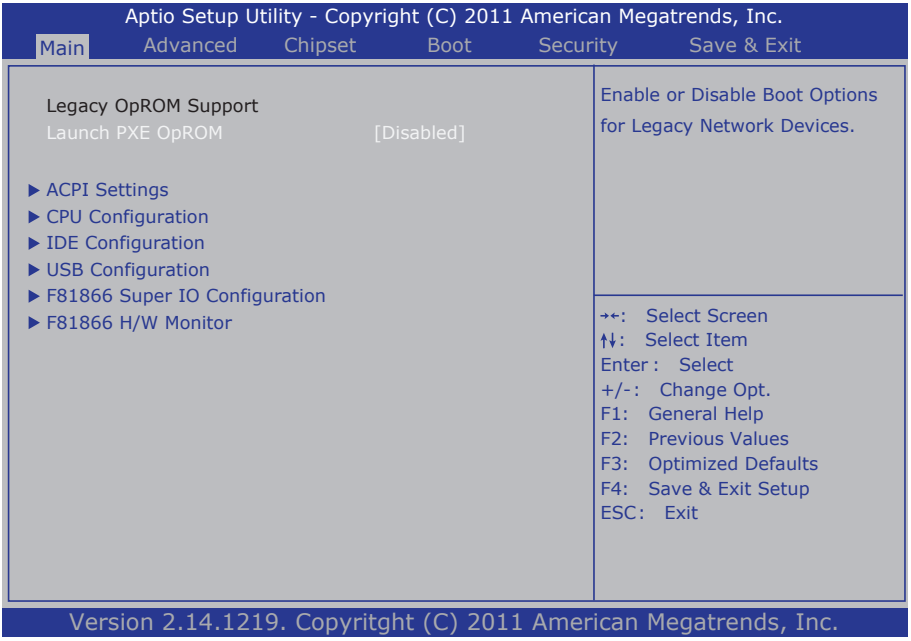
Key Commands

BIOS Setup Utility is mainly a key-based navigation interface. Please refer to the following key command instructions for navigation process.

Keystroke	Function
◄ ►	Move to highlight a particular configuration screen from the top menu bar / Move to highlight items on the screen
▼ ▲	Move to highlight previous/next item
Enter	Select and access a setup item/field
Esc	On the Main Menu – Quit the setup and not save changes into CMOS (a message screen will display and ask you to select “OK” or “Cancel” for exiting and discarding changes. Use “←” and “→” to select and press “Enter” to confirm) On the Sub Menu – Exit current page and return to main menu
Page Up / +	Increase the numeric value on a selected setup item / make change
Page Down -	Decrease the numeric value on a selected setup item / make change
F1	Activate “General Help” screen
F4	Save the changes that have been made in the setup and exit. (a message screen will display and ask you to select “OK” or “Cancel” for exiting and saving changes. Use “←” and “→” to select and press “Enter” to confirm)

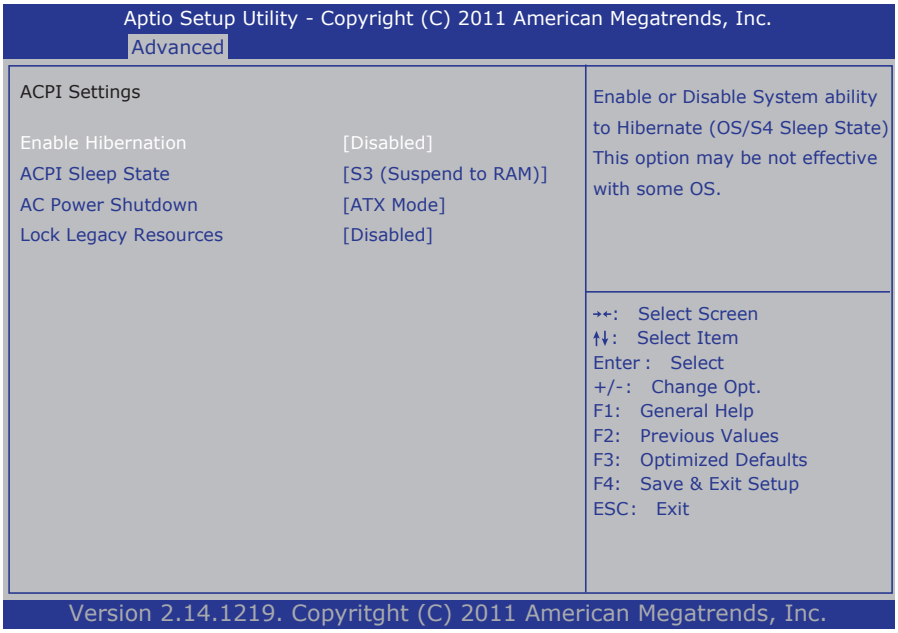
4.2 Advanced

The “Advanced” setting page provides you the options to configure the details of your hardware, such as ACPI, CPU, IDE, USB and Super IO.



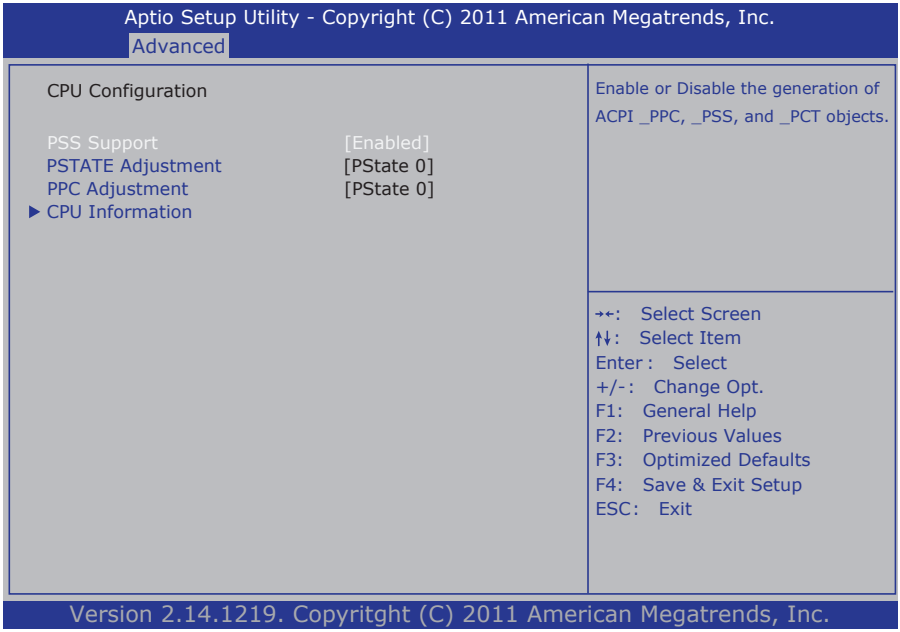
Item	Description
ACPI Settings	See Section 4.2.1
CPU Configuration	See Section 4.2.2
IDE Configuration	See Section 4.2.3
USB Configuration	See Section 4.2.4
F81866 Super IO Configuration	See Section 4.2.5
F81866 H/M Monitor	See Section 4.2.6

4.2.1 ACPI Settings



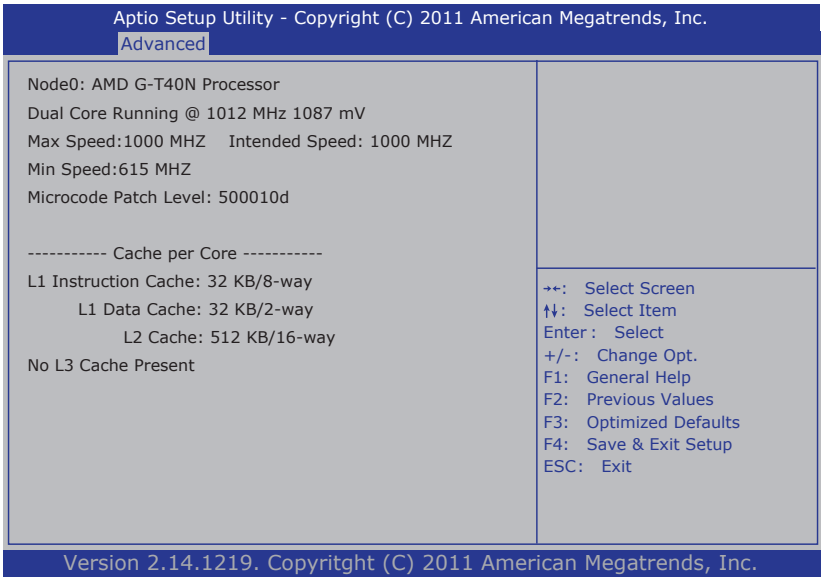
Item	Description
Enable Hibernation	**Enable** (default) or **Disable** system ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed. ► Options: **Suspend Disabled**, **S3 (Suspend to RAM)** (default).
AC Power Shutdown	ATX: OS will turn off system power when shutdown. AT: OS show it is now safe to turn off your computer. NOTE: AT mode will not support S3 & S4. ► Options: **AT Mode**, **ATX Mode** (default).
Lock Legacy Resources	**Enable** or **disable** (default) Lock of Legacy Resources.

4.2.2 CPU Configuration

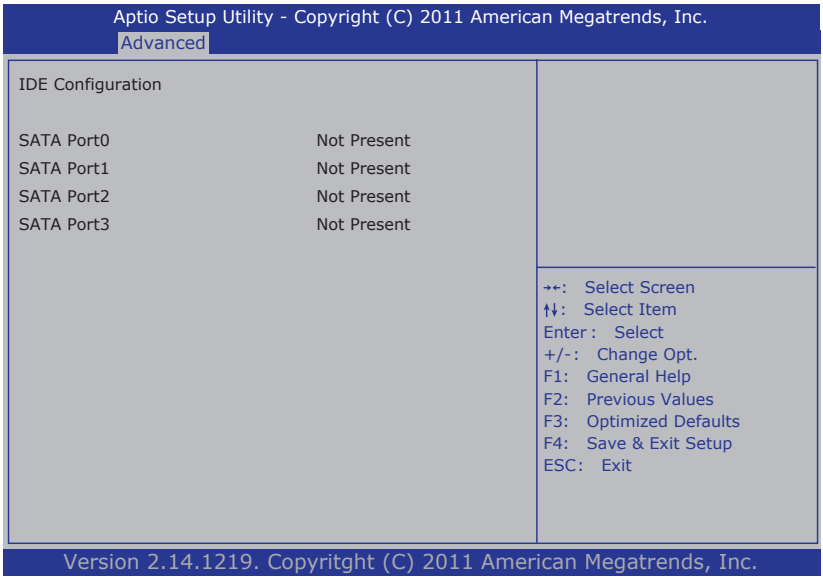


Item	Description
PSS Support	**Enable** (default) or **Disable** the generation of ACPI _PPC, _PSS, and _PCT objects.
PSTATE Adjustment	Provide to adjust startup P-state level. ► Options: **PState 0** (default), **PState 1** and **PState 2**.
PPC Adjustment	Provide to adjust startup _PPC objects. ► Options: **PState 0** (default), **PState 1** and **PState 2**.
CPU Information	View Memory Information related to Node 0, as shown in next page.

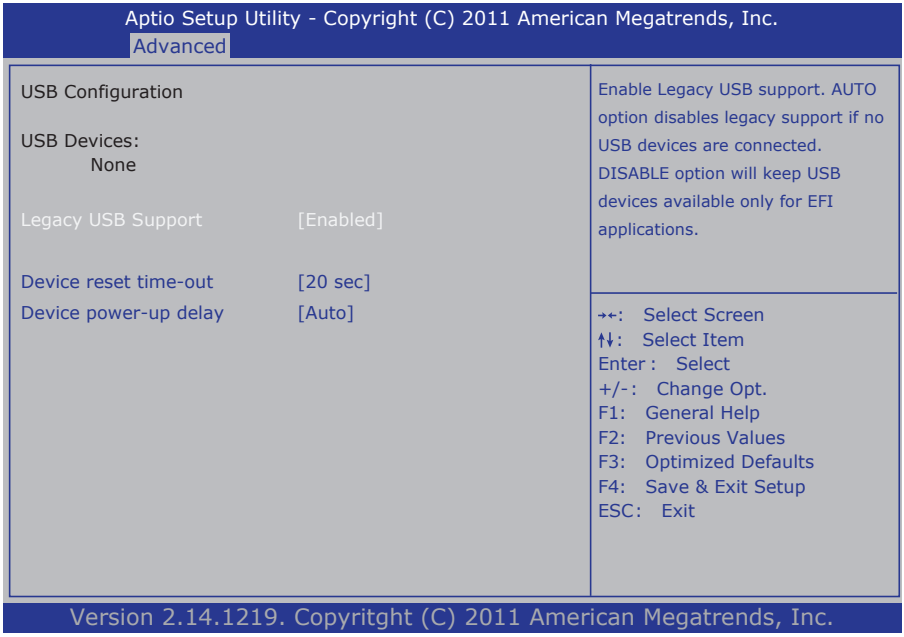
CPU Information



4.2.3 IDE Configuration

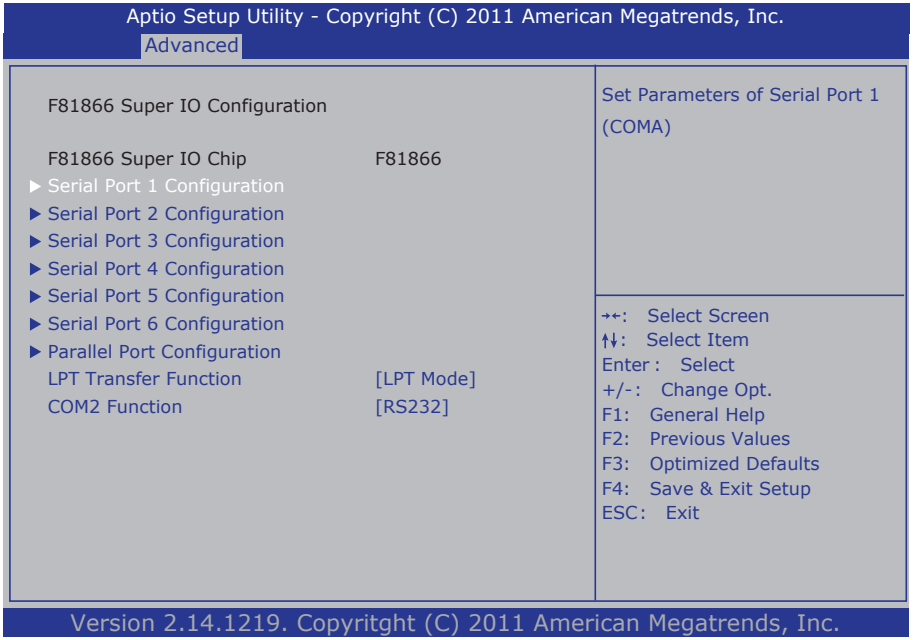


4.2.4 USB Configuration



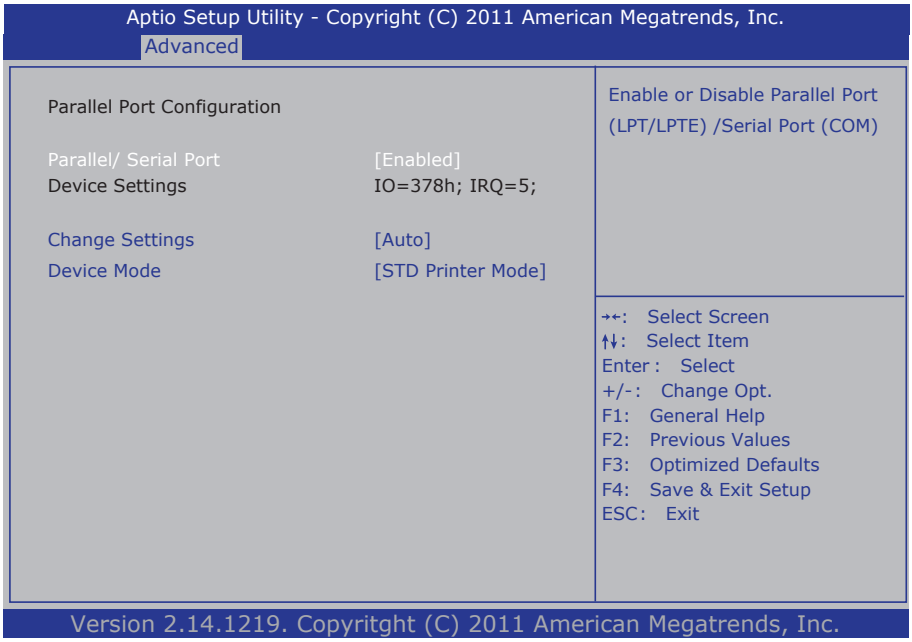
Item	Description
Legacy USB Support	**Enables** (default) Legacy USB support. **AUTO** option disables legacy support if no USB devices are connected. **DISABLE** option will keep USB devices available only for EFI applications.
Device reset time-out	USB mass storage device Start Unit command time-out. ► Options: **10 sec**, **20 sec** (default), **30 sec** and **40 sec**.
Device power-up delay	Maximum time the device will take before it properly reports itself to the host controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from hub descriptor. ► Options: **Auto** (default) and **Manual**.

4.2.5 F81866 Super IO Configuration



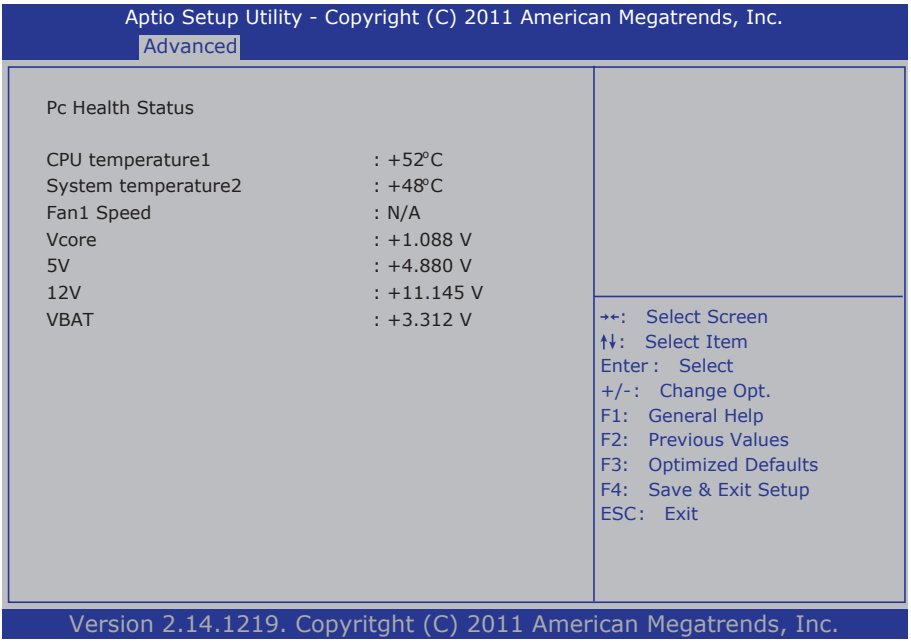
Item	Description
Serial Port 1~6 Configuration	See next page.
Parallel Port Configuration	See next page.
LPT Transfer Function	Select LPT or GPIO Mode NOTE: Select GPIO mode to use DIO. Refer to Appendix E: Digital I/O Setting on page 70. ► Options: **LPT Mode** (default) and **GPIO Mode**.
COM2 Function	Select RS232/422/485 ► Options: **RS232** (default), **RS422** and **RS485**.

Serial Port 1~6/ Parallel Configuration

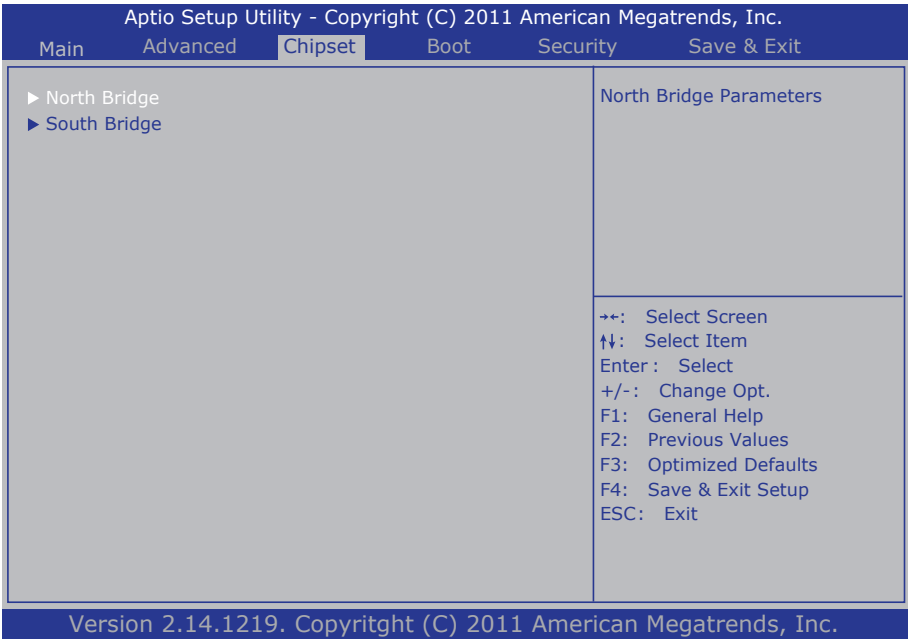


Item	Description
Serial Port	**Enable** (default) or **Disable** serial port (COM).
Parallel Port	**Enable** (default) or **Disable** Parallel port (LPT/ LPTE).
Change Settings	Select an optimal setting for Super IO device. ► Options: **Auto** (default)/ **IO=3F8h; IRQ=4**,/ **IO=3F8h; IRQ=3,4,5,6,7,10,11,12**/ **IO=2F8h; IRQ=3,4,5,6,7,10,11,12**/ **IO=3E8h; IRQ=3,4,5,6,7,10,11,12**/ **IO=2E8h; IRQ=3,4,5,6,7,10,11,12**/
Device Mode (only for Parallel Port Configuration)	Change the Printer Port mode. ► Options: **STD Printer Mode** (default), **SPP Mode**, **EPP-1.9 and SPP Mode**, **EPP-1.7 and SPP Mode**, **ECP Mode**, **ECP and EPP 1.9 Mode**, **ECP and EPP 1.7 Mode**.

4.2.6 F81866 H/W Monitor

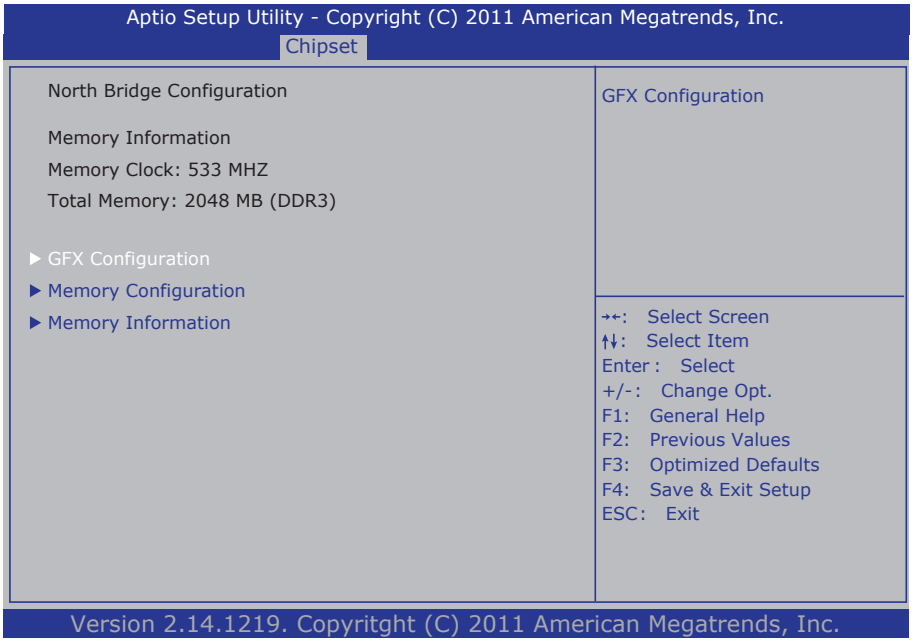


4.3 Chipset



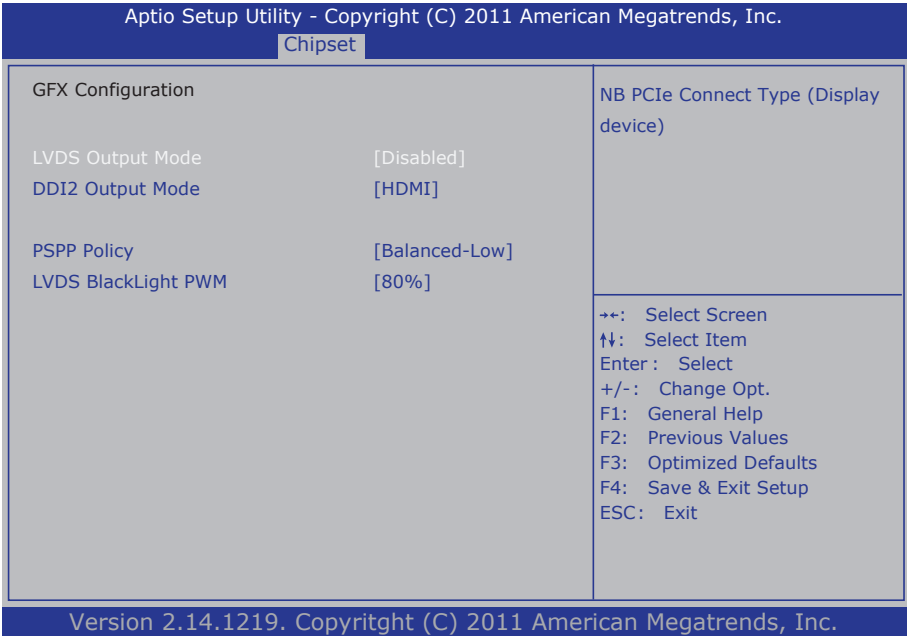
Item	Description
North Bridge	See Section 4.3.1
South Bridge	See Section 4.3.2

4.3.1 North Bridge



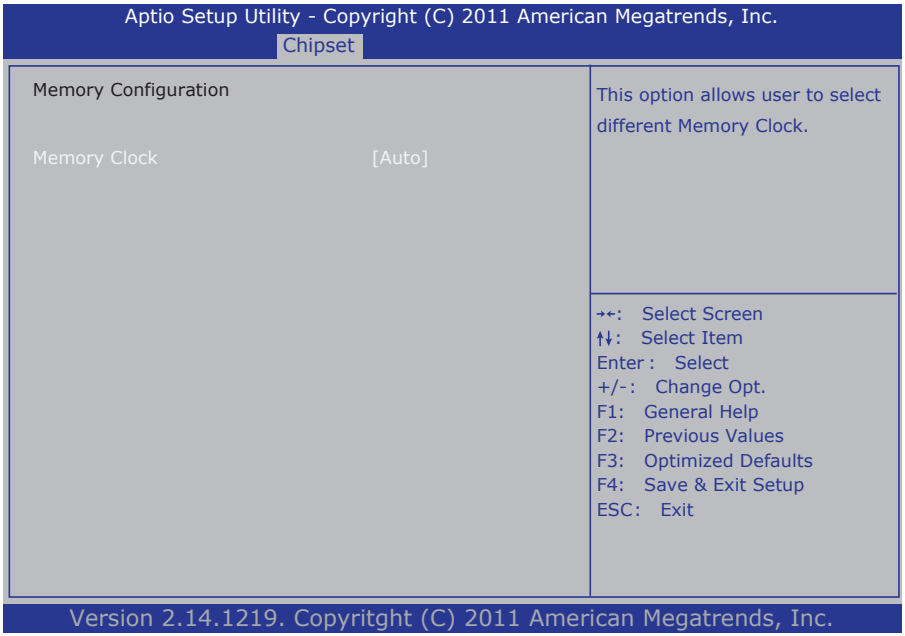
Item	Description
GFX Configuration	See GFX Configuration page
Memory Configuration	See Memory Configuration page
Memory Information	See Memory Information page

GFX Configuration



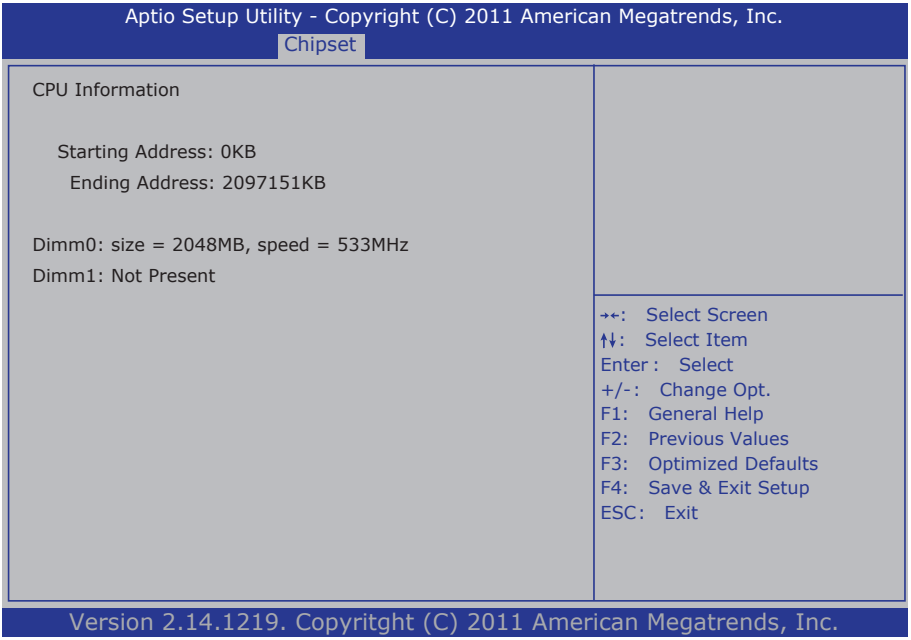
Item	Description
LVDS Output Mode	NB PCIe Connect Type (Display device) ► Options: **Disabled** (default) and **Enabled**.
DDI2 Output Mode	NB PCIe Connect Type (Display device) ► Options: **HDMI** (default) and **Disabled**.
PSPP Policy	PCIe speed power policy ► Options: **Disabled**, **Performance**, **Balanced-High**, **Balanced-Low** (default) and **Power Saving**.
LVDS BlackLight PWM	► Options: **20%**, **40%**, **60%**, **80%** (default) and **100%**.

Memory Configuration

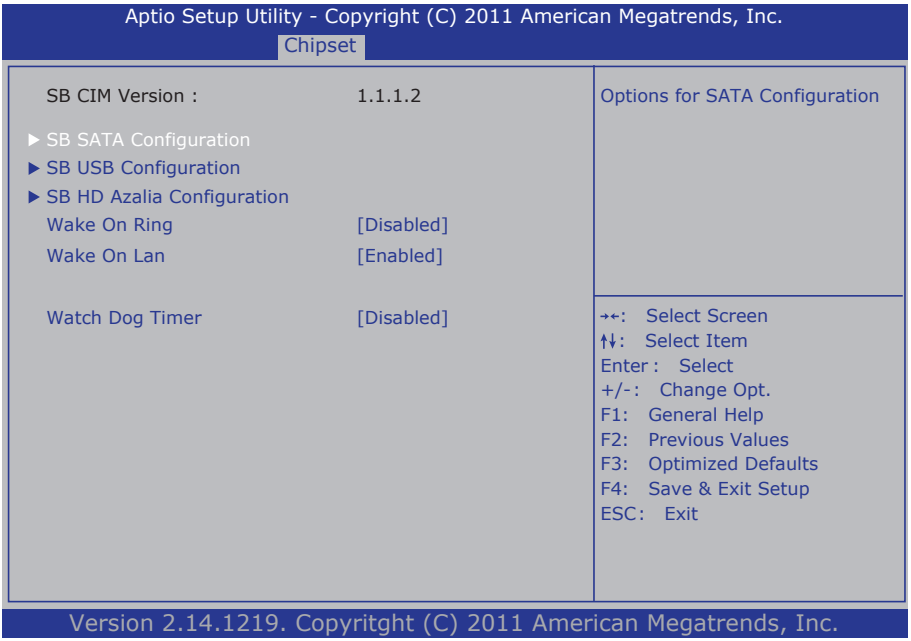


Item	Description
Memory Clock	This option allows user to select different Memory Clock. ► Options: **Auto** (default), **400MHz**, **533MHz**, **667MHz**

Memory Information

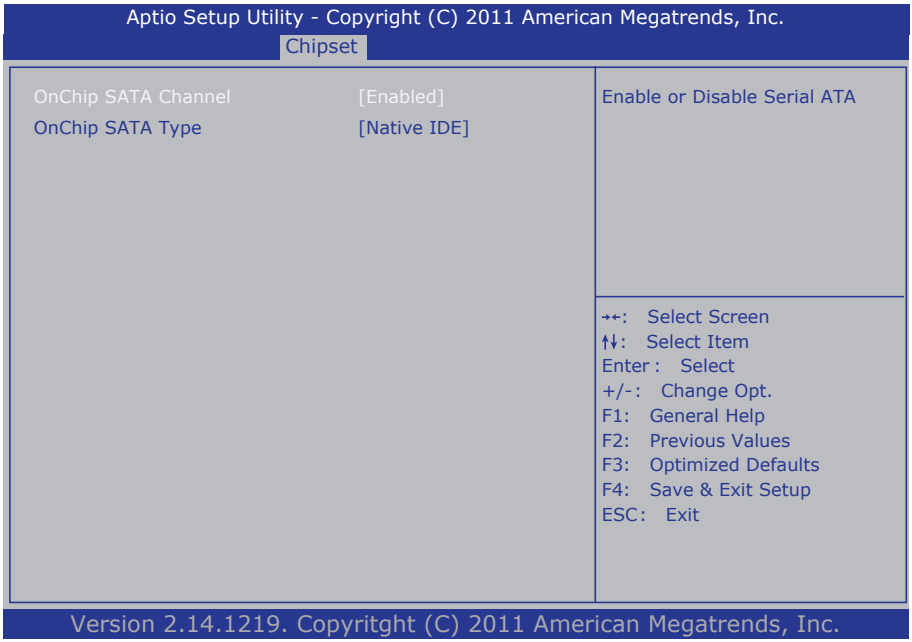


4.3.2 South Bridge



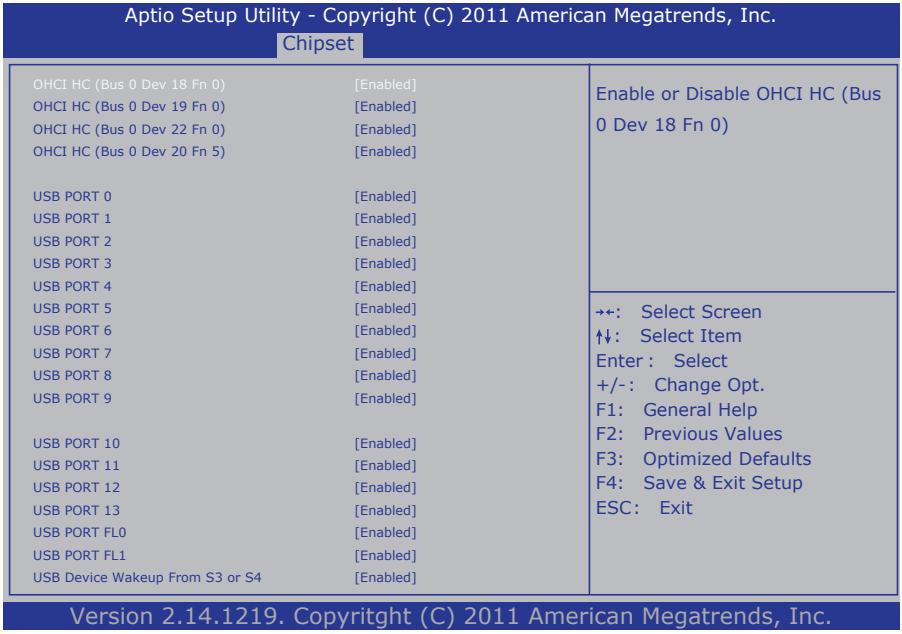
Item	Description
SB SATA Configuration	See SB SATA Configuration page
SB USB Configuration	See SB USB Configuration page
SB HD Azalia Configuration	See SB HD Azalia Configuration page
Wake On Ring	► Options: **Disabled** (default) and **Enabled**.
Wake On Lan	► Options: **Disabled** and **Enabled** (default).
Watch Dog Timer	► Options: **Disabled** (default) and **Enabled**.

SB SATA Configuration



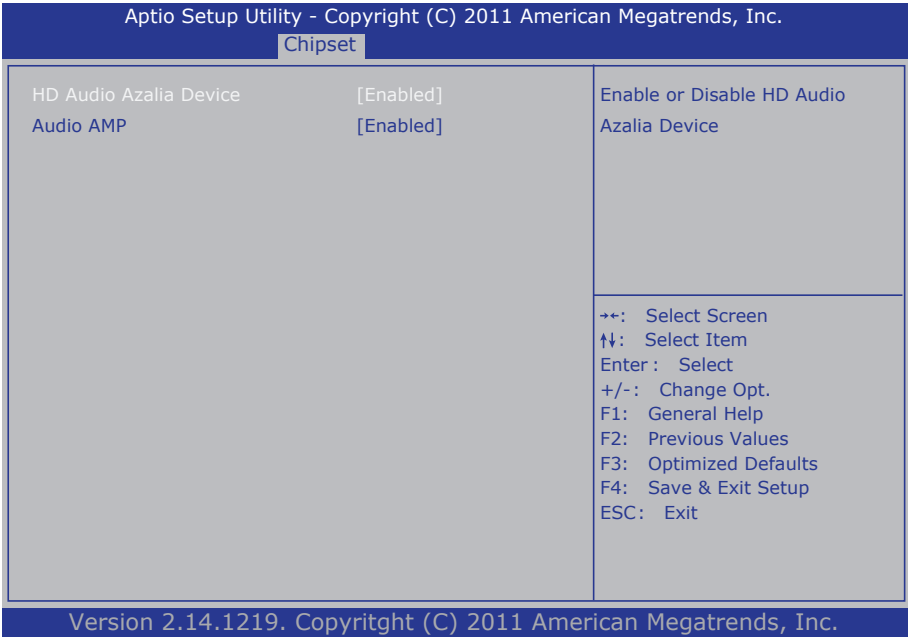
Item	Description
OnChip SATA Channel	**Enable** (default) or **Disable** Serial ATA.
OnChip SATA Type	► Options: **Native IDE** (default), **RAID**, **AHCI**, **Legacy IDE** and **IDE->AHCI**.

SB USB Configuration



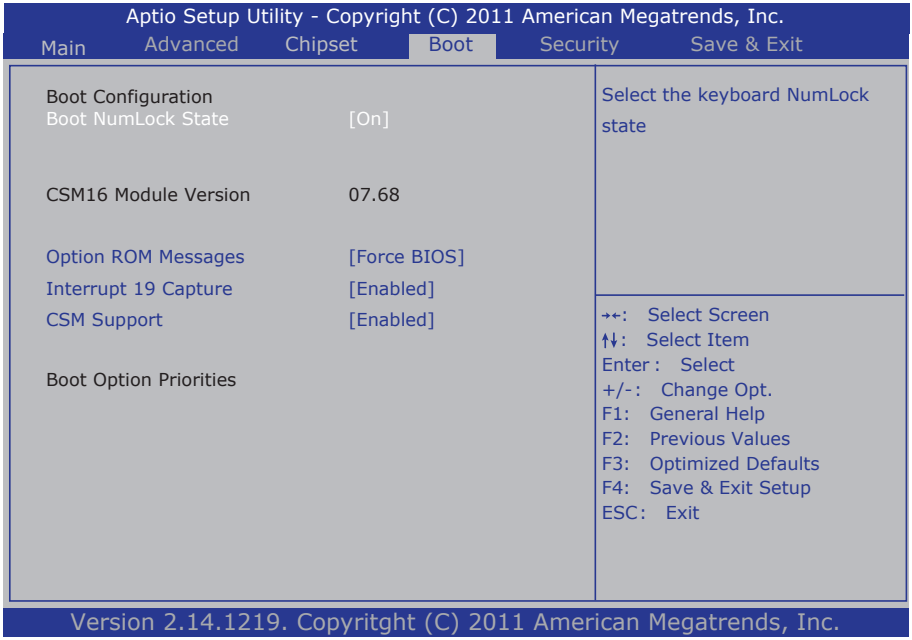
Item	Description
OHCI HC (Bus 0 Dev 18/19/22/20 Fn 0/5)	► Options: **Disabled** and **Enabled** (default).
USB PORT 0~13/ FL0 / FL1	► Options: **Disabled** and **Enabled** (default).
USB Device Wakeup From S3 or S4	► Options: **Disabled** and **Enabled** (default).

SB HD Azalia Configuration



Item	Description
HD Audio Azalia Device	▶ Options: **Disabled** and **Enabled** (default).
Audio AMP	▶ Options: **Disabled** and **Enabled** (default).

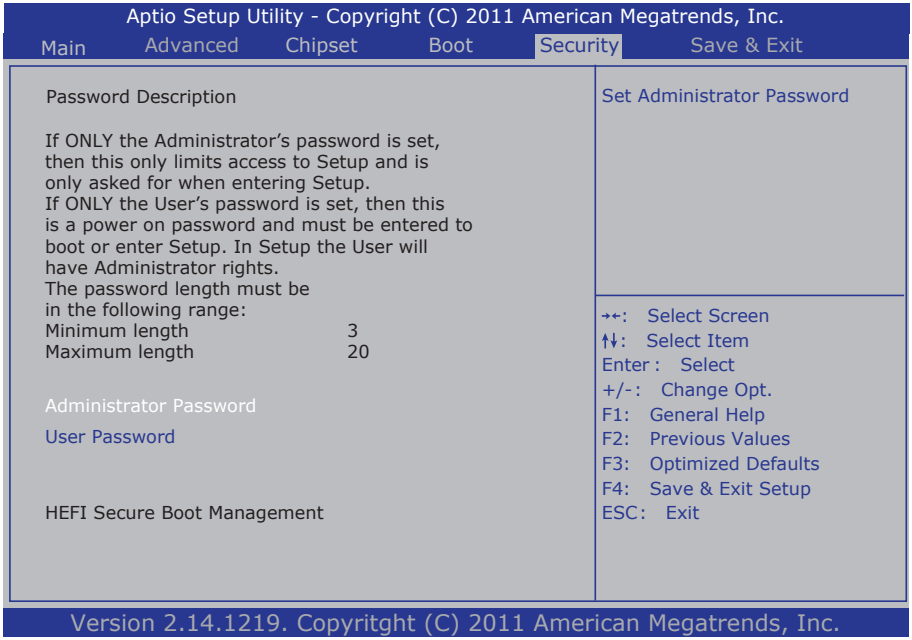
4.4 Boot



Item	Description
Boot NumLock State	Select the keyboard NumLock state ► Options: **On** (default) and **Off**.
Option ROM Messages	Set display mode for Option ROM ► Options: **Force BIOS** (default) and **Keep Current**.
Interrupt 19 Capture	Allows Option ROMs to trap Int 19 ► Options: **Disabled** and **Enabled** (default).
CSM Support	If Auto is selected, based on OS, CSM will be enabled/disabled automatically. ► Options: **Disabled**, **Enabled** (default) and **Auto**.

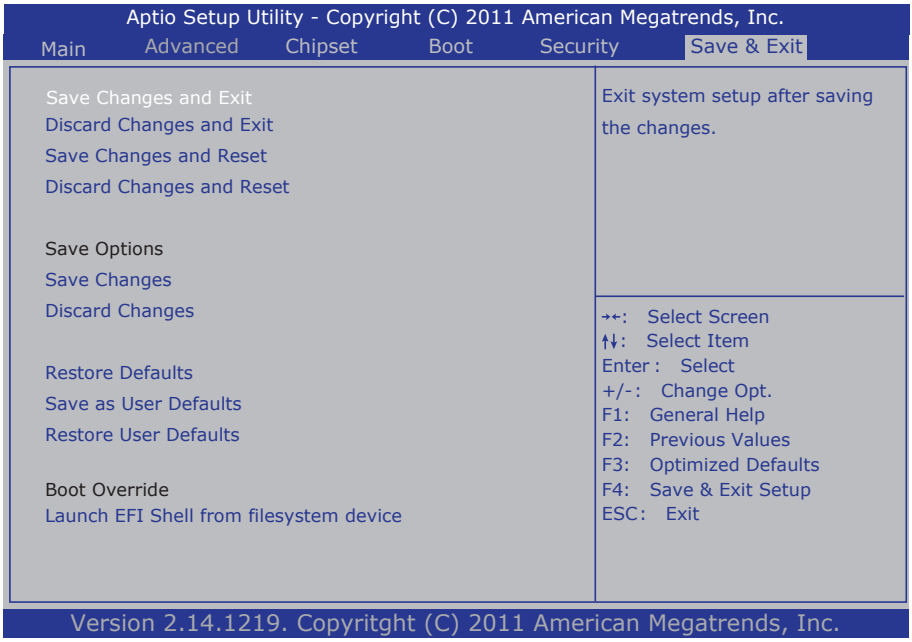
4.5 Security

The **Security** menu sets up the administrator and user password. Once an administrator password is set up, this BIOS SETUP utility is limited to access and will ask for the password each time any access is attempted.



Item	Description
Administrator/User Password	To set up an administrator password: 1. Select **Administrator Password**. The screen then pops up an **Create New Password** dialog. 2. Enter your desired password that is no less than 3 characters and no more than 20 characters. 3. Hit [Enter] key to submit.

4.6 Save & Exit



Item	Description
Save Changes and Exit	Exit system setup after saving the changes. ► Enter the item and then a dialog box pops up: **Save configuration and exit? (Yes/ No)**
Discard Changes and Exit	Exit system setup without saving any changes. ► Enter the item and then a dialog box pops up: **Quit without saving? (Yes/ No)**
Save Changes and Reset	Reset the system after saving the changes. ► Enter the item and then a dialog box pops up: **Save configuration and reset? (Yes/ No)**
Discard Changes and Reset	Reset system setup without saving any changes. ► Enter the item and then a dialog box pops up: **Reset without saving? (Yes/ No)**

Save Changes	Save Changes done so far to any of the setup options. ► Enter the item and then a dialog box pops up: **Save configuration? (Yes/ No)**
Discard Changes	Discard Changes done so far to any of the setup options. ► Enter the item and then a dialog box pops up: **Load previous values? (Yes/ No)**
Restore Defaults	Restore/Load default values for all the setup options. ► Enter the item and then a dialog box pops up: **Load optimized defaults? (Yes/ No)**
Save as USER Defaults	Save the changes done so far as User Defaults. ► Enter the item and then a dialog box pops up: **Save configuration? (Yes/ No)**
Restore User Defaults	Restore the User Defaults to all the setup options. ► Enter the item and then a dialog box pops up: **Restore user defaults? (Yes/ No)**
Launch EFI Shell from filesystem device	Attempts to Launch EFI Shell application (Shellx64.efi) from one of the available filesystem devices

4.7 AMI BIOS Checkpoints

4.7.1 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

4.7.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed

0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.

0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available

0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)

0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable

0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found

0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

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Appendix

Appendix A: I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.
The following table lists the I/O port addresses used.

Address	Device Description
0x0000D000-0x0000DFFF	PCI standard PCI-to-PCI bridge
0x0000D000-0x0000DFFF	Ethernet Controller
0x000002E8-0x000002EF	Communications Port (COM4)
0x00000228-0x0000022F	Communications Port (COM5)
0x00000220-0x00000227	Communications Port (COM6)
0x00000061-0x00000061	System speaker
0x00000000-0x000003AF	PCI bus
0x00000000-0x000003AF	Motherboard resources
0x00000000-0x000003AF	Direct memory access controller
0x000003E0-0x00000CF7	PCI bus
0x000003B0-0x000003DF	PCI bus
0x000003B0-0x000003DF	Standard VGA graphics card
0x00000D00-0x0000FFFF	PCI bus
0x00000070-0x00000071	System CMOS/real time clock
0x0000F190-0x0000F197	Standard Dual Channel PCI IDE Controller
0x0000F180-0x0000F183	Standard Dual Channel PCI IDE Controller
0x0000F170-0x0000F177	Standard Dual Channel PCI IDE Controller
0x0000F160-0x0000F163	Standard Dual Channel PCI IDE Controller
0x0000F150-0x0000F15F	Standard Dual Channel PCI IDE Controller
0x0000F100-0x0000F10F	Standard Dual Channel PCI IDE Controller
0x00000010-0x0000001F	Motherboard resources
0x00000022-0x0000003F	Motherboard resources
0x00000044-0x0000005F	Motherboard resources
0x00000062-0x00000063	Motherboard resources
0x00000065-0x0000006F	Motherboard resources
0x00000072-0x0000007F	Motherboard resources
0x00000080-0x00000080	Motherboard resources

0x00000084-0x00000086	Motherboard resources
0x00000088-0x00000088	Motherboard resources
0x0000008C-0x0000008E	Motherboard resources
0x00000090-0x0000009F	Motherboard resources
0x000000A2-0x000000BF	Motherboard resources
0x000000E0-0x000000EF	Motherboard resources
0x000004D0-0x000004D1	Motherboard resources
0x00000A00-0x00000A0F	Motherboard resources
0x00000A10-0x00000A1F	Motherboard resources
0x00000A20-0x00000A2F	Motherboard resources
0x000001F0-0x000001F7	ATA Channel 0
0x000003F6-0x000003F6	ATA Channel 0
0x0000040B-0x0000040B	Motherboard resources
0x000004D6-0x000004D6	Motherboard resources
0x00000C00-0x00000C01	Motherboard resources
0x00000C14-0x00000C14	Motherboard resources
0x00000C50-0x00000C51	Motherboard resources
0x00000C52-0x00000C52	Motherboard resources
0x00000C6C-0x00000C6C	Motherboard resources
0x00000C6F-0x00000C6F	Motherboard resources
0x00000CD0-0x00000CD1	Motherboard resources
0x00000CD2-0x00000CD3	Motherboard resources
0x00000CD4-0x00000CD5	Motherboard resources
0x00000CD6-0x00000CD7	Motherboard resources
0x00000CD8-0x00000CDF	Motherboard resources
0x00000800-0x0000089F	Motherboard resources
0x00000B20-0x00000B3F	Motherboard resources
0x00000900-0x0000090F	Motherboard resources
0x00000910-0x0000091F	Motherboard resources
0x0000FE00-0x0000FEFE	Motherboard resources
0x00000170-0x00000177	ATA Channel 1

0x00000376-0x00000376	ATA Channel 1
0x0000F000-0x0000F0FF	Standard VGA graphics card
0x000003C0-0x000003DF	Standard VGA graphics card
0x000000F0-0x000000FF	Numeric data processor
0x00000020-0x00000021	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x00000040-0x00000043	System timer
0x00000081-0x00000083	Direct memory access controller
0x00000087-0x00000087	Direct memory access controller
0x00000089-0x0000008B	Direct memory access controller
0x0000008F-0x0000008F	Direct memory access controller
0x000000C0-0x000000DF	Direct memory access controller
0x00000060-0x00000060	Standard PS / 2 Keyboard
0x00000064-0x00000064	Standard PS / 2 Keyboard
0x00000378-0x0000037F	Printer Port (LPT1)
0x0000E000-0x0000EFFF	PCI standard PCI-to-PCI bridge
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x000003E8-0x000003EF	Communications Port (COM3)

Appendix B: Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System timer
IRQ 1	Standard PS / 2 Keyboard
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 6	Communications Port (COM6)
IRQ 7	Communications Port (COM3)
IRQ 8	System CMOS/real time clock
IRQ 11	Communications Port (COM4)
IRQ 11	Ethernet Controller
IRQ 12	Microsoft PS/2 Mouse
IRQ 13	Numeric data processor
IRQ 14	ATA Channel 0

Appendix C: BIOS Memory Mapping

Address	Device Description
0xFEB49000-0xFEB49FFF	Standard OpenHCD USB Host Controller
0xFE900000-0xFE9FFFFF	PCI standard PCI-to-PCI bridge
0xFE900000-0xFE9FFFFF	Ethernet Controller
0xFEB4A000-0xFEB4AFFF	Standard OpenHCD USB Host Controller
0xA0000-0xBFFFF	PCI bus
0xA0000-0xBFFFF	Standard VGA graphics card
0xC0000-0xDFFFF	PCI bus
0x80000000-0xFFFFFFFF	PCI bus
0xFEB4F000-0xFEB4F3FF	Standard Dual Channel PCI IDE Controller
0xFE920000-0xFE923FFF	Ethernet Controller
0xE0000000-0xEFFFFFFF	System board

0xFEB4D000-0xFEB4D0FF	Standard Enhanced PCI to USB Host Controller
0x68000000-0x7FFFFFFF	Motherboard resources
0xFEC00000-0xFEC00FFF	Motherboard resources
0xFEE00000-0xFEE00FFF	Motherboard resources
0xFED80000-0xFED8FFFF	Motherboard resources
0xFED61000-0xFED70FFF	Motherboard resources
0xFEC10000-0xFEC10FFF	Motherboard resources
0xFED00000-0xFED00FFF	Motherboard resources
0xFED00000-0xFED00FFF	High Precision Event Timer, HPET
0xFFC00000-0xFFFFFFFF	Motherboard resources
0xFEB4B000-0xFEB4B0FF	Standard Enhanced PCI to USB Host Controller
0xD0000000-0xDFFFFFFF	Standard VGA graphics card
0xFEB00000-0xFEB3FFFF	Standard VGA graphics card
0xFEB48000-0xFEB480FF	Standard Enhanced PCI to USB Host Controller
0xFEB44000-0xFEB47FFF	High Definition Audio Controller
0xFEB4E000-0xFEB4EFFF	Standard OpenHCD USB Host Controller
0xFEB40000-0xFEB43FFF	High Definition Audio Controller
0xFEB4C000-0xFEB4CFFF	Standard OpenHCD USB Host Controller
0xFEA00000-0xFEAFFFFF	PCI standard PCI-to-PCI bridge

Appendix D: Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitor the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. The WDT will not be reloaded by an abnormal system, then WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming I/O ports. Below are the source codes written in C, please take them as WDT application example.

```
/*-----  Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

#define SIO_INDEX       0x2E                /* or index = 0x4E */
#define SIO_DATA        0x2F                /* or data  = 0x4F */

/*-----  routing, sub-routing -----*/
void main()
{
         outportb(SIO_INDEX, 0x87);              /* SIO - Enable */
         outportb(SIO_INDEX, 0x87);

         outportb(SIO_INDEX, 0x07);              /* LDN - WDT */
         outportb(SIO_DATA,  0x07);

         outportb(SIO_INDEX, 0x30);              /* WDT - Enable */
         outportb(SIO_DATA,  0x01);

         outportb(SIO_INDEX, 0xF6);              /* WDT - Timeout Value : 5sec */
         outportb(SIO_DATA,  0x05);

         outportb(SIO_INDEX, 0xFA);              /* WDOUT - Enable */
         outportb(SIO_DATA,  0x01);

         outportb(SIO_INDEX, 0xF5);              /* WDT - Configuration */
         outportb(SIO_DATA,  0x31);

         outportb(SIO_INDEX, 0xAA);              /* SIO - Disable */
}
```

Appendix E: Digital I/O Setting

Below are the source codes written in C, please take them for Digital I/O application examples. The default I/O address is 6Eh. But before all, change LPT Transfer Function to ***GPIO Mode*** in Super IO Configuration in BIOS. Refer to 4.2.5 F81866 Super IO Configuration on page 37 for how to do that.

```
/*-----  Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

#define SIO_INDEX       0x2E                /* or index = 0x4E */
#define SIO_DATA        0x2F                /* or data  = 0x4F */

unsigned char DIO_Set(unsigned char oMode, unsigned char oData);

/*-----  routing, sub-routing -----*/
void main()
{
         DIO_Set(0xFF,0xFF);
         delay(2000);

         DIO_Set(0xFF,0x00);
         delay(2000);

         DIO_Set(0xFF,0x55);
         delay(2000);

         DIO_Set(0xFF,0xAA);
         delay(2000);

}

unsigned char DIO_Set(unsigned char oMode, unsigned char oData)
{
    unsigned char iData;

         outportb(SIO_INDEX, 0x87);              /* SIO - Enable */
         outportb(SIO_INDEX, 0x87);

    outportb(SIO_INDEX, 0x07);              /* LDN - GPIO */
    outportb(SIO_DATA,  0x06);

    outportb(SIO_INDEX, 0x30);              /* GPIO - Enable */
    outportb(SIO_DATA,  0x01);

    outportb(SIO_INDEX, 0x88);              /* GPIO5 - Output */
    outportb(SIO_DATA,  oMode);

    outportb(SIO_INDEX, 0x89);              /* GPIO5 - Data */
    outportb(SIO_DATA,  oData);

    outportb(SIO_INDEX, 0x8A);              /* GPIO5 - Status */
```

```
    iData = inportb(SIO_DATA);

    outportb(SIO_INDEX, 0xAA);              /* SIO - Disable */

        return iData;
}
```

CN2 Pin	Description	Correspond to
3	DIO0	GPIO80
5	DIO1	GPIO81
7	DIO2	GPIO82
9	DIO3	GPIO83
11	DIO4	GPIO84
13	DIO5	GPIO85
15	DIO6	GPIO86
17	DIO7	GPIO87