Quick Installation Guide

Part No. 2007901A12 Printed in Taiwan June. 2005

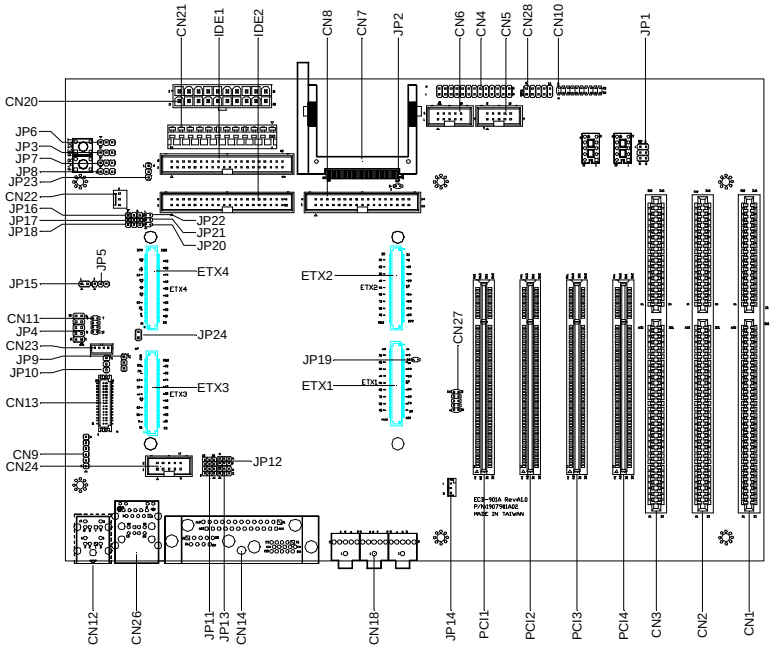
Safety Precautions

Always completely disconnect the power cord from your board whenever you are working on it. Do not make connections while the power is on, because a sudden rush of power can damage sensitive electronic components.

Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis

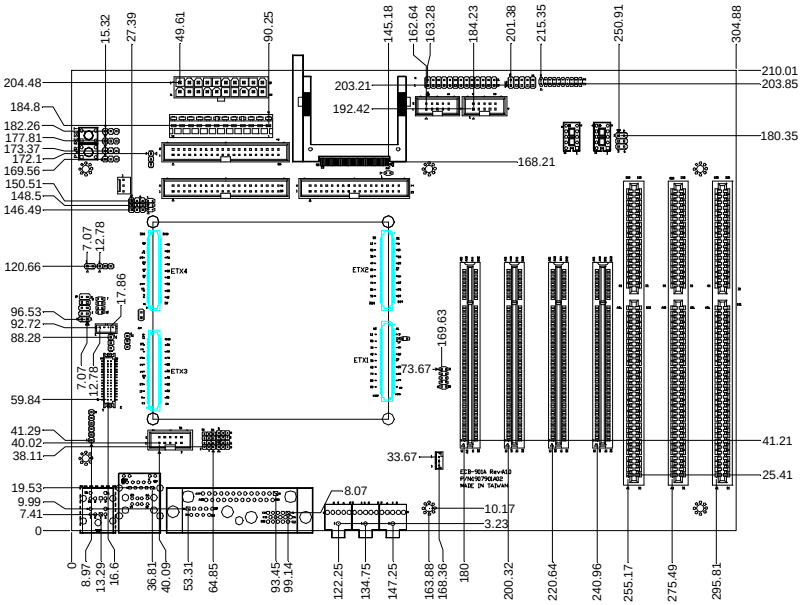
1. Location of Connectors and Jumpers

Component Side

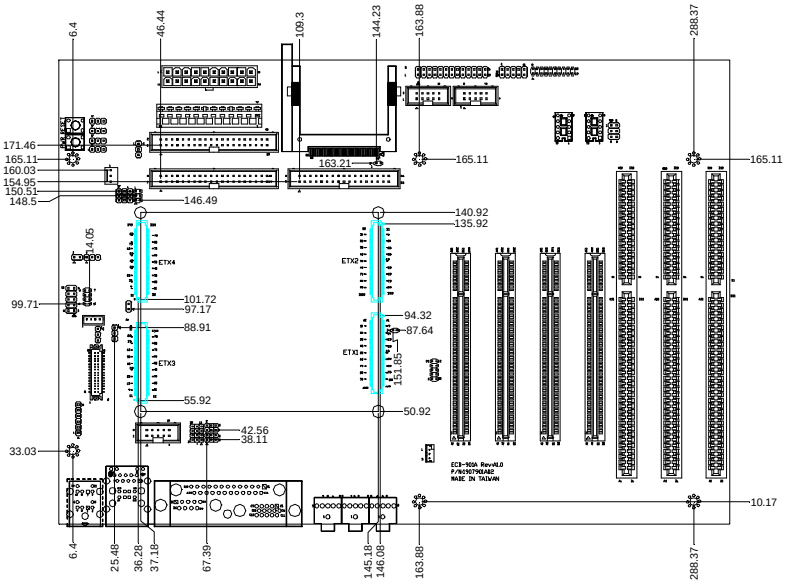


2. Mechanical Drawing

Component Side-1



Component Side-2



3. List of Jumpers

The board has a number of jumpers that allow you to configure your system to suit your application.

The table below shows the function of each of the board's jumpers:

Jumpers

Label	Function
JP1	DOC Address selection
JP2	Compact flash master-slave selection
JP3	ATA cable detection or SPDIAG#
JP5	CMOS Clear
JP6	AT and ATX type power supply selection
JP7	WDT Reset, IOCHCK# selection
JP8	External-internal speaker selection
JP9	LCD Power Selection
JP10	Backlight Power selection
JP11	COM2 RS-232/422/485 Select
JP12	COM2 RS-232/422/485 Select
JP13	COM2 Ring/+5V/+12V Select
JP16	ETX-4 Pin D90 Selection
JP17	ETX-4 Pin D19 Selection
JP18	ETX-4 Pin D35 Selection
JP19	ETX-1 Pin A21 Selection
JP20	ETX-4 Pin D9 Selection
JP21	ETX-4 Pin D26 Selection
JP22	ETX-4 Pin D41 Selection
JP23	Fan Power Selection

JP24	5VSB For ETX Module

4. List of Connectors

The board has a number of connectors that allow you to configure your system to suit your application. The table below shows the function of each board's connectors:

Connectors

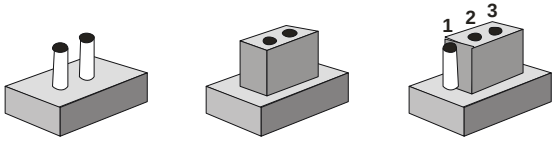
Label	Function
CN1	ISA connector
CN2	ISA Connector
CN3	ISA Connector
CN4 (LPT2)	PRINTER PORT Connector
CN5 (COM3)	RS-232 Serial Port Connector
CN6 (COM4)	RS-232 Serial Port Connector
CN7	Compact Flash connector
CN8	FLOPPY DRIVER Connector
CN9	SIR Connector
CN10	DIGITAL IO Connector
CN11	TV-OUT Connector
CN12	PS2 KB+MS Connector
CN13	LVDS connector
CN14 (COM1+LPT1+VGA)	RS232+Printer+VGA Connector
CN17	Audio LINE-IN Connector

CN18	Audio LINE-OUT connector
CN19	Audio Microphone-IN Connector
CN20	ATX Power Connector
CN21	AT Power Connector
CN22	FAN Connector
CN23	Backlight Power connector
CN24（COM2）	RS-232 Serial Port Connector
CN26	USB+RJ45 Connector
CN27	USB 3/4 Connector
IDE1	Primary IDE connector
IDE2	Secondary IDE connector
PCI1	PCI Connector
PCI2	PCI Connector
PCI3	PCI Connector
JP4	Front Panel
JP14	LAN Wake Up

5. Setting Jumpers

You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" a jumper you connect the pins with the clip.

To "open" a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



Open **Closed** **Closed 2-3**

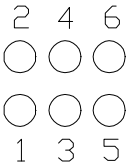
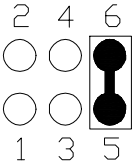
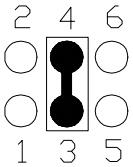
A pair of needle-nose pliers may be helpful when working with jumpers.

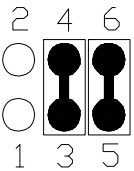
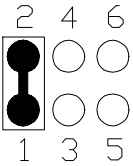
If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any change.

Generally, you simply need a standard cable to make most connections.

6. DOC Address Selection (JP1)

The DiskOnChip 2000 occupies an 8 K byte window in the upper memory address range of CC00 to DC00. You should ensure this does not conflict with any other device's memory address.

Address	cc00	D000	D400
			

Address	D800	DC00
		

These addresses might conflict with the ROM BIOS on some of the other peripheral boards. Please select appropriate memory address to avoid memory conflict.

7. CompactFlash™ Master-Slave Selection (JP2)

JP2	Function
1-2 ON	Master
1-2OFF	Slave (Default)

8. IDE2 ATA Cable Detection or PDIAG# Selection (JP3)

JP3	Function
1-2	ATA Cable Detection (Default)
2-3	PDIAG#

Remark: When IDE2 and CN7 have devices installed, select 2-3 for proper operation.

9. Clear CMOS Selection (JP5)

JP5	Function
1-2	Protect (Default)
2-3	Clear CMOS

10. AT and ATX type power supply selection (JP6)

JP6	Function
1-2	AT
2-3	ATX (Default)

11. WDT Reset IOCHCK# Selection (JP7)

JP7	Function
1-2	IOCHCK#
2-3	WDT Reset (Default)

12. External-Internal Speaker Selection (JP8)

JP8	Function
1-4	External Speaker
3-4	Internal Speaker (Default)

13. LCD Power Selection (JP9)

JP9	Function
1-2	5V
2-3	3.3V (Default)

14. LCD Backlight Power Selection (JP10)

JP10	Function
1-2	12V (Default)
2-3	+5V

15. COM 2 RS-232/422/485 Selection (JP11 & JP12)

JP11	JP12	Function
1-2, 4-5, 7-8, 10-11	1-2	RS-232 (Default)
2-3, 5-6, 8-9, 11-12	3-4	RS-422
2-3, 5-6, 8-9, 11-12	5-6	RS-485

16. COM 2 Ring/+5V/+12V Selection (JP13)

JP13	Function
1-2	+12V
3-4	+5V
5-6	Ring (Default)

17. ETX-4 Pin D90 Selection (JP16)

JP16	Function
1-2	LAN Wakeup (LWAKE)
2-3	Primary IDE ATA33/100 Detect (PD_80P) (Default)

18. ETX-4 Pin D19 Selection (JP17)

JP17	Function
1-2	OVCR# (USB) (Default)
2-3	DACK2#

19. ETX-4 Pin D35 Selection (JP18)

JP18	Function
1-2	Primary IDE ATA33/100 Detect
2-3	Secondary IDE ATA33/100 Detect (SD_80P) (Default)

20. ETX-1 Pin A21 Selection (JP19)

JP19	Function
1-2 ON	DRQ2
1-2 OFF	N.C. (Default)

21. ETX-4 Pin D9 Selection (JP20)

JP20	Function
1-2 ON	CPU FAN (Default)
1-2 OFF	N.C.

22. ETX-4 Pin D26 Selection (JP21)

JP21	Function
1-2 ON	CPU FAN
1-2 OFF	N.C. (Default)

23. ETX-4 Pin D41 Selection (JP22)

JP22	Function
1-2 ON	Secondary IDE ATA33/100 Detect
1-2 OFF	N.C. (Default)

24. Front Panel Connector (JP4)

JP4	Function		
1-2	Power Button		
3	HDD LED -	4	HDD LED +
5	Speaker -	6	Speaker +
7	Power LED -	8	Power LED +
9-10	Reset Button		

25. LAN Wake up Connector (JP14)

Pin	Signal
1	+5VSB
2	LWAKE
3	GND

26. Fan Power Selection (JP23)

JP23	Function
1-2	5V
2-3	12V
OFF	5V

27. 5VSB For ETX Module (JP24)

JP24	Function
ON	Standby 5V(5VSB) for ETX Module
OFF	No Standby 5V(5VSB) for ETX Module

28. RS-232 Serial Port Connector (CN5, CN6 & CN24)

Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	N.C.

29. CompactFlash™ Disk Connector (CN7)

Pin	Signal	Pin	Signal
1	GND	26	GND
2	SDD3	27	SDD11
3	SDD4	28	SDD12
4	SDD5	29	SDD13

5	SDD6	30	SDD14
6	SDD7	31	SDD15
7	SDCS#1	32	SDCS#3
8	GND	33	GND
9	GND	34	SDIOR#
10	GND	35	SDIOW#
11	GND	36	+5V
12	GND	37	IRQ15
13	+5V	38	+5V
14	GND	39	CSEL#
15	GND	40	N.C.
16	GND	41	SEC_IDERST#
17	GND	42	SIORDY
18	SDA2	43	N.C.
19	SDA1	44	+5V
20	SDA0	45	DASP#
21	SDD0	46	PDIAG#
22	SDD1	47	SDD8
23	SDD2	48	SDD9
24	N.C.	49	SDD10
25	GND	50	GND

30. Floppy Drive Connector (CN8)

Pin	Signal	Pin	Signal
1	GND	2	#DENSITYSEL
3	GND	4	N.C.
5	GND	6	#DS1

7	GND	8	#INDEX
9	GND	10	#MOTORA
11	GND	12	#DRIVE SELECT B
13	GND	14	#DRIVE SELECT A
15	GND	16	#MOTOR B
17	GND	18	#DIR
19	GND	20	#STEP
21	GND	22	#WRITE DATA
23	GND	24	#WRITE GATE
25	GND	26	#TRACK0
27	GND	28	#WRITE PROTECT
29	GND	30	#READ DATA
31	GND	32	#HEADSEL
33	GND	34	#DISK CHANGE

31. IR Connector (CN9)

Pin	Signal
1	+5V
2	N.C.
3	IRRX
4	GND
5	IRTX
6	N.C.

32. Digital IO Connector (CN10)

Pin	Signal	Pin	Signal
1	OUT0	2	OUT1
3	OUT2	4	OUT3
5	OUT4	6	OUT5
7	OUT6	8	OUT7
9	GND	10	GND
11	IN0	12	IN1
13	IN2	14	IN3
15	IN4	16	IN5
17	IN6	18	IN7
19	+5V	20	+12V

33. TV Out Connector (CN11)

Pin	Signal	Pin	Signal
1	Y	2	CVBS
3	GND	4	GND
5	C	6	NC
7	GND	8	CSYNC

34. Keyboard & Mouse Connector (CN12)

Pin	Signal	Pin	Signal
1	KB_DATA	7	MS_DATA
2	MS_DATA	8	N.C.
3	GND	9	GND

4	+5VSB	10	+5VSB
5	KB_CLK	11	MS_CLK
6	MS_CLK	12	N.C.

35. AAEON LVDS Connector (CN13)

Pin	Signal	Pin	Signal
1	Backlight Enable	2	Backlight Control
3	PPVCC	4	GND
5	#LCLK	6	LCLK
7	PPVCC	8	GND
9	#LDATA0	10	LDATA0
11	#LDATA1	12	LDATA1
13	#LDATA2	14	LDATA2
15	#LDATA3	16	LDATA3
17	SMBDATA	18	SMBCLK
19	#UDATA0	20	UDATA0
21	#UDATA1	22	UDATA1
23	#UDATA2	24	UDATA2
25	#UDATA3	26	UDATA3
27	PPVCC	28	GND
29	#UCLK	30	UCLK

36. VGA Display + Printer + COM Connector (CN14)

Pin	Signal	Pin	Signal
A1	#STROBE	A14	#AFD
A2	Printer DATA0	A15	#ERROR
A3	Printer DATA1	A16	#INIT
A4	Printer DATA2	A17	#SLIN
A5	Printer DATA3	A18	GND
A6	Printer DATA4	A19	GND
A7	Printer DATA5	A20	GND
A8	Printer DATA6	A21	GND
A9	Printer DATA7	A22	GND
A10	#ACK	A23	GND
A11	BUSY	A24	GND
A12	PE	A25	GND
A13	SELECT		
B1	DCD	B2	RXD
B3	TXD	B4	DTR
B5	GND	B6	DSR
B7	RTS	B8	CTS
B9	RI		
C1	RED	C2	GREEN
C3	BLUE	C4	NC
C5	GND	C6	GND
C7	GND	C8	GND

C9	+5V	C10	GND
C11	NC	C12	DDCDATA
C13	HSYNC	C14	VSYNC
C15	DDCCLK		

37. ATX Power Connector (CN20)

Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
2	+3.3V	4	-12V
3	GND	6	GND
4	+5V	8	PS-ON
5	GND	10	GND
6	+5V	12	GND
7	GND	14	GND
8	PW-OK	16	-5V
9	+5VSB	18	+5V
10	+12V	20	+5V

38. AT Power Connector (CN21)

Pin	Signal
1	N.C. (POWER GOOD)
2	+5V
3	+12V

4	-12V
5	GND
6	GND
7	GND
8	GND
9	-5V
10	+5V
11	+5V
12	+5V

39. Fan Connector (CN22)

Pin	Signal
1	GND
2	+12V
3	Speed Sense

40. Backlight Power Connector (CN23)

Pin	Signal
1	Backlight Power
2 & 3	GND
4	Backlight on

41. LAN + USB Connector (CN26)

Pin	Signal	Pin	Signal
1	TCT	2	TD+
3	TD-	4	RD+
5	RD-	6	NA
7	NA	8	NA
9	NA	10	RCT
11	LED1 (Y-)	12	LED1 (Y+)
13	LED2 (G-, O+)	14	LED2 (G +, O-)
15	N.C.	16	N.C.
17	N.C.	18	N.C.
19	+5V	20	USB DATA0-
21	USB DATA1+	22	GND
23	+5V	24	USB DATA1-
25	USB DATA1+	26	GND

42. IDE1 & IDE2: IDE Hard Drive Connector

Pin	Signal	Pin	Signal
1	IDE RESET	2	GND
3	DATA7	4	DATA8
5	DATA6	6	DATA9
7	DATA5	8	DATA10
9	DATA4	10	DATA11

11	DATA3	12	DATA12
13	DATA2	14	DATA13
15	DATA1	16	DATA14
17	DATA0	18	DATA15
19	GND	20	NC
21	REQ	22	GND
23	IO WRITE	24	GND
25	IO READ	26	GND
27	IO READY	28	GND
29	DACK	30	GND
31	IRQ	32	NC
33	ADDR1	34	UDMA DETECT
35	ADDR0	36	ADDR2
37	CS#1	38	CS#3
39	LED	40	GND

43. USB Connector (CN27)

Pin	Signal	Pin	Signal
1	+5V	2	GND
3	USBD2-	4	GND
5	USBD2+	6	USBD3+
7	GND	8	USBD3-
9	GND	10	+5V

44. Second Printer Connector (CN4)

Pin	Signal	Pin	Signal
1	#STROBE	2	#AFD
3	Printer DATA0	4	#ERROR
5	Printer DATA1	6	#INIT
7	Printer DATA2	8	#SLIN
9	Printer DATA3	10	GND
11	Printer DATA4	12	GND
13	Printer DATA5	14	GND
15	Printer DATA6	16	GND
17	Printer DATA7	18	GND
19	#ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SELECT	26	N.C.

45. ETX Connector – 1

PCI BUS

AD0 – AD31

PCI bus multiplexed address /data signals.

CBE0# - C/BE3# (C/BE#0-C/BE#3)

PCI bus multiplexed command /byte enable signals.

FRAME#

When this signals is asserted, a PCI cycle is started.

DEVSEL#

Device select signal. When the target device has decoded the address as its own cycle, it will assert DEVSEL#

TRDY#

Target ready signal. When a device is ready to complete data transaction, it asserts this signal.

IRDY#

Initial ready signals. A PCI initiator assert this signal when it is ready to complete data transaction.

STOP#

The signal is asserted by target to request initiator to stop the current PCI transaction.

PCICLK1 – PCICLK4

PCI clock signals for each PCI slots.

REQ0# - REQ3# (PREQ#0-PREQ#3)

PCI bus request signals for each PCI slots. A PCI device assert this signal to gain the control of PCI bus from host bridge.

GNT0# - GNT3# (PGNT#0-PGNT#3)

PCI bus grant signals for each PCI slots. Host Bridge asserts this signal to a PCI device and allows it to be a PCI master.

INTA#, INTB#,INTC#,INTD# (INT#A, INT#B,INT#C,INT#D)

PCI interrupt request signals. Rout all four signals to each PCI slots.

Please refer to below table for detailed.

PCI SLOT	1	2	3	4
IDSEL	AD19	AD20	AD21	AD31
INT (PinA6,B6,A7,B7)	A, B, C, D	B, C, D, A	C, D, A, B	D, A, B, C
REQ/GNT	REQ0# GNT0#	REQ1# GNT1#	REQ2# GNT2#	REQ3# GNT3#
PCI CLOCK	PCICLK0	PCICLK1	PCICLK2	PCICLK3

PAR

This signal is used for the even parity check on both AD & C/BE lines.

PERR#

This signal is used for reporting data parity errors during all PCI transactions. Except in a Special cycle.

SERR#

This signal is used for reporting address parity errors during all PCI transactions. Except in a Special cycle.

LOCK# (PLOCK#)

This signal indicates a lock Cycle for an atomic operation that may Require multiple transactions to complete.

PCIRST#

This signal is used to reset PCI device.

PME#

PCI device assert this signal for power management event.

USB

USB0, USB0# (USBP0, USBP#0)

USB port 0 signals. USB0 is positive signal, USB0# is negative signal. They are differential pair. For proper operation, rout the two signals parallel and equal length. .

USB1, USB1# (USBP1, USBP#1)

USB port 1 signals. USB1 is positive signal, USB1# is negative signal. They are differential pair. For proper operation, rout the two signals parallel and equal length.

USB2, USB2# (USBP2, USBP#2)

USB port 2 signals. USB2 is positive signal, USB2# is negative signal. They are differential pair. For proper operation, rout the two signals parallel and equal length.

USB3, USB3# (USBP3, USBP#3)

USB port 3 signals. USB3 is positive signal, USB3# is negative signal. They are differential pair. For proper operation, rout the two signals parallel and equal length.

Audio

VCCAUD

Audio power 5V output. This power signal is fed by ETX CPU module.

GNDAUD

Audio Ground.

LOUTR

Right Line-out signal.

LOUTL

Left Line-out signal.

MIC (MIC-IN)

Microphone input signal.

LINR

Right Line-in signal.

LINL

Left Line-in signal.

Miscellaneous

3.3V (VCC3)

3V power input. This power signal is fed by ETX carrier board. 3.3V power is generated by linear regulator on carrier board or provided by ATX power supply.

SERIRQ/DRQ2

SERIRQ or DRQ2 signal. SERIRQ is serial interrupt request signal. DRQ2 is DMA request 2 signal. On this carrier board,

SERIRQ is not implemented. SERIRQ is default on ETX module. JP19 1-2 is off to set it as no connection as default on carrier board.

VCC

5V power input. This power signal is fed by ETX carrier board.

RESVD

Reserved.

N.C

No connection.

Pin	Signal	Pin	Signal	Pin	Signa	Pin	Signal
A1	GND	A2	GND	A51	VCC	A52	VCC
A3	PCICLK3	A4	PCICLK4	A53	PAR	A54	SERR#
A5	GND	A6	GND	A55	PERR#	A56	N.C
A7	PCICLK1	A8	PCICLK2	A57	PME#	A58	USB2#
A9	REQ3#	A10	GNT3#	A59	LOCK#	A60	DEVSEL#
A11	GNT2#	A12	3.3V	A61	TRDY#	A62	USB3#
A13	REQ2#	A14	GNT1#	A63	IRDY#	A64	STOP#
A15	REQ1#	A16	3.3V	A65	FRAME#	A66	USB2
A17	GNT0#	A18	N.C	A67	GND	A68	GND
A19	VCC	A20	VCC	A69	AD16	A70	C/BE2#
A21	NC / DRQ2	A22	REQ0#	A71	AD17	A72	USB3
A23	AD0	A24	3.3V	A73	AD19	A74	AD18
A25	AD1	A26	AD2	A75	AD20	A76	USB0#
A27	AD4	A28	AD3	A77	AD22	A78	AD21
A29	AD6	A30	AD5	A79	AD23	A80	USB1#

A31	C/BE0#	A32	AD7	A81	AD24	A82	CBE3#
A33	AD8	A34	AD9	A83	VCC	A84	VCC
A35	GND	A36	GND	A85	AD25	A86	AD26
A37	AD10	A38	LINL	A87	AD28	A88	USB0
A39	AD11	A40	MIC	A89	AD27	A90	AD29
A41	AD12	A42	LINR	A91	AD30	A92	USB1
A43	AD13	A44	VCCAUD	A93	PCIRST#	A94	AD31
A45	AD14	A46	LOUTL	A95	INTC#	A96	INTD#
A47	AD15	A48	GNDAUD	A97	INTA#	A98	INTB#
A49	C/BE1#	A50	LOUTR	A99	GND	A100	GND

46. ETX Connector – 2

ISA BUS

SA0 – SA19

ISA bus address signals allow access of up to 1MB of memory on ISA bus.

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LA17-LA23

LA17-LA23 address signals allow access of up to 16MB of memory on ISA bus.

SD0 – SD15

ISA bus data signals.

AEN

Address enable signal. It is high during DMA and Master cycle.

IOCHCK#

I/O channel check signal. When I/O device parity error occurs, this signal is asserted.

IOW#

To write data to I/O port, this signal is asserted.

IOR#

To read data from I/O port, this signal is asserted.

SMEMW#

To write data to I/O memory space below 1 M address, this signal is asserted.

SMEMR#

To read data from I/O memory space below 1 M address, this signal is asserted.

MEMW#

To write data to I/O memory space, this signal is asserted.

MEMR#

To read data from I/O memory space, this signal is asserted.

BALE

ISA Bus buffer latch enable.

IOCHRDY

This signal is asserted low by I/O device to extend the ISA bus cycle.

NOWS# (ZWS#)

No wait state signal. It is asserted by I/O device to shorten

the ISA bus cycle.

RSTDRV (RES-DRV)

This signal is asserted during POWER-ON period and reset period. It is used to reset ISA device.

REFSH# (REFRESH#)

This signal is used for I/O device to recharge on-board DRAM.

SYSCLK

ISA Bus clock signal. It provide I/O device internal state machine clock source.

OSC (SIOCLK)

14.31818MHz clock source.

IRQ3 – IRQ15 (Not include IRQ8, IRQ12, IRQ13)

Interrupt request signals.

MASTER#

This signal indicates a 16-bit ISA master is taking control of ISA bus.

DREQ0 – DREQ7 (Not include DREQ4)

DMA request signals. DRQ0 - DRQ3 are for 8 bits data transfer. DRQ5 - DRQ7 are for 16 bits data transfer.

DACK0# - DACK7# (Not include DACK4#) (DACK#0-DACK#7)

DMA acknowledge signals. DACK0# - DACK3# are for 8 bits data transfer. DACK5# - DACK7# are for 16 bits data transfer.

TC

This signal is asserted to indicated the end of a DMA transfer,

SBHE#

This signal indicates that the high byte on the ISA data bus is valid.

M16# (MEMCS16#)

MEMCS16# signal. This signal indicates that the bus size of current ISA memory slave is 16 bits.

IO16# (IOCS16#)

IOCS16# signal. This signal indicates that the bus size of current ISA I/O slave is 16 bits.

Pin	Signal	Pin	Signal	Pin	Signa	Pin	Signal
B1	GND	B2	GND	B51	VCC	B52	VCC
B3	SD14	B4	SD15	B53	SA6	B54	IRQ5
B5	SD13	B6	MASTER#	B55	SA7	B56	IRQ6
B7	SD12	B8	DREQ7	B57	SA8	B58	IRQ7
B9	SD11	B10	DACK7#	B59	SA9	B60	SYSCLK
B11	SD10	B12	DREQ6	B61	SA10	B62	REFSH#
B13	SD9	B14	DACK6#	B63	SA11	B64	DREQ1
B15	SD8	B16	DREQ5	B65	SA12	B66	DACK1#
B17	MEMW#	B18	DACK5#	B67	GND	B68	GND
B19	MEMR#	B20	DREQ0	B69	SA13	B70	DREQ3
B21	LA17	B22	DACK0#	B71	SA14	B72	DACK3#
B23	LA18	B24	IRQ14	B73	SA15	B74	IOR#
B25	LA19	B26	IRQ15	B75	SA16	B76	IOW#

B27	LA20	B28	N.C	B77	SA18	B78	SA17
B29	LA21	B30	IRQ11	B79	SA19	B80	SMEMR#
B31	LA22	B32	IRQ10	B81	IOCHRDY	B82	AEN
B33	LA23	B34	IO16#	B83	VCC	B84	VCC
B35	GND	B36	GND	B85	SD0	B86	SMEMW#
B37	SBHE#	B38	M16#	B87	SD2	B88	SD1
B39	SA0	B40	OSC	B89	SD3	B90	NOWS#
B41	SA1	B42	BALE	B91	DREQ2	B92	SD4
B43	SA2	B44	TC	B93	SD5	B94	IRQ9
B45	SA3	B46	DACK2#	B95	SD6	B96	SD7
B47	SA4	B48	IRQ3	B97	IOCHK#	B98	RSTDRV
B49	SA5	B50	IRQ4	B99	GND	B100	GND

47. ETX Connector – 3

Parallel port

PD0 – PD7 (PRD0 – PRD7)

Parallel port data signals

SLCT

An active high input on this pin indicate the printer is selected.

SLIN# (SLCTIN#)

Output of detection. of printer selected.

INIT# (PINIT#)

Output for printer initialization.

BUSY

An active high input on this pin indicate that the printer is not ready to receive data.

ACK#

An active low input on this pin indicate that the printer has received data and is ready to receive more.

ERR# (ERROR#)

An active low input on this pin indicate that the printer has encounter an error.

AFD# (AUTOFD#)

An active low output from this signal cause the printer to auto feed a line after a line is printed.

STB# (STROBE#)

An active low output of this signal is used to latch the parallel data into the printer.

PE

An active high input on this pin indicate that the printer has detected the end of paper.

PS/2 Keyboard and Mouse

KBDAT

PS/2 keyboard data signal.

KBCLK

PS/2 keyboard clock signal.

MSDAT

PS/2 mouse data signal.

MSCLK

PS/2 mouse clock signal.

VGA

R (RED)

RED analog output.

G (GREEN)

Green analog output.

B (BLUE)

Blue analog output.

HSY (HSYNC)

CRT horizontal synchronous signal.

VSY (VSYNC)

CRT vertical synchronous signal.

DDCK (SCL)

This clock signal is used for monitor type detection.

DDDA (SDA)

This data signal is used for monitor type detection.

Serial port

DCD1# (SDCD1X)

COM1 Data Carrier Detect signal

RXD1# (SRXD1)

COM1 data serial input signal.

TXD1# (STXD1)

COM1 data serial output signal.

RTS1# (SRTS1X)

COM1 Request To Send signal.

CTS1# (SCTS1X)

COM1 Clear To Send signal.

DSR1# (SDSR1X)

COM1 Data Set Ready signal.

DTR1# (SDTR1X)

COM1 Data Terminal Ready signal.

RI1# (SRI1X)

COM1 Ring signal.

DCD2# (SDCD2X)

COM2 Data Carrier Detect signal.

RXD2# (SRXD2)

COM2 Data serial in signal.

TXD2# (STXD2)

COM2 data serial output signal.

RTS2# (SRTS2X)

COM2 Request To Send signal.

CTS2# (SCTS2X)

COM2 Clear To Send signal.

DSR2# (SDSR2X)

COM2 Data Set Ready signal.

DTR2# (SDTR2X)

COM2 Data Terminal Ready signal.

RI2# (SRI2X)

COM2 Ring signal.

LVDS

TX1OUT0,TX1OUT0# (TX1QUT0, TX1QUT#0)

LVDS channel 1 differential pair no. 0

TX1OUT1,TX1OUT1# (TX1QUT1,TX1QUT#1)

LVDS channel 1differential pair no. 1

TX1OUT2,TX1OUT2# (TX1QUT2,TX1QUT#2)

LVDS channel 1differential pair no. 2

TX1OUT3,TX1OUT3# (TX1QUT3,TX1QUT#3)

LVDS channel 1differential pair no. 3

TX1CLK,TX1CLK#

LVDS channel 1 clock differential pair

TX2OUT0,TX2OUT0# (TX2OUT0,TX2OUT#0)

LVDS channel 2 differential pair no. 0

TX2OUT1,TX2OUT1# (TX2OUT1,TX2OUT#1)

LVDS channel 2 differential pair no. 1

TX2OUT2,TX2OUT2# (TX2OUT2, TX2OUT#2)

LVDS channel 2 differential pair no. 2

TX2OUT3,TX2OUT3# (TX2OUT3,TX2OUT#3)

LVDS channel 2 differential pair no. 3

TX2CLK,TX2CLK#

LVDS channel 2 clock differential pair

PLCLK (DDCPCLK)

This clock signal is used for panel type detection. To use this signal, check the support of ETX module.

PLDAT (DDCPDATA)

This data signal is used for panel type detection. To use this signal, check the support of ETX module.

DIGON (ENVDD)

This active high output signal is used to enable LCD power.

BLON (BLON# For this carrier board, it is active high signal)

This active high output signal is used to enable inverter power.

BLK_CTL (BLK_CTRL)

Backlight contrast control output(Option)

DETECT#

Panel detection input. When low it indicates a LCD panel is present. When high, a LCD panel is absent. This signal is not implement on this carrier board. It is left as no connection.

TV OUT

Y (Y_R)

SVIDEO Luminance output.

C (C_C)

SVIDEO Chrominance output.

COMP (COMP/B)

Composite video output.

SYNC (CSYNC)

Composite Sync for RGB Video. When use this signal, Y is R, C is G and COMP is B by setting ETX TV chip.

IR

IRTX

Infrared transmit signal.

IRRX

Infrared receive signal.

other

GPIO0

General purpose I/O 0. This signal is connected to AT_ATX signal in schematics and on this carrier board intended for AT and ATX power detection, but the function is not implemented.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
C1	GND	C2	GND	C51	RESVD	C52	N.C
C3	R	C4	B	C53	VCC	C54	GND
C5	HSY	C6	G	C55	STB#	C56	AFD#
C7	VSY	C8	DDCK	C57	RESVD	C58	PD7
C9	DETECT#	C10	DDDA	C59	IRRX	C60	ERR#
C11	TX2CLK#	C12	TX2OUT3#	C61	IRTX	C62	PD6
C13	TX2CLK	C14	TX2OUT3	C63	RXD2	C64	INIT#
C15	GND	C16	GND	C65	GND	C66	GND
C17	TX2OUT1	C18	TX2OUT2	C67	RTS2#	C68	PD5
C19	TX2OUT1#	C20	TX2OUT2#	C69	DTR2#	C70	SLIN#
C21	GND	C22	GND	C71	DCD2#	C72	PD4

C23	TX1OUT3#	C24	TX2OUT0	C73	DSR2#	C74	PD3
C25	TX1OUT3	C26	TX2OUT0#	C75	CTS2#	C76	PD2
C27	GND	C28	GND	C77	TXD2#	C78	PD1
C29	TX1OUT2#	C30	TX1CLK	C79	RI2#	C80	PD0
C31	TX1OUT2	C32	TX1CLK#	C81	VCC	C82	VCC
C33	GND	C34	GND	C83	RXD1	C84	ACK#
C35	TX1OUT0	C36	TX1OUT1	C85	RTS1#	C86	BUSY
C37	TX1OUT0#	C38	TX1OUT1#	C87	DTR1#	C88	PE
C39	VCC	C40	VCC	C89	DCD1#	C90	SLCT
C41	PLDAT	P42	GPIO0	C91	DSR1#	C92	MSCLK
C43	PLCLK	C44	BLON	C93	CTS1#	C94	MSDAT
C45	BLK_CTL	C46	DIGON	C95	TXD1	C96	KBCLK
C47	COMP	C48	Y	C97	RI1#	C98	KBDAT
C49	SYNC	C50	C	C99	GND	C100	GND

48. ETX Connector – 4 (Default)

IDE interface

PIDE_D0 – PIDE_D15 (PDD0 – PDD15)

Primary IDE channel data bus signals..

PIDE_IOW# (PDDIOW#)

Primary IDE channel IOW# signal.

PIDE_IOR# (PDDIOR#)

Primary IDE channel IOR# signal.

PIDE_RDY (PDDRDY)

Primary IDE channel RDY# signal.

PIDE_A0 – PIDEA2 (PDDA0, PDDA2)

Primary IDE channel address signals.

PIDE_CS1# (PDDCS#1)

Primary IDE channel chip select 1 signal.

PIDE_CS3# (PDDCS#3)

Primary IDE channel chip select 3 signal.

PIDE_INT# (IRQ14)

Primary IDE channel interrupt request signal.

PIDE_AK# (PDDACK#)

Primary IDE channel acknowledge signal.

PIDE_DRQ (PDDREQ)

Primary IDE DMA request signal.

SIDE_D[0..15] (SDD0-SDD15)

Secondary IDE channel data bus signals.

SIDE_IOW# (SDDIOR#)

Secondary IDE channel IOW# signal.

SIDE_IOR# (SDDIOR#)

Secondary IDE channel IOR# signal.

SIDE_RDY (SDDRDY)

Secondary IDE channel RDY# signal.

SIDE_A[0..2] (SDDA0-SDDA2)

Secondary IDE channel address signals.

SIDE_CS1# (SDDCS#1)

Secondary IDE channel chip select 1 signal.

SIDE_CS3# (SDDCS#3)

Secondary IDE channel chip select 3 signal.

SIDE_INT (IRQ15)

Secondary IDE channel interrupt request signal.

SIDE_AK# (SDDACK#)

Secondary IDE channel acknowledge signal.

SIDE_DRQ (SDDREQ)

Secondary IDE DMA request signal.

SD80/PD80

Secondary or primary IDE channel 80-pin cable detection.

Default is SD80. (Set JP18 2-3 ON)

PD80/LWAKE

Primary IDE channel 80 pin cable detection or LAN wake up output signal.

Default is PD80. (Set JP16 2-3 ON)

BATLOW#/SD80

Battery low input or Secondary IDE channel 80 pin cable detection. When BATLOW# signal is low indicates an external battery is in low battery capacity condition. This battery low signal is not implemented on this carrier board.

Default is No connection (Set JP22 1-2 OFF).

HDRST# (IDERST#)

IDE reset signal.

other

5V_SB (VSB5)

5V Standby voltage input. This power signal is fed by ETX

carrier board. This power signal is from JP6. Set JP6 1-2 for AT type power supply. Set JP6 2-3 for ATX type power supply.

VBAT

Power input for RTC backup. This power signal is fed by ETX carrier board

RSTIN#

Reset input. Reset button and Watchdog timer can generate this signal.

PWRBTN# (PW_BN)

Power button input.

PS_ON (PSON)

A low on this signal enable ATX power supply output. A high on this signal disable ATX power supply output.

EXTSMI#

External SMI signal input. Assert this signal for power management event.

OVCR#/DACK2#

USB over current input. Tie all USB over current signal together by open-drain circuit on this signal.

Default is OVCR# (Set JP17 1-2 ON)

Note: There are two USB over current detection methods. Refer to schematics page 13. Use U20 or U21. For U20, the support chip is VIA82C686B.

SPEAKER (SPKR)

Speaker signal output.

RING#

This input signal is asserted to wake up the system from low power state. The input source of this signal are RI signal of COM port and LWAKE signal of LAN.

GPIO1 (GPIOD)

General purpose I/O 1. Currently is defined as output.

CPUFAN/NC

CPU fan frequency detection or NC.

Default is CPUFAN. (Set JP20 1-2 ON)

ROMCS#

BIOS ROM chip select output. This pin D11 is connected to IRQ1 in schematics, but is not support by ETX module.

SMALRT#/CPUFAN

SM bus alert signal or fan frequency input (CPUFAN). This signal is not implemented on this carrier board.

Default is left as no connection (Set JP21 1-2 OFF).

I2CLK (SMBCLK)

I2C clock signal.

I2DAT (SMBDATA)

I2C data signal..

SMCLK (SMBCLK)

SM bus clock signal.

SMDAT (SMBDATA)

SM bus data signal.

NC/WDRST#

NC pin or Watch dog reset output signal. This pin is default as no connection on ETX module.

EX_PRG

This signal is reserved. This pin is connected to IRQ8X in schematics and carrier board, but is not supported by ETX module.

LAN

TXD, TXD# (TXD+, TXD-)

Ethernet LAN transfer data differential signal.

RXD,RXD# (RXIN+, RXIN-)

Ethernet LAN received data differential signal.

LILED

Link LED signal output.

ACTLED (TXRX_LED)

Active LED signal output.

SPEEDLED (LINK100_LED)

Speed LED. When high, indicate 10MHZ. When low, indicate 100MHz.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
D1	GND	D2	GND	D51	SIDE_IOW#	D52	PIDE_IOR#
D3	5V_SB	D4	RSTIN#	D53	SIDE_DRQ	D54	PIDE_IOW#
D5	PS_ON	D6	SPEAKER	D55	SIDE_D15	D56	PIDE_DRQ

D7	PWRBTN#	D8	VBAT	D57	SODE_D0	D58	PIDE_D15
D9	CPUFAN/NC	D10	LILED	D59	SIDE_D14	D60	PIDE_D0
D11	NC/WDRST#	D12	ACTLED	D61	SIDE_D1	D62	PIDE_D14
D13	ROMCS#	D14	SPEEDLED	D63	SIDE_D13	D64	PIDE_D1
D15	EX_PRG	D16	I2CLK	D65	GND	D66	GND
D17	VCC	D18	VCC	D67	SIDE_D2	D68	PIDE_D13
D19	OVCR#DACK2#	D20	GPIO1	D69	SIDE_D12	D70	PIDE_D2
D21	EXTSMI#	D22	I2DAT	D71	SIDE_D3	D72	PIDE_D12
D23	SMCLK	D24	SMDAT	D73	SIDE_D11	D74	PIDE_D3
D25	SIDE_CS3#	D26	SMALRT#/ CPUFAN	D75	SIDE_D4	D76	PIDE_D11
D27	SIDE_CS1#	D28	RESVD	D77	SIDE_D10	D78	PIDE_D4
D29	SIDE_A2	D30	PIDE_CS3#	D79	SIDE_D5	D80	PIDE_D10
D31	SIDE_A0	D32	PIDE_CS1#	D81	VCC	D82	VCC
D33	GND	D34	GND	D83	SIDE_D9	D84	PIDE_D5
D35	SD80/PD8	D36	PIDE_A2	D85	SIDE_D6	D86	PIDE_D9
D37	SIDE_A1	D38	PIDE_A0	D87	SIDE_D8	D88	PIDE_D6
D39	SIDE_INT	D40	PIDE_A1	D89	RING#	D90	PD80/LWAKE
D41	BATLOW#/SD80	D42	RESVD	D91	RXD#	D92	PIDE_D8
D43	SIDE_AK#	D44	PIDE_INT	D93	RXD	D94	SIDE_D7
D45	SIDE_RDY	D46	PIDE_AK#	D95	TXD#	D96	PIDE_D7
D47	SIDE_IOR#	D48	PIDE_RDY	D97	TXD	D98	HDRST#
D49	VCC	D50	VCC	D99	GND	D100	GND