

**COM-U15**

Intel® Atom™ Z530/Z510 Processor

24-bit Single Channel LVDS

DDR2 400/533 SODIMM Memory

High Definition Audio

1 PATA or 1 SATA II, 8 USB2.0

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## Packing List

Before you begin installing your card, please make sure that the following materials have been shipped:

- 1 COM-U15 CPU module
- 1 CD-ROM for manual (in PDF format) and drivers
- 4 M2.5 screws

If any of these items should be missing or damaged, please contact your distributor or sales representative immediately.

## Application Notes

### 1. Wake-On-LAN and PXE function

For saving the battery power, the standby power in the ECB-951D (COM Express carrier board) has been removed. Therefore, the COM-U15 cannot support Wake-On-LAN and PXE function when the ECB-951D has been using.

If you need the function of Wake-On-LAN or PXE, AAEON can provide the custom BIOS to you.

### 2. USB Client Port

The COM-U15 supports 8 USB ports. Port 7 can be the host or client port. It can be chosen via BIOS.

### 3. Legacy and legacy-free BIOS

The COM-U15 equips with legacy-free BIOS in default. If you test the functions on ECB-951D accompanied with the COM-U15, please use the legacy BIOS instead of legacy-free BIOS. You can find the legacy BIOS in the utility CD and get the latest one on AAEON website.

### 4. Display Support

If you want to get the display(s) not only from LVDS LCD, but also from DVI monitor for debugging, please purchase the ECB-951D. It is a COM Express carrier board and equips with SDVO to DVI daughter board to provide the DVI connector.

### 5. Touch Screen Controller with USB Interface

If you implement a touch screen controller with USB interface in the carrier board and use the Operating System of Windows CE, please use USB#0, 1 and 3 of COM-U15. There is a driver support issue of Windows CE.

# Contents

## Chapter 1 General Information

1.1 Introduction.....	1-2
1.2 Features .....	1-3
1.3 Specifications .....	1-4

## Chapter 2 Quick Installation Guide

2.1 Safety Precautions .....	2-2
2.2 Location of Connectors/Jumpers & Mechanical Drawings .....	2-3
2.3 List of Jumpers/ Connectors/ Switches .....	2-5
2.4 CPLD Writing Programming Connector (JP1) .....	2-5
2.5 SSD Writing Protection and SATA Bridge Master/Slave Setting and SSD Master/ Slave Setting (JP2).....	2-5
2.6 AT/ATX Selection (S1) .....	2-6
2.7 RTC Battery Connector (BAT1) .....	2-6
2.8 SODIMM (CN1) .....	2-6
2.9 COM Express Row A/B Connector (CN3).....	2-7
2.10 COM Express Row C/D Connector (CN4) .....	2-12
2.11 SCI & SMI Connector (CN6) .....	2-12

## Chapter 3 Award BIOS Setup

3.1 System Test and Initialization. ....	3-2
3.2 Award BIOS Setup .....	3-3

**Chapter 4 Driver Installation**

4.1 Installation .....	4-3
------------------------	-----

**Appendix A Programming The Watchdog Timer**

A.1 Programming .....	A-2
-----------------------	-----

**Appendix B I/O Information**

B.1 I/O Address Map .....	B-2
B.2 Memory Address Map .....	B-3
B.3 IRQ Mapping Chart .....	B-4
B.4 DMA Channel Assignments .....	B-4

Chapter

1

**General  
Information**



## 1.1 Introduction

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To accommodate fast growing marketing segments, AAEON has developed a brand new COM Express CPU module. The COM-U15, and its accompanying carrier board-ECB-951D, adopts Intel® Atom Z530/Z510 processor and Intel® System Controller Hub US15W chipset, offering high speed PCI-Express bus interface and serial ATA for your high performance applications requiring high-speed and greater stability. The COM Express CPU module offers flexibility and time-to-market advantages over a fully customized platform.

AAEON's COM-U15 supports up to 24-bit single channel LVDS interface and supports one 200-pin DDR2 400/533 SODIMM memory module up to 2GB. A high definition audio interface is available to connect to an audio codec on the carrier board. Moreover, one onboard PATA SSD (Master device) and one PATA/ one SATAII interfaces are featured giving the user flexibility in storage choices.

To satisfy the requirements of leading-edge applications in gaming, entertainment, industrial automation, medical, and POS, etc, COM Express carrier boards can be designed with features and technologies specifically targeting the needs of the different market segments. AAEON can design your COM Express carrier board to meet your specific project requirements.

## 1.2 Features

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- Onboard Intel® Atom™ Z530/Z510 Processor
- Intel® System Controller Hub US15W
- DDR2 400/533 Memory, Max. 2GB
- Gigabit Ethernet
- Up to 24-bit Single Channel LVDS LCD, SDVO
- High Definition Audio Interface
- PATA SSD (Up to 4GB) x 1, PATA x 1 or SATA II x 1
- USB2.0 x 8
- PCI-Express[x1] x 1
- Wide DC Input Range, +8.5V to +19V
- COM Express Pin-out Type II
- Compact Module Size, 95mm x 95mm

### 1.3 Specifications

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#### System

- Processor Intel® Atom™ Z530/Z510 Processor  
Z530: 1.6GHz/ FSB 533MHz  
Z510: 1.1GHz/ FSB 400MHz
- System Memory 200-pin DDR2 SODIMM x 1, supports DDR2 400/533 up to 2GB
- Chipset Intel® System Controller Hub US15W
- I/O Chipset Intel® System Controller Hub US15W
- Ethernet Intel® 82574L for 10/100/1000Base-TX Ethernet
- BIOS Award BIOS v8.0, TSOP type, 1MB ROM
- H/W status monitoring CPU Temperature Monitoring (Optional)
- Watchdog Timer Fintek F75111
- Power Requirement Wide DC Input Range, +8.5V DC to +19V DC
- Board Size 3.75" (L) x 3.75" (W) (95mm x 95mm)
- Gross Weight 0.55 lb (0.25kg)

- Operating Temperature 32°F~140°F (0°C~60°C)
- Storage Temperature -40°F~176°F (-40°C~80°C)
- Operating Humidity 0%~90% relative humidity, non-condensing

***Display: Supports LCD/DVI or LCD/LCD (via SDVO)***

***Simultaneous/ Dual View Displays***

- Chipset Intel® System Controller Hub  
US15W integrated
- Memory Shared system memory up to 256MB
- Resolution Up to 1366 x 768 @ 85Hz (Max. pixel clock of 112MHz) for LVDS;  
Up to 1280 x 1024 @ 85Hz (Max. pixel clock of 160MHz) for SDVO
- LCD Interface Up to 24-bit single channel  
LVDS
- SDVO Supports SDVO x 1

***I/O***

- Storage
  1. PATA SSD onboard (Master device), Max. 4GB;
  2. PATA x 1 (One device) or SATA II x 1

- USB USB2.0 x 8
- Audio High Definition Audio
- GPIO Up to 4 in or 4 out: Multiplexed with 4-bit SDIO

## Chapter

# 2

## Quick Installation Guide

*Notice:*

*The Quick Installation Guide is derived from Chapter 2 of user manual. For other chapters and further installation instructions, please refer to the user manual CD-ROM that came with the product.*



## 2.1 Safety Precautions

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### **Warning!**



*Always completely disconnect the power cord from your board whenever you are working on it. Do not make connections while the power is on, because a sudden rush of power can damage sensitive electronic components.*

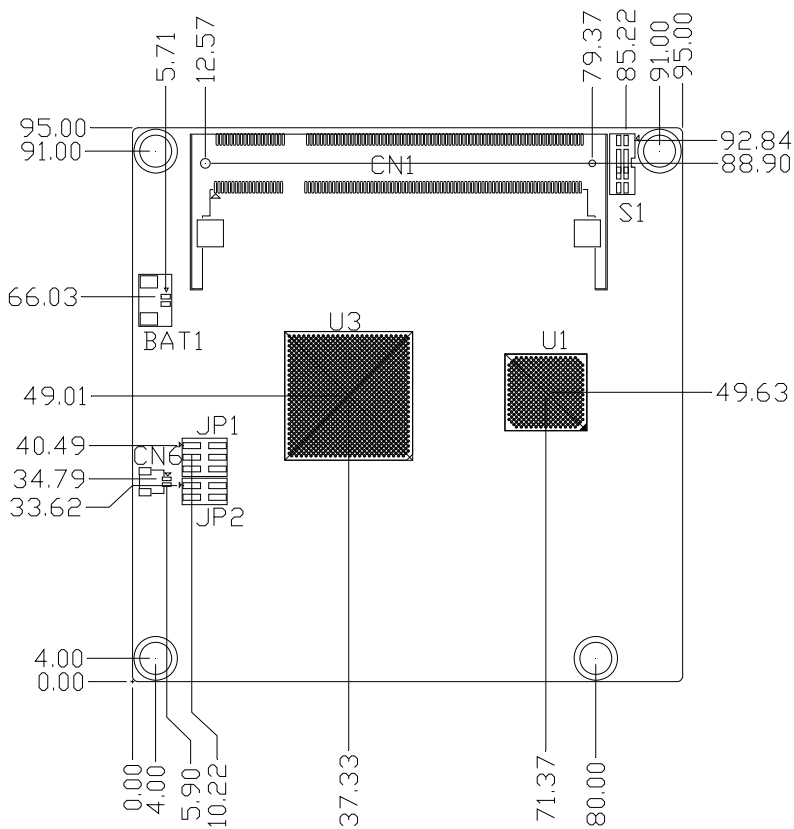
### **Caution!**



*Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis*

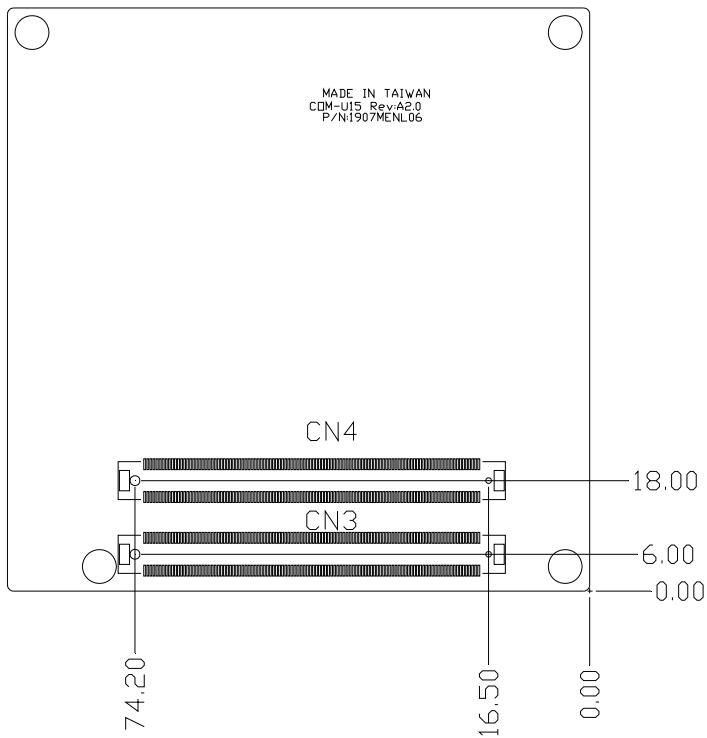
## 2.2 Location of Connectors/ Jumpers & Mechanical Drawings

### Component Side





Solder Side



## 2.3 List of Jumpers/ Connectors/ Switches

The board has a number of jumpers that allow you to configure your system to suit your application.

The table below shows the function of them:

Label	Function
JP1	CPLD Writing Programming Connector
JP2	SSD Writing Protection and SATA Bridge Master/ Slave Setting and SSD Master/ Slave Setting
S1	AT/ATX Setting Switch
BAT1	RTC Battery Connector
CN1	SODIMM
CN3	COM Express Row A/B Connector
CN4	COM Express Row C/D Connector
CN6	SCI & SMI Connector

## 2.4 CPLD Writing Programming Connector (JP1)

Pin	Signal	Pin	Signal
1	TMS	2	TDI
3	TDO	4	TCK
5	GND	6	+3.3V_DUAL

## 2.5 SSD Writing Protection and SATA Bridge Master/ Slave Setting and SSD Master/ Slave Setting (JP2)

Label	Function
1-2 (Short)	Writing Protection
1-2 (Open)	Unprotected

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3-4 (Short) Set JM20330 (SATA Bridge) as Device 0 (Master)

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3-4 (Open) Set JM20330 (SATA Bridge) as Device 1 (Slave)

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5-6 (Short) Set SSD as Device 0 (Master)

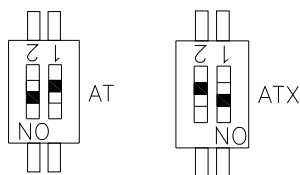
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5-6 (Open) Set SSD as Device 1 (Slave)

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## 2.6 AT/ATX Selection (S1)

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Label	Function
1 (On), 2 (Off)	ATX (Default)
1 (Off), 2 (On)	AT

## 2.7 RTC Battery Connector (BAT1)

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Pin	Signal
1	+3.3V_BAT
2	GND

## 2.8 SODIMM (CN1)

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Standard DDR2 SODIMM

## 2.9 COM Express Row A/B Connector (CN3)

Row A		Row B	
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK#	B8	N.C.
A9	GBE0_MDI1-	B9	N.C.
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	N.C.
A17	SATA0_TX-	B17	N.C.
A18	N.C.	B18	SUS_STAT#
A19	SATA0_RX+	B19	N.C.
A20	SATA0_RX-	B20	N.C.
A21	GND (FIXED)	B21	GND (FIXED)

A22	N.C.	B22	N.C.
A23	N.C.	B23	N.C.
A24	SUS_S5#	B24	PWR_OK
A25	N.C.	B25	N.C.
A26	N.C.	B26	N.C.
A27	N.C.	B27	WDT
A28	DASP_L	B28	N.C.
A29	AC_SYNC	B29	AC_SDIN1
A30	AC_RST#	B30	AC_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR
A33	AC_SDOUT	B33	I2C_CK
A34	BIOS_DISABLE#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB3-	B36	USB2-
A37	USB3+	B37	USB2+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB6-	B39	USB7-
A40	USB6+	B40	USB7+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB4-	B42	USB5-
A43	USB4+	B43	USB5+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-

A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	N.C.
A48	EXCD0_PERST#	B48	N.C.
A49	N.C.	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	N.C.	B52	N.C.
A53	N.C.	B53	N.C.
A54	GPI0 D54	B54	GPO1
A55	N.C.	B55	N.C.
A56	N.C.	B56	N.C.
A57	GND	B57	GPO2
A58	N.C.	B58	N.C.
A59	N.C.	B59	N.C.
A60	GND (FIXED)	B60	GND (FIXED)
A61	N.C.	B61	N.C.
A62	N.C.	B62	N.C.
A63	GPI1	B63	GPO3
A64	N.C.	B64	N.C.
A65	N.C.	B65	N.C.
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-

A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+	B71	N.C.
A72	LVDS_A0-	B72	N.C.
A73	LVDS_A1+	B73	N.C.
A74	LVDS_A1-	B74	N.C.
A75	LVDS_A2+	B75	N.C.
A76	LVDS_A2-	B76	N.C.
A77	LVDS_VDD_EN	B77	N.C.
A78	LVDS_A3+	B78	N.C.
A79	LVDS_A3-	B79	LVDS_BKLT_EN
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+	B81	N.C.
A82	LVDS_A_CK-	B82	N.C.
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	KBD_RST#	B86	VCC_5V_SBY
A87	N.C.	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	RSVD
A89	PCIE0_CK_REF-	B89	N.C.
A90	GND (FIXED)	B90	GND (FIXED)
A91	RSVD (EC_SCI)	B91	N.C.
A92	RSVD (SMI#)	B92	N.C.
A93	GPO0	B93	N.C.

A94	RSVD	B94	N.C.
A95	RSVD	B95	N.C.
A96	GND	B96	N.C.
A97	VCC_12V	B97	N.C.
A98	VCC_12V	B98	N.C.
A99	VCC_12V	B99	N.C.
A100	GND (FIXED)	B100	GND (FIXED)
A101	VCC_12V	B101	VCC_12V
A102	VCC_12V	B102	VCC_12V
A103	VCC_12V	B103	VCC_12V
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)

**Note:** Multi-function pins for 4-bit SDIO

Pin	GPIO	SDIO	Pin	GPIO	SDIO
A54	GPIO0	DATA0	B54	GPO1	CMD
A63	GPI1	DATA1	B57	GPO2	WP
A67	GPI2	DATA2	B63	GPO3	CD#
A85	GPI3	DATA3			
A93	GPO0	CLK			



## 2.10 COM Express Row C/D Connector (CN4)

Row C		Row D	
C1	GND (FIXED)	D1	GND (FIXED)
C2	IDE_PDD7	D2	IDE_PDD5
C3	IDE_PDD6	D3	IDE_PDD10
C4	IDE_PDD3	D4	IDE_PDD11
C5	IDE_PDD15	D5	IDE_PDD12
C6	IDE_PDD8	D6	IDE_PDD4
C7	IDE_PDD9	D7	IDE_PDD0
C8	IDE_PDD2	D8	IDE_PDDREQ
C9	IDE_PDD13	D9	IDE_PDIOW#
C10	IDE_PDD1	D10	IDE_PDDACK#
C11	GND (FIXED)	D11	GND (FIXED)
C12	IDE_PDD14	D12	INT_IRQ14
C13	IDE_PDIPRDY	D13	IDE_PDA0
C14	IDE_PDIOR#	D14	IDE_PDA1
C15	N.C.	D15	IDE_PDA2
C16	N.C.	D16	IDE_PDICS1#
C17	N.C.	D17	IDE_PDICS3#
C18	N.C.	D18	IDERST#
C19	N.C.	D19	N.C.
C20	N.C.	D20	N.C.
C21	GND (FIXED)	D21	GND (FIXED)

C22	N.C.	D22	N.C.
C23	N.C.	D23	N.C.
C24	N.C.	D24	N.C.
C25	N.C.	D25	N.C.
C26	N.C.	D26	N.C.
C27	N.C.	D27	N.C.
C28	N.C.	D28	N.C.
C29	N.C.	D29	N.C.
C30	N.C.	D30	N.C.
C31	GND (FIXED)	D31	GND (FIXED)
C32	N.C.	D32	N.C.
C33	N.C.	D33	N.C.
C34	N.C.	D34	N.C.
C35	N.C.	D35	N.C.
C36	SLOT0_DATA4_R	D36	N.C.
C37	N.C.	D37	N.C.
C38	N.C.	D38	N.C.
C39	N.C.	D39	N.C.
C40	SLOT0_CMD_R	D40	N.C.
C41	GND (FIXED)	D41	GND (FIXED)
C42	N.C.	D42	N.C.
C43	N.C.	D43	SLOT0_DATA7_R
C44	SLOT0_DATA1_R	D44	N.C.
C45	SLOT0_CD#_R	D45	SLOT0_DATA2_R

C46	SLOT0_WP_R	D46	SLOT0_CLK_R
C47	SLOT0_DATA3_R	D47	SLOT0_DATA0_R
C48	SLOT0_DATA6_R	D48	SLOT0_DATA5_R
C49	N.C.	D49	SLOT0_VDD
C50	N.C.	D50	N.C.
C51	GND (FIXED)	D51	GND (FIXED)
C52	PEG_RX0+	D52	PEG_TX0+
C53	PEG_RX0-	D53	PEG_TX0-
C54	N.C.	D54	N.C.
C55	PEG_RX1+	D55	PEG_TX1+
C56	PEG_RX1-	D56	PEG_TX1-
C57	N.C.	D57	N.C.
C58	PEG_RX2+	D58	PEG_TX2+
C59	PEG_RX2-	D59	PEG_TX2-
C60	GND (FIXED)	D60	GND (FIXED)
C61	PEG_RX3+	D61	PEG_TX3+
C62	PEG_RX3-	D62	PEG_TX3-
C63	RSVD	D63	RSVD
C64	RSVD	D64	RSVD
C65	N.C.	D65	N.C.
C66	N.C.	D66	N.C.
C67	RSVD (DASP for IDE)	D67	GND
C68	N.C.	D68	N.C.
C69	N.C.	D69	N.C.

C70	GND (FIXED)	D70	GND (FIXED)
C71	N.C.	D71	N.C.
C72	N.C.	D72	N.C.
C73	SDVO_DATA	D73	SDVO_CLK
C74	N.C.	D74	N.C.
C75	N.C.	D75	N.C.
C76	GND	D76	GND
C77	RSVD	D77	P66DET
C78	N.C.	D78	N.C.
C79	N.C.	D79	N.C.
C80	GND (FIXED)	D80	GND (FIXED)
C81	N.C.	D81	N.C.
C82	N.C.	D82	N.C.
C83	RSVD	D83	RSVD
C84	GND	D84	GND
C85	N.C.	D85	N.C.
C86	N.C.	D86	N.C.
C87	GND	D87	GND
C88	N.C.	D88	N.C.
C89	N.C.	D89	N.C.
C90	GND (FIXED)	D90	GND (FIXED)
C91	N.C.	D91	N.C.
C92	N.C.	D92	N.C.
C93	GND	D93	GND

C94	N.C.	D94	N.C.
C95	N.C.	D95	N.C.
C96	GND	D96	GND
C97	RSVD	D97	N.C.
C98	N.C.	D98	N.C.
C99	N.C.	D99	N.C.
C100	GND (FIXED)	D100	GND (FIXED)
C101	N.C.	D101	N.C.
C102	N.C.	D102	N.C.
C103	GND	D103	GND
C104	VCC_12V	D104	VCC_12V
C105	VCC_12V	D105	VCC_12V
C106	VCC_12V	D106	VCC_12V
C107	VCC_12V	D107	VCC_12V
C108	VCC_12V	D108	VCC_12V
C109	VCC_12V	D109	VCC_12V
C110	GND (FIXED)	D110	GND (FIXED)

## 2.11 SCI & SMI Connector (CN6)

Pin	Signal
1	EC_SCI
2	SMI#

## Below Table for China RoHS Requirements

产品中有毒有害物质或元素名称及含量

## AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	×	○	○	○	○	○
外部信号 连接器及线材	×	○	○	○	○	○
<p><b>O:</b> 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。</p> <p><b>X:</b> 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。</p> <p>备注: 此产品所标示之环保使用期限, 系指在一般正常使用状况下。</p>						

Chapter

3

**Award  
BIOS Setup**

### 3.1 System Test and Initialization

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These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors. Non-fatal error messages usually appear on the screen along with the following instructions:

Press <F1> to RESUME

Write down the message and press the F1 key to continue the boot up sequence.

#### System configuration verification

These routines check the current system configuration against the values stored in the CMOS memory. If they do not match, the program outputs an error message. You will then need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The CMOS memory has lost power and the configuration information has been erased.



## 3.2 Award BIOS Setup

---

Awards BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM so that it retains the Setup information when the power is turned off.

### Entering Setup

Power on the computer and press <Del> immediately. This will allow you to enter Setup.

### Standard CMOS Features

Use this menu for basic system configuration. (Date, time, IDE, etc.)

### Advanced BIOS Features

Use this menu to set the advanced features available on your system.

### Advanced Chipset Features

Use this menu to change the values in the chipset registers and optimize your system performance.

### Integrated Peripherals

Use this menu to specify your settings for integrated peripherals. (Primary slave, secondary slave, keyboard, mouse etc.)

### Power Management Setup

Use this menu to specify your settings for power management. (HDD power down, power on by ring, KB wake up, etc.)

### PnP/PCI Configurations

This entry appears if your system supports PnP/PCI.

## **PC Health Status**

This menu allows you to set the shutdown temperature for your system.

## **Frequency/Voltage Control**

Use this menu to specify your settings for auto detect DIMM/PCI clock and spread spectrum.

## **Load Fail-Safe Defaults**

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

## **Load Optimized Defaults**

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While AWARD has designated the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

## **Set Supervisor/User Password**

Use this menu to set Supervisor/User Passwords.

## **Save and Exit Setup**

Save CMOS value changes to CMOS and exit setup.

## **Exit Without Saving**

Abandon all CMOS value changes and exit setup.

**You can refer to the "AAEON BIOS Item Description.pdf" file in the CD for the meaning of each setting in this chapter.**

Chapter

4

**Driver  
Installation**

The COM-U15 comes with an AutoRun CD-ROM that contains all drivers and utilities that can help you to install the driver automatically.

Insert the driver CD, the driver CD-title will auto start and show the installation guide. If not, please follow the sequence below to install the drivers.

***Follow the sequence below to install the drivers:***

Step 1 – Install INF Driver

Step 2 – Install VGA Driver

Step 3 – Install LAN Driver

Step 4 – Install Audio Driver (For ECB-951D)

Step 5 – Install Touch Panel Driver (For ECB-951D)

USB 2.0 Drivers are available for download using Windows<sup>®</sup> Update for both Windows<sup>®</sup> XP and Windows<sup>®</sup> 2000. For additional information regarding USB 2.0 support in Windows<sup>®</sup> XP and Windows<sup>®</sup> 2000, please visit [www.microsoft.com/hwdev/usb/](http://www.microsoft.com/hwdev/usb/).

Please read instructions below for further detailed installations.

## 4.1 Installation:

---

Insert the COM-U15 CD-ROM into the CD-ROM drive. And install the drivers from Step 1 to Step 5 in order.

### Step 1 – Install INF Driver

1. Click on the **Step 1 – INF** folder and double click on the ***Infinst\_autol.exe***
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

### Step 2 – Install VGA Driver

1. Click on the **Step 2 – VGA** folder and double click on the ***Setup.exe***
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

### Step 3 – Install LAN Driver

1. Click on the **Step 3 – LAN** folder and double click on the ***pro2kxp\_v13\_1\_2.exe***
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

### Step 4 – Install Audio Driver (For ECB-951D)

1. Click on the **Step 4 – Audio** folder and double click on

**Setup.exe**

2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

## Step 5 – Install Touch Panel Driver (For ECB-951D)

1. Click on the **Step 5 – Touch Panel** folder and double click on the **Setup.exe**
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

Appendix

**A**

# Programming the Watchdog Timer

## A.1 Programming

---

```
#include <stdio.h>
```

```
#include <conio.h>
```

```
void functionA();
```

```
void functionB();
```

```
void functionC();
```

```
void functionD();
```

```
void functionE();
```

```
void Chk_Ready();
```

```
#define SMBus_Port 0x500
```

```
int i;
```

```
int j;
```

```
int inputbuffer;
```

```
int index;
```

```
void main (void)
```

```
{
```



```
char option_var='x';

//device ID(smbus):6Eh,index:03h data:03h

    outportb(SMBus_Port+0x04,0x6E);

        delay(5);

    outportb(SMBus_Port+0x02,0x54);

        delay(5) ;

    outportb(SMBus_Port+0x03,0x00);

        delay(5) ;

    outportb(SMBus_Port+0x05,0x03);

        delay(5) ;

    outportb(SMBus_Port+0x06,0x03);

        delay(5) ;

    outportb(SMBus_Port+0x00,0x08);

        delay(5) ;

    outportb(SMBus_Port+0x01,0x0F);

        delay(5) ;

    outportb(SMBus_Port+0x00,0x12);

        delay(5) ;
```

```
Chk_Ready();
```

```
while(option_var!='0')
{
    printf("0.quit\n");
    printf("1. 5 sec \n");
    printf("2. 10 sec \n");
    printf("3. 60 sec \n");
    printf("4. 256 sec \n");
    printf("Please Select One option\n");
    option_var = getchar();
    getchar();
    printf("input = %c ,pls wait\n",option_var);

    switch(option_var)
    {
```

```
        case '0':  
            printf("exit program \n");  
            break;  
        case '1':  
            functionA();  
            break;  
        case '2':  
            functionB();  
            break;  
        case '3':  
            functionC();  
            break;  
        case '4':  
            functionD();  
            break;  
    }  
}  
exit(0);
```

```
}
```

```
void functionA()
```

```
{
```

```
    outportb(SMBus_Port+0x05,0x37);
```

```
        delay(5) ;
```

```
    outportb(SMBus_Port+0x06,0x05);
```

```
        delay(5) ;
```

```
    outportb(SMBus_Port+0x00,0x08);
```

```
        delay(5) ;
```

```
    outportb(SMBus_Port+0x01,0x0F);
```

```
        delay(5) ;
```

```
    outportb(SMBus_Port+0x00,0x12);
```

```
        delay(5) ;
```

```
    Chk_Ready();
```

```
    outportb(SMBus_Port+0x05,0x36);
```

```
        delay(5) ;
```

```
    outportb(SMBus_Port+0x06,0x73);
```

```
        delay(5) ;
        outportb(SMBus_Port+0x00,0x08);
        delay(5) ;
        outportb(SMBus_Port+0x01,0x0F);
        delay(5) ;
        outportb(SMBus_Port+0x00,0x12);
        delay(5) ;
        Chk_Ready();

    }

void functionB()
{
    outportb(SMBus_Port+0x05,0x37);
    delay(5) ;
    outportb(SMBus_Port+0x06,0x0A);
    delay(5) ;
    outportb(SMBus_Port+0x00,0x08);
    delay(5) ;
```

```
    outportb(SMBus_Port+0x01,0x0F);  
        delay(5) ;  
    outportb(SMBus_Port+0x00,0x12);  
        delay(5) ;  
    Chk_Ready();  
  
    outportb(SMBus_Port+0x05,0x36);  
        delay(5) ;  
    outportb(SMBus_Port+0x06,0x73);  
        delay(5) ;  
    outportb(SMBus_Port+0x00,0x08);  
        delay(5) ;  
    outportb(SMBus_Port+0x01,0x0F);  
        delay(5) ;  
    outportb(SMBus_Port+0x00,0x12);  
        delay(5) ;  
    Chk_Ready();  
  
}
```

```
void functionC()
{
    outportb(SMBus_Port+0x05,0x37);
        delay(5) ;
    outportb(SMBus_Port+0x06,0x3C);
        delay(5) ;
    outportb(SMBus_Port+0x00,0x08);
        delay(5) ;
    outportb(SMBus_Port+0x01,0x0F);
        delay(5) ;
    outportb(SMBus_Port+0x00,0x12);
        delay(5) ;
    Chk_Ready();

    outportb(SMBus_Port+0x05,0x36);
        delay(5) ;
    outportb(SMBus_Port+0x06,0x73);
        delay(5) ;
    outportb(SMBus_Port+0x00,0x08);
```

```
        delay(5) ;  
        outputb(SMBus_Port+0x01,0x0F);  
        delay(5) ;  
        outputb(SMBus_Port+0x00,0x12);  
        delay(5) ;  
        Chk_Ready();  
    }
```

```
void functionD()  
{  
    outputb(SMBus_Port+0x05,0x37);  
        delay(5) ;  
    outputb(SMBus_Port+0x06,0xFF);  
        delay(5) ;  
    outputb(SMBus_Port+0x00,0x08);  
        delay(5) ;  
    outputb(SMBus_Port+0x01,0x0F);  
        delay(5) ;  
    outputb(SMBus_Port+0x00,0x12);
```



```
        delay(5) ;  
    Chk_Ready();  
  
    outportb(SMBus_Port+0x05,0x36);  
        delay(5) ;  
    outportb(SMBus_Port+0x06,0x73);  
        delay(5) ;  
    outportb(SMBus_Port+0x00,0x08);  
        delay(5) ;  
    outportb(SMBus_Port+0x01,0x0F);  
        delay(5) ;  
    outportb(SMBus_Port+0x00,0x12);  
        delay(5) ;  
    Chk_Ready();  
}  
  
void Chk_Ready()  
  
{
```

```
index=0;
while(index<0x800)
{
    inputbuffer=inportb(SMBus_Port+0x01);
    delay(5);

    if((inputbuffer&0x08)==0)
        return;
    index++;

}
outportb(SMBus_Port+0x00,0x08);
delay(5);
}
```

Appendix

**B**

# I/O Information

## B.1 I/O Address Map

Input/output (IO)	
[00000000 - 0000000F]	Direct memory access controller
[00000000 - 00000CF7]	PCI bus
[00000010 - 0000001F]	Motherboard resources
[00000020 - 00000021]	Programmable interrupt controller
[00000022 - 0000002D]	Motherboard resources
[00000030 - 0000003F]	Motherboard resources
[00000040 - 00000043]	System timer
[00000044 - 0000005F]	Motherboard resources
[00000061 - 00000061]	System speaker
[00000062 - 00000063]	Motherboard resources
[00000065 - 0000006F]	Motherboard resources
[00000070 - 00000073]	System CMOS/real time clock
[00000074 - 0000007F]	Motherboard resources
[00000080 - 00000090]	Direct memory access controller
[00000091 - 00000093]	Motherboard resources
[00000094 - 0000009F]	Direct memory access controller
[000000A0 - 000000A1]	Programmable interrupt controller
[000000A2 - 000000BF]	Motherboard resources
[000000C0 - 000000DF]	Direct memory access controller
[000000E0 - 000000EF]	Motherboard resources
[000000F0 - 000000FF]	Numeric data processor
[00000170 - 00000177]	Secondary IDE Channel
[000001F0 - 000001F7]	Primary IDE Channel
[00000274 - 00000277]	ISAPNP Read Data Port
[00000279 - 00000279]	ISAPNP Read Data Port
[00000376 - 00000376]	Secondary IDE Channel
[000003B0 - 000003BB]	Intel(R) Graphics Media Accelerator 500
[000003C0 - 000003DF]	Intel(R) Graphics Media Accelerator 500
[000003F6 - 000003F6]	Primary IDE Channel
[000004D0 - 000004D1]	Motherboard resources
[00000880 - 0000088F]	Motherboard resources
[00000900 - 000009BF]	Motherboard resources
[00000A79 - 00000A79]	ISAPNP Read Data Port
[00000D00 - 0000FFFF]	PCI bus
[0000D000 - 0000DFFF]	Intel(R) SCH Family PCI Express Root Port 3 - 8112
[0000DF00 - 0000DF1F]	Intel(R) 82574L Gigabit Network Connection
[0000E000 - 0000EFFF]	Intel(R) SCH Family PCI Express Root Port 1 - 8110
[0000FB00 - 0000FB0F]	Standard Dual Channel PCI IDE Controller
[0000FC00 - 0000FC1F]	Intel(R) SCH Family USB Universal Host Controller - 8116
[0000FD00 - 0000FD1F]	Intel(R) SCH Family USB Universal Host Controller - 8115
[0000FE00 - 0000FE1F]	Intel(R) SCH Family USB Universal Host Controller - 8114
[0000FF00 - 0000FF07]	Intel(R) Graphics Media Accelerator 500

## B.2 Memory Address Map

Address Range	Device
[00000000 - 0009FFFF]	System board
[000A0000 - 000BFFFF]	Intel(R) Graphics Media Accelerator 500
[000A0000 - 000BFFFF]	PCI bus
[000C0000 - 000DFFFF]	PCI bus
[000E0000 - 000EFFFF]	PCI bus
[000E0000 - 000EFFFF]	System board
[000F0000 - 000FFFFF]	PCI bus
[000F0000 - 000FFFFF]	System board
[00100000 - 0F6DFFFF]	System board
[0F6E0000 - 0F6FFFFF]	System board
[0F700000 - 0F7FFFFF]	System board
[0F800000 - FEBFFFFF]	PCI bus
[D0000000 - DFFFFFFF]	Intel(R) Graphics Media Accelerator 500
[E0000000 - EFFFFFFF]	Motherboard resources
[FD800000 - FDBFFFFF]	Intel(R) SCH Family PCI Express Root Port 3 - 8112
[FDC00000 - FDCFFFFF]	Intel(R) SCH Family PCI Express Root Port 3 - 8112
[FDC00000 - FDC0FFFF]	Intel(R) 82574L Gigabit Network Connection
[FDCFC000 - FDCFFFFF]	Intel(R) 82574L Gigabit Network Connection
[FDD00000 - FDDFFFFF]	Intel(R) SCH Family PCI Express Root Port 1 - 8110
[FDE00000 - FDEFFFFF]	Intel(R) SCH Family PCI Express Root Port 1 - 8110
[FDF00000 - FDF7FFFF]	Intel(R) Graphics Media Accelerator 500
[FDF80000 - FDFBFFFF]	Intel(R) Graphics Media Accelerator 500
[FDF80000 - FDFBFFFF]	Microsoft UAA Bus Driver for High Definition Audio
[FDFFC000 - FDFFC0FF]	SDA Standard Compliant SD Host Controller
[FDFFD000 - FDFFD0FF]	SDA Standard Compliant SD Host Controller
[FDFFE000 - FDFFE0FF]	SDA Standard Compliant SD Host Controller
[FDFFF000 - FDFFF3FF]	Intel(R) SCH Family USB2 Enhanced Host Controller - 8117
[FEC00000 - FEC00FFF]	System board
[FED00000 - FED000FF]	System board
[FED00000 - FED003FF]	High precision event timer
[FED13000 - FED1DFFF]	System board
[FED20000 - FED8FFFF]	System board
[FEE00000 - FEE00FFF]	System board
[FFB00000 - FFB7FFFF]	System board
[FFB80000 - FFBFFFFF]	Intel(R) 82802 Firmware Hub Device
[FFF00000 - FFFFFFFF]	System board

### B.3 IRQ Mapping Chart

---

Interrupt request (IRQ)	
(ISA) 0	High precision event timer
(ISA) 8	High precision event timer
(ISA) 9	Microsoft ACPI-Compliant System
(ISA) 13	Numeric data processor
(ISA) 14	Primary IDE Channel
(PCI) 16	Intel(R) Graphics Media Accelerator 500
(PCI) 16	Intel(R) SCH Family PCI Express Root Port 1 - 8110
(PCI) 16	Intel(R) SCH Family USB Universal Host Controller - 8114
(PCI) 16	Microsoft UAA Bus Driver for High Definition Audio
(PCI) 16	SDA Standard Compliant SD Host Controller
(PCI) 17	Intel(R) 82574L Gigabit Network Connection
(PCI) 17	Intel(R) SCH Family PCI Express Root Port 3 - 8112
(PCI) 17	Intel(R) SCH Family USB Universal Host Controller - 8115
(PCI) 17	SDA Standard Compliant SD Host Controller
(PCI) 18	Intel(R) SCH Family USB Universal Host Controller - 8116
(PCI) 18	SDA Standard Compliant SD Host Controller
(PCI) 19	Intel(R) SCH Family USB2 Enhanced Host Controller - 8117

### B.4 DMA Channel Assignments

---

Direct memory access (DMA)	
4	Direct memory access controller