ADLD25PC

Manual

rev. 1.3

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Contents

0 Document History

Version	Changes
0.1	first pre-release
1.0	first released version
1.1	- new photographs - now D525-only - 4GB max RAM - added notes concerning memory frequency and RS485 mode - minor changes and additions
1.2	- bottom photo now also showing mPCIe socket - symbols for LAN and Audio headers rotated by 180°
1.3	- improved output quality of dimensional drawings

NOTE

All company names, brand names, and product names referred to in this manual are registered or unregistered trademarks of their respective holders and are, as such, protected by national and international law.

1 Introduction

1.1 Important Notes

Please read this manual carefully before you begin installation of this hardware device. To avoid Electrostatic Discharge (ESD) or transient voltage damage to the board, adhere to the following rules at all times:

- You must discharge your body from electricity before touching this board.
- Tools you use must be discharged from electricity as well.
- Please ensure that neither the board you want to install, nor the unit on which you want to install this board, is energized before installation is completed.
- Please do not touch any devices or components on the board.

CAUTION

As soon as the board is connected to a working power supply, touching the board may result in electrical shock, even if the board has not been switched on yet. Please also note that the mounting holes for heat sinks are connected to ground, so when using an externally AC powered device, a substantial ground plane differential can occur if the external device's AC power supply or cable does not include an earth ground. This could also result in electrical shock when touching the device and the heat sink simultaneously.

1.2 Technical Support

Technical support for this product can be obtained in the following ways:

- By contacting our support staff at +1 858-490-0597 or +49 (0) 271 250 810 0
- By contacting our staff via e-mail at support@adl-usa.com or support@adl-europe.com
- Via our website at www.adl-usa.com/support or www.adl-europe.com/support

1.3 Warranty

This product is warranted to be free of defects in workmanship and material. ADL Embedded Solutions' sole obligation under this warranty is to provide replacement parts or repair services at no charge, except shipping cost. Such defects which appear within 12 months of original shipment of ADL Embedded Solutions will be covered, provided a written claim for service under warranty is received by ADL Embedded Solutions no less then 30 days prior to the end of the warranty period of within 30 days of discovery of the defect – whichever comes first. Warranty coverage is contingent upon proper handling and operation of the product. Improper use such as unauthorized modifications or repair, operation outside of specified ratings, or physical damage may void any service claims under warranty.

1.4 Return Authorization

All equipment returned to ADL Embedded Solutions for evaluation, repair, credit return, modification, or any other reason must be accompanied by a Return Material Authorization (RMA) number. ADL Embedded Solutions requires a completed RMA request form to be submitted in order to issue an RMA number. The form can be found under the Support section at our website: www.adl-usa.com or www.adl-europe.com. Submit the completed form to support@adl-usa.com or fax to +1 858-490-0599 for the USA office, or to rma@adl-europe.com or fax to +49 (0) 271 250 810 20 to request an RMA from the European office in Germany. Following a review of the information provided, ADL Embedded Solutions will issue an RMA number.

1.5 Description of Safety Symbols

The following safety symbols are used in this documentation. They are intended to alert the reader to the associated safety instructions.

ACUTE RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is immediate danger to life and health of individuals!

RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is danger to life and health of individuals!

HAZARD TO INDIVIDUALS, ENVIRONMENT, DEVICES, OR DATA!

If you do not adhere to the safety advise next to this symbol, there is obvious hazard to individuals, to environment, to materials, or to data.

NOTE OR POINTER

This symbol indicates information that contributes to better understanding.

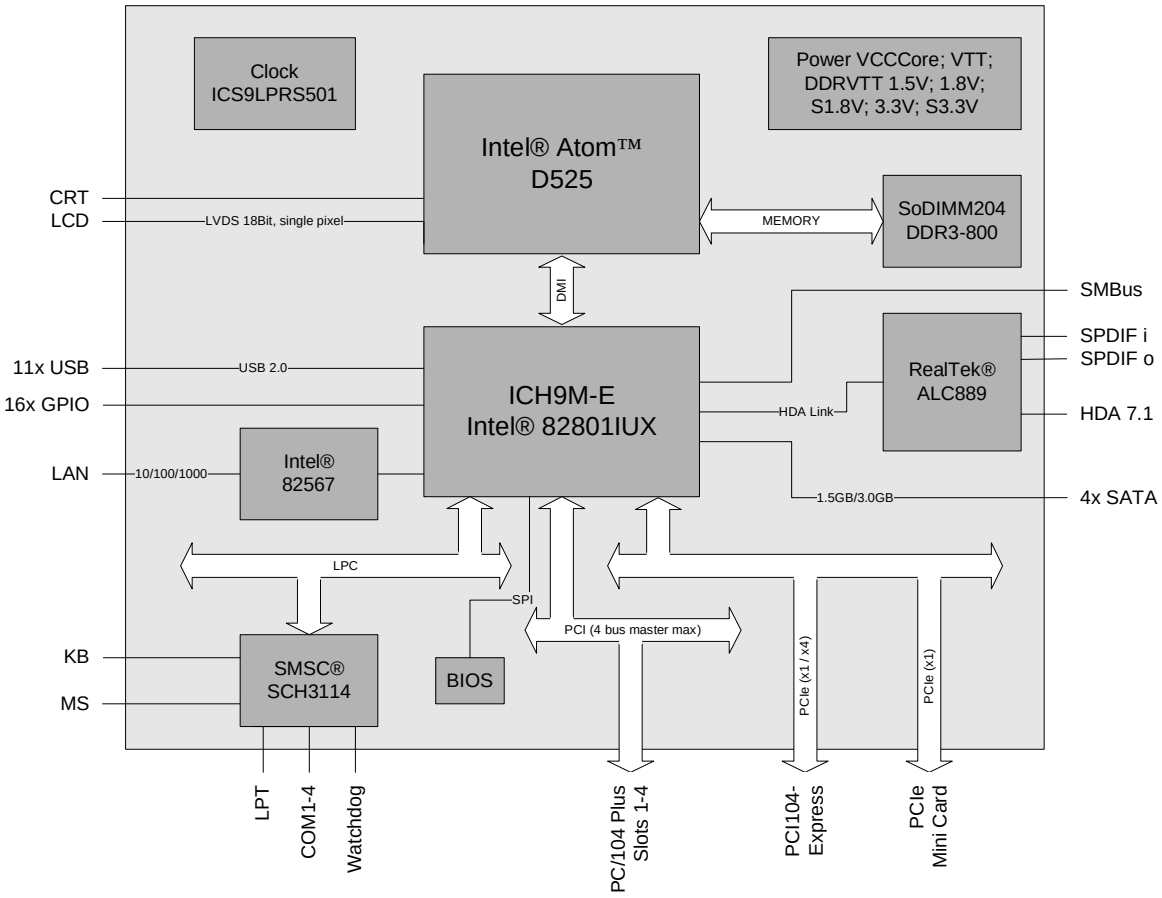
1.6 RoHS

The PCB and all components are RoHS compliant (RoHS = Restriction of Hazardous Substances Directive). The soldering process is lead free.

2 Overview

2.1 Features

The ADLD25PC is a highly complex computer motherboard in the PC/104™ form factor, complying with the state-of-the-art "PCI/104-Express™" standard. It's based on Intel®'s Atom® D525 CPUs combined with the ICH9M-E chip (SFF). Modern DDR3 technology provides top-notch memory performance, accomodating up to 4 GByte of RAM (DDR3-800) via SO-DIMM204. PCI bus and PCI-Express are available through the PC/104-Plus and PCI/104-Express Type 2 connectors respectively, giving system builders a great deal of flexibility as far as expansion cards are concerned. An optional PCIe Mini Card connector adds to that picture. Additional onboard peripheral devices include four serial interfaces, one Gigabit Ethernet interface (LAN), up to four SATA channels, an audio interface (HDA 7.1), up to eleven USB channels and CRT and LVDS/TFT support. There are also 16 discrete programmable GPIO signals available.



- o Processor Intel® Atom® D525 (Dualcore, 1.8 GHz, 13W TDP)
- o Chipset Intel® ICH9M-E (SFF)
- o SO-DIMM204 socket for one DDR3-800 module of up to 4 GByte
- o Four serial interfaces COM1-4
- o LAN interface Ethernet 10/100/1000 (Base-T)
- o Four SATA channels (two of which on the PCI104-Express connector)
- o PS2 keyboard / mouse interface
- o LPT interface

- Up to eleven USB 2.0 interfaces (two on PCI104-Express connector, one on Mini Card)
- AWARD BIOS 6.10
- CRT connection
- LCD connection via LVDS 18Bit (single pixel)
- HDA compatible sound controller with SPDIF in and out
- RTC with external CMOS battery
- PCI bus via PC/104-Plus (max. four master devices)
- PCI-Express bus via PCI/104-Express connector (type 2, four x1 lanes)
- PCI-Express Mini Card connector (option, one x1 lane)
- 16x GPIO
- 5V and 12V supply voltage
- Size: 96 mm x 90 mm

2.2 Specifications and Documents

In making this manual and for further reading of technical documentation, the following documents, specifications and web-pages were used and are recommended.

- § PC/104™ Specification
  Version 2.5
  www.pc104.org
- § PC/104-Plus™ Specification
  Version 2.3
  www.pc104.org
- § PCI104-Express™ Specification
  Version 1.1
  www.pc104.org
- § PCI-Express® Mini Card Specification
  Version 1.2
  www.pcisig.com
- § PCI Specification
  Version 2.3 and 3.0
  www.pcisig.com
- § ACPI Specification
  Version 3.0
  www.acpi.info
- § ATA/ATAPI Specification
  Version 7 Rev. 1
  www.t13.org
- § USB Specifications
  www.usb.org
- § SM-Bus Spedifidation
  Version 2.0
  www.smbus.org
- § Intel®-Chip Description
  Atom® D425/D525
  www.intel.com
- § Intel® Chip Description
  Intel® ICH9 Datasheet
  www.intel.com
- § Intel® Chip Description
  82567 Datasheet
  www.intel.com
- § SMSC® Chip Description
  SCH3114 Datasheet
  www.smsc.com
- § IDT® Chip Description
  ICS9LPRS501SKLF Datasheet
  www.idt.com
- § Realtek® Chip Description
  ALC889 Datasheet
  www.realtek.com.tw

3 Connectors

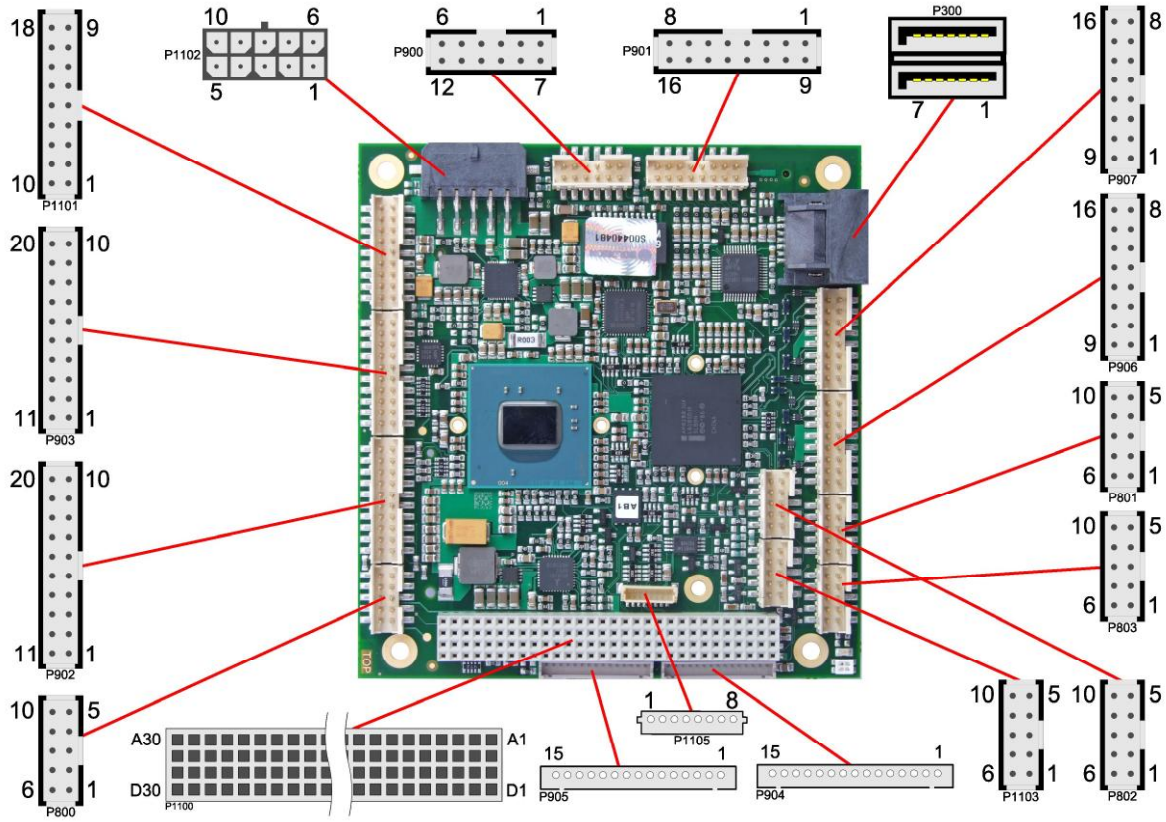
This section describes all the connectors found on the ADLD25PC.

CAUTION

For most interfaces, the cables must meet certain requirements. For instance, USB 2.0 requires twisted and shielded cables to reliably maintain full speed data rates. Restrictions on maximum cable length are also in place for many high speed interfaces and for power supply. Please refer to the respective specifications and use suitable cables at all times.

3.1 Connector Map

Please use the connector map below for quick reference. Only connectors on the component side are shown. For more information on each connector refer to the table below.



Ref-No.	Function	Page
P300	"SATA Interfaces"	p. 31
U400*	"Memory"	p. 15
P800/P803	"COM1 and COM2"	p. 32
P801/P802	"COM3 and COM4"	p. 33
P900	"LAN"	p. 30
P901	"Audio"	p. 27
P902	"Parallel Interface LPT"	p. 34
P903	"GPIO"	p. 35
P904/P905	"LCD"	p. 25
P906/P907	"USB"	p. 28
P1000	"PCI/104-Express Bus"	p. 20
P1001*	"PCI-Express Mini Card"	p. 22
P1100	"PC/104-Plus Bus"	p. 18
P1101	"System/SM-Bus"	p. 14
P1102	"Power Supply"	p. 13
P1103	"VGA"	p. 24
P1105	"Monitoring Functions"	p. 36

* not in the picture above (cf. bottom side of board)

3.2 Power Supply

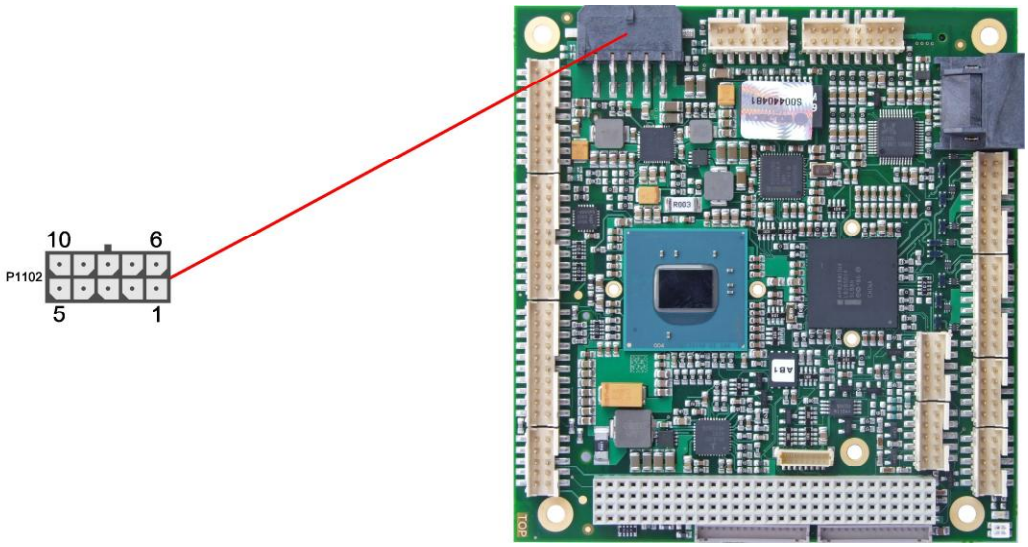
The power supply of the hardware module is realized via a 2x5-pin connector (Molex PS 43045-10xx, mating connector: Molex PS 43025-10xx). The 12V input can be left unconnected if not required by attached peripherals.

CAUTION

The ADLD25PC includes circuitry that will notify an intelligent power supply to shut down if the processor reaches a critical temperature. This is achieved by deasserting the (low-active) PS_ON# signal found on the SM-Bus connector. When PS_ON# is no longer pulled low, an intelligent power supply would take this as a signal to shut down power. For this to work, PS_ON# must be connected to the power supply's PS_ON input. If PS_ON# is not otherwise connected, the ADLD25PC can be damaged beyond repair if a thermal shutdown event occurs. In rare instances, if power is not shut down, the board will continue to heat up until failure occurs.

NOTE

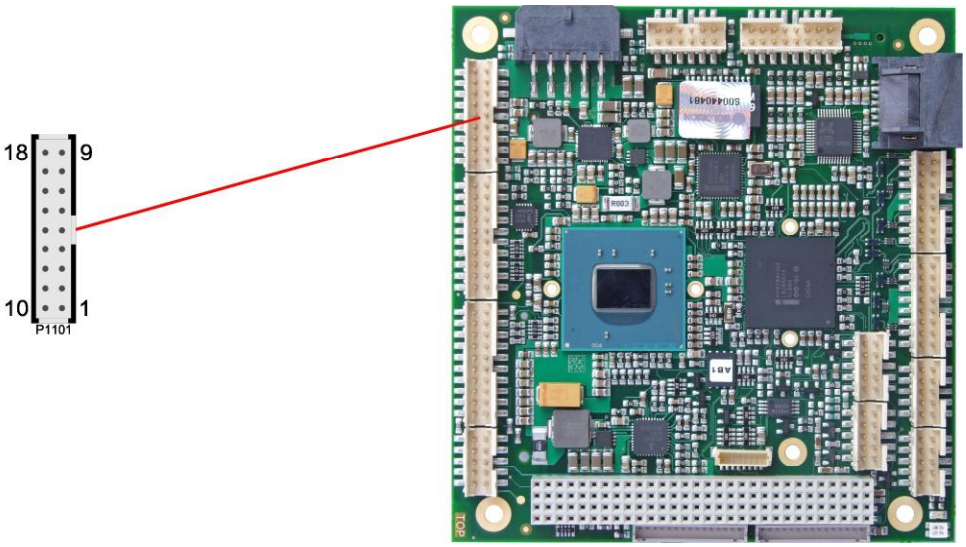
Since this is a 90 degree connector, the symbol in the drawing below represents the connector face as seen from the side (PCB on bottom) rather than from above.



Description	Name	Pin		Name	Description
12 volt supply	12V	1	6	12V	12 volt supply
ground	GND	2	7	GND	ground
ground	GND	3	8	SVCC	standby-supply 5V
ground	GND	4	9	GND	ground
5 volt supply	VCC	5	10	VCC	5 volt supply

3.3 System/SM-Bus

Both SM-Bus signals, and signals for PS/2 keyboard, PS/2 mouse and speaker are provided through a 2x9pin connector (FCI 98424-G52-18LF, mating connector e.g. FCI 90311-018LF). For the #PSON signal, please refer to the cautionary note in the chapter "Power Supply" (p. 13).



Pinout 2x9pin connector:

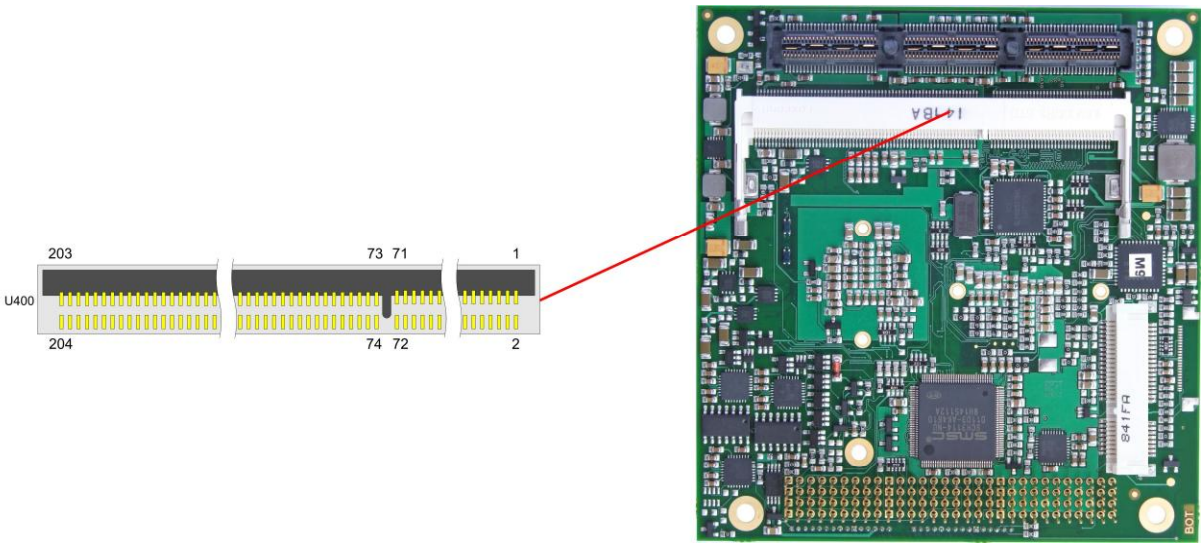
Description	Name	Pin		Name	Description
speaker to 5V	SPEAKER	1	10	GND	ground
reset to ground	RSTBTN#	2	11	N/C	reserved
keyboard data	KDAT	3	12	KCLK	keyboard clock
mouse data	MDAT	4	13	MCLK	mouse clock
battery	BATT	5	14	VCC	5 volt supply
power supply on	PS-ON#	6	15	SMBCLK	SMB clock
standby supply 3.3V	S3.3V	7	16	SMBDAT	SMB data
power button	PWRBTN#	8	17	SMBALERT#	SMB alert
ground	GND	9	18	3.3V	3.3 volt supply

3.4 Memory

There is one conventional SO-DIMM204 socket available to equip the board with memory (DDR3-800). It is located on the bottom side of the board. For technical and mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your sales representative for recommended memory modules.
With currently available SO-DIMM modules a memory extension up to 4 GByte is possible. The timing parameters for different memory modules are automatically set by BIOS.

NOTE

It is not necessary that the memory modules' rated speed and the motherboard's specified memory bus speed match exactly. The system will automatically configure the fastest mutually supported memory bus speed available. For best performance, however, the memory modules' rated speed should be equal to or faster than the motherboard's specified memory bus speed.



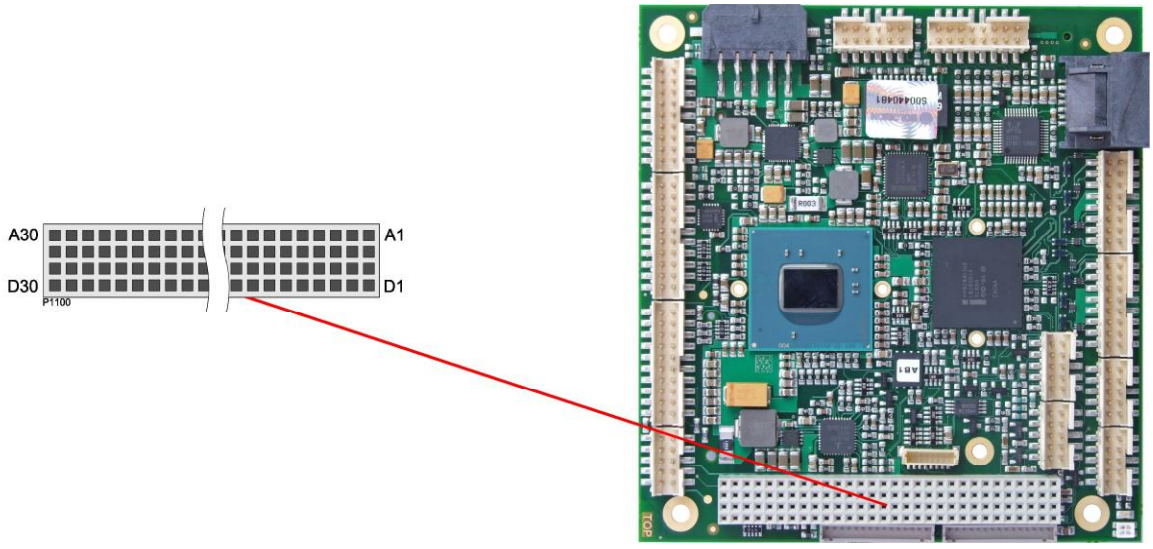
Description	Name	Pin		Name	Description
memory reference current	REF-DQ	1	2	GND	ground
ground	GND	3	4	DQ4	data 4
data 0	DQ0	5	6	DQ5	data 5
data 1	DQ1	7	8	GND	ground
ground	GND	9	10	DQS0#	data strobe 0 -
data mask 0	DM0	11	12	DQS0	data strobe 0 +
ground	GND	13	14	GND	ground
data 2	DQ2	15	16	DQ6	data 6
data 3	DQ3	17	18	DQ7	data 7
ground	GND	19	20	GND	ground
data 8	DQ8	21	22	DQ12	data 12
data 9	DQ9	23	24	DQ13	data 13
ground	GND	25	26	GND	ground
data strobe 1 -	DQS1#	27	28	DM1	data mask 1
data strobe 1 +	DQS1	29	30	RESET#	Reset
ground	GND	31	32	GND	ground
data 10	DQ10	33	34	DQ14	data 14
data 11	DQ11	35	36	DQ15	data 15

Description	Name	Pin		Name	Description
ground	GND	37	38	GND	ground
data 16	DQ16	39	40	DQ20	data 20
data 17	DQ17	41	42	DQ21	data 21
ground	GND	43	44	GND	ground
data strobe 2 -	DQS2#	45	46	DM2	data mask 2
data strobe 2 +	DQS2	47	48	GND	ground
ground	GND	49	50	DQ22	data 22
data 18	DQ18	51	52	DQ23	data 23
data 19	DQ19	53	54	GND	ground
ground	GND	55	56	DQ28	data 28
data 24	DQ24	57	58	DQ29	data 29
data 25	DQ25	59	60	GND	ground
ground	GND	61	62	DQS3#	data strobe 3 -
data mask 3	DQM3	63	64	DQS3	data strobe 3 +
ground	GND	65	66	GND	ground
data 26	DQ26	67	68	DQ30	data 30
data 27	DQ27	69	70	DQ31	data 31
ground	GND	71	72	GND	ground
clock enables 0	CKE0	73	74	CKE1	clock enables 1
1.5 volt supply	1.5V	75	76	1.5V	1.5 volt supply
reserved	N/C	77	78	(A15)	reserved
SDRAM bank 2	BA2	79	80	A14	address 14
1.5 volt supply	1.5V	81	82	1.5V	1.5 volt supply
address 12 (burst chop)	A12/BC#	83	84	A11	address 11
address 9	A9	85	86	A7	address 7
1.5 volt supply	1.5V	87	88	1.5V	1.5 volt supply
address 8	A8	89	90	A6	address 6
address 5	A5	91	92	A4	address 4
1.5 volt supply	1.5V	93	94	1.5V	1.5 volt supply
address 3	A3	95	96	A2	address 2
address 1	A1	97	98	A0	address 0
1.5 volt supply	1.5V	99	100	1.5V	1.5 volt supply
Clock 0 +	CK0	101	102	CK1	clock 1 +
Clock 0 -	CK0#	103	104	CK1#	clock 1 -
1.5 volt supply	1.5V	105	106	1.5V	1.5 volt supply
address 10 (auto precharge)	A10/AP	107	108	BA1	SDRAM bank 1
SDRAM Bank 0	BA0	109	110	RAS#	row address strobe
1.5 volt supply	1.5V	111	112	1.5V	1.5 volt supply
write enable	WE#	113	114	S0#	chip select 0
column address strobe	CAS#	115	116	ODT0	on die termination 0
1.5 volt supply	1.5V	117	118	1.5V	1.5 volt supply
address 13	A13	119	120	ODT1	on die termination 1
Chip Select 1	S1#	121	122	N/C	reserved
1.5 volt supply	1.5V	123	124	1.5V	1.5 volt supply
reserved	(TEST)	125	126	REF-CA	reference current
ground	GND	127	128	GND	ground
data 32	DQ32	129	130	DQ36	data 36
data 33	DQ33	131	132	DQ37	data 37
ground	GND	133	134	GND	ground
data strobe 4 -	DQS4#	135	136	DQM4	data mask 4
data strobe 4 +	DQS4	137	138	GND	ground
ground	GND	139	140	DQ38	data 38
data 34	DQ34	141	142	DQ39	data 39
data 35	DQ35	143	144	GND	ground
ground	GND	145	146	DQ44	data 44

Description	Name	Pin		Name	Description
data 40	DQ40	147	148	DQ45	data 45
data 41	DQ41	149	150	GND	ground
ground	GND	151	152	DQS5#	data strobe 5 -
data mask 5	DQM5	153	154	DQS5	data strobe 5 +
ground	GND	155	156	GND	ground
data 42	DQ42	157	158	DQ46	data 46
data 43	DQ43	159	160	DQ47	data 47
ground	GND	161	162	GND	ground
data 48	DQ48	163	164	DQ52	data 52
data 49	DQ49	165	166	DQ53	data 53
ground	GND	167	168	GND	ground
data strobe 6 -	DQS6#	169	170	DQM6	data mask 6
data strobe 6	DQS6	171	172	GND	ground
ground	GND	173	174	DQ54	data 54
data 50	DQ50	175	176	DQ55	data 55
data 51	DQ51	177	178	GND	ground
ground	GND	179	180	DQ60	data 60
data 56	DQ56	181	182	DQ61	data 61
data 57	DQ57	183	184	GND	ground
ground	GND	185	186	DQS7#	data strobe 7 -
data mask 7	DQM7	187	188	DQS7	data strobe 7 +
ground	GND	189	190	GND	ground
data 58	DQ58	191	192	DQ62	data 62
data 59	DQ59	193	194	DQ63	data 63
ground	GND	195	196	GND	ground
SPD address 0	SA0	197	198	EVENT#	Event
3.3 volt supply	3.3V	199	200	SDA	SMBus data
SPD address 1	SA1	201	202	SCL	SMBus clock
termination current	VTT	203	204	VTT	termination current

3.5 PC/104-Plus Bus

Expansion cards can be connected to the board using the PCI connector first introduced with the PC/104-Plus standard. A maximum of four PC/104-Plus cards are supported.
The interrupt routing and the IDSEL signals for the expansion cards are specified in the PC/104-Plus specification (see "Specifications and Documents", p. 10).

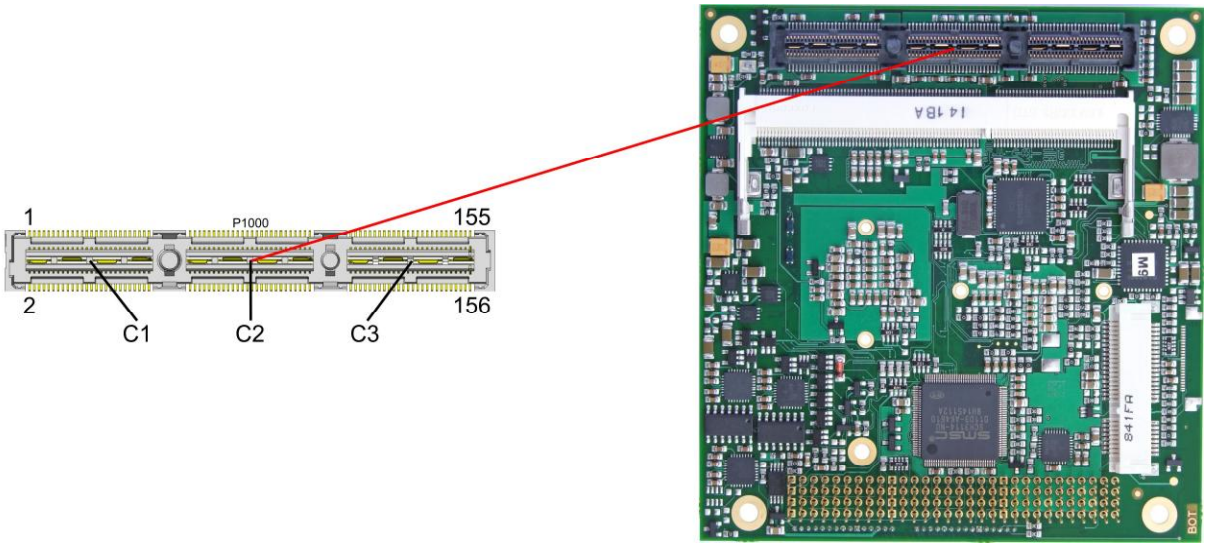


Description	Name	Pin		Name	Description
ground	GND	A1	B1	N/C	reserved
3.3 volt - IO buffer power	VIO	A2	B2	AD2	PCI – address/data 2
PCI – address/data 5	AD5	A3	B3	GND	ground
PCI – com/byte enable 0	CBE0#	A4	B4	AD7	PCI – address/data 7
ground	GND	A5	B5	AD9	PCI – address/data 9
PCI – address/data 11	AD11	A6	B6	VIO	3.3 volt - IO buffer power
PCI – address/data 14	AD14	A7	B7	AD13	PCI – address/data 13
3.3 volt supply	3.3V	A8	B8	CBE1#	PCI – com/byte enable 1
PCI – system error	SERR#	A9	B9	GND	ground
ground	GND	A10	B10	PERR#	PCI – parity error
PCI – stop	stop#	A11	B11	3.3V	3.3 volt supply
3.3 volt supply	3.3V	A12	B12	TRDY#	PCI – target ready
PCI – frame	FRAME#	A13	B13	GND	ground
ground	GND	A14	B14	AD16	PCI – address/data 16
PCI – address/data 18	AD18	A15	B15	3.3V	3.3 volt supply
PCI – address/data 21	AD21	A16	B16	AD20	PCI – address/data 20
3.3 volt supply	3.3V	A17	B17	AD23	PCI – address/data 23
PCI – ID select slot 1	IDSEL0	A18	B18	GND	ground
PCI – address/data 24	AD24	A19	B19	CBE3#	PCI – com/byte enable 3
ground	GND	A20	B20	AD26	PCI – address/data 26
PCI – address/data 29	AD29	A21	B21	VCC	5 volt supply
5 volt supply	VCC	A22	B22	AD30	PCI – address/data 30
PCI – bus request slot 1	REQ0#	A23	B23	GND	ground
ground	GND	A24	B24	REQ2#	PCI – bus request slot 3
PCI – bus grant slot 4	GNT1#	A25	B25	VIO	5 volt - IO buffer power
5 volt supply	VCC	A26	B26	CLK0	PCI – clock slot 1
PCI – clock slot 3	CLK2	A27	B27	VCC	5 volt supply

Description	Name	Pin		Name	Description
ground	GND	A28	B28	INTD#	PCI – interrupt D
12V supply	12V	A29	B29	INTA#	PCI – interrupt A
-12V supply	-12V	A30	B30	REQ3#	PCI – bus request slot 4
5 volt supply	VCC	C1	D1	AD0	PCI – address/data 0
PCI – address/data 1	AD1	C2	D2	VCC	5 volt supply
PCI – address/data 4	AD4	C3	D3	AD3	PCI – address/data 3
ground	GND	C4	D4	AD6	PCI – address/data 6
PCI – address/data 8	AD8	C5	D5	GND	ground
PCI – address/data 10	AD10	C6	D6	M66EN	PCI – 66MHz enable
ground	GND	C7	D7	AD12	PCI – address/data 12
PCI – address/data 15	AD15	C8	D8	3.3V	3.3 volt supply
reserved	N/C	C9	D9	PAR	PCI – parity bit
3.3 volt supply	3.3V	C10	D10	N/C	reserved
PCI – lock	LOCK#	C11	D11	GND	ground
ground	GND	C12	D12	DEVSEL#	PCI – device select
PCI – initiator ready	IRDY#	C13	D13	3.3V	3.3 volt supply
3.3 volt supply	3.3V	C14	D14	CBE2#	PCI – com/byte enable 2
PCI – address/data 17	AD17	C15	D15	GND	ground
ground	GND	C16	D16	AD19	PCI – address/data 19
PCI – address/data 22	AD22	C17	D17	3.3V	3.3 volt supply
PCI – ID select slot 2	IDSEL1	C18	D18	IDSEL2	PCI – ID select slot 3
3,3 volt - IO buffer power	VIO	C19	D19	IDSEL3	PCI – ID select slot 4
PCI – address/data 25	AD25	C20	D20	GND	ground
PCI – address/data 28	AD28	C21	D21	AD27	PCI – address/data 27
ground	GND	C22	D22	AD31	PCI – address/data 31
PCI – bus request slot 2	REQ1#	C23	D23	VIO	3,3 volt - IO buffer power
5 volt supply	VCC	C24	D24	GNT0#	PCI – bus grant slot 1
PCI – bus grant slot 3	GNT2#	C25	D25	GND	ground
ground	GND	C26	D26	CLK1	PCI – clock slot 2
PCI – clock slot 4	CLK3	C27	D27	GND	ground
5 volt supply	VCC	C28	D28	RST#	PCI – reset
PCI – interrupt B	INTB#	C29	D29	INTC#	PCI – interrupt C
PCI – bus grant slot 4	GNT3#	C30	D30	GND	ground

3.6 PCI/104-Express Bus

Expansion modules for the PCI-Express bus can be connected to the board using the PCI/104-Express™ connector. This is a "type 2" connector with only those signals connected that are supported by the chipset. "Stacking Error" functionality is available. For specifics, please refer to the PCI/104-Express™ documentation (rev. 2.0).



Pinout PCI104-Express connector (type 2):

Description	Name	Pin		Name	Description
USB overcurrent	USBOC#	1	2	PERST#	PCIe reset
3.3 volt supply	3.3V	3	4	3.3V	3.3 volt supply
USB11 +	USB11	5	6	USB10	USB10 +
USB11 -	USB11#	7	8	USB10#	USB10 -
ground	GND	9	10	GND	ground
transmit lane 2 +	PET2	11	12	PET1	transmit Lane 1 +
transmit lane 2 -	PET2#	13	14	PET1#	transmit lane 1 -
ground	GND	15	16	GND	ground
transmit lane 3 +	PET3	17	18	PET4	transmit lane 4 +
transmit lane 3 -	PET3#	19	20	PET4#	transmit lane 4 -
ground	GND	21	22	GND	ground
receive lane 2 +	PER2	23	24	PER1	receive lane 1 +
receive lane 2 -	PER2#	25	26	PER1#	receive lane 1 -
ground	GND	27	28	GND	ground
receive lane 3 +	PER3	29	30	PER4	receive lane 4 +
receive lane 3 -	PER3#	31	32	PER4#	receive lane 4 -
ground	GND	33	34	GND	ground
clock slot 1 +	PECLK1	35	36	PECLK0	clock slot 0 +
clock slot 1 -	PECLK1#	37	38	PECLK0#	clock slot 0 -
5 volt standby supply	SVCC	39	40	SVCC	5 volt standby supply
clock slot 2 +	PECLK2	41	42	PECLK3	clock slot 3 +
clock slot 2 -	PECLK2#	43	44	PECLK3#	clock slot 3 -
CPU direction	CPU_DIR	45	46	PWRGOOD	powergood
SMBus data	SMBDAT	47	48	N/C	reserved
SMBus clock	SMBCLK	49	50	N/C	reserved
SMBus alert	SMBALERT	51	52	PSON#	power supply on
link reactivation	PEWAKE#	53	54	ST1-ERR#	stacking error 1

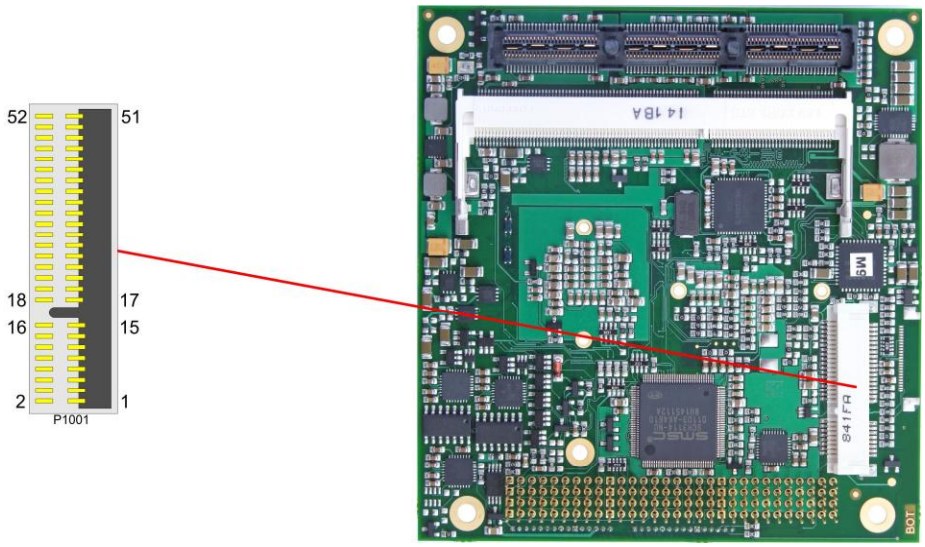
Description	Name	Pin		Name	Description
ground	GND	55	56	GND	ground
reserved	N/C	57	58	N/C	reserved
reserved	N/C	59	60	N/C	reserved
ground	GND	61	62	GND	ground
reserved	N/C	63	64	N/C	reserved
reserved	N/C	65	66	N/C	reserved
ground	GND	67	68	GND	ground
reserved	N/C	69	70	N/C	reserved
reserved	N/C	71	72	N/C	reserved
ground	GND	73	74	GND	ground
reserved	N/C	75	76	N/C	reserved
reserved	N/C	77	78	N/C	reserved
ground	GND	79	80	GND	ground
SATA5 send +	SATA5TX	81	82	SATA4TX	SATA4 send +
SATA5 send -	SATA5TX#	83	84	SATA4TX#	SATA4 send -
ground	GND	85	86	GND	ground
reserved	N/C	87	88	N/C	reserved
reserved	N/C	89	90	N/C	reserved
ground	GND	91	92	GND	ground
reserved	N/C	93	94	N/C	reserved
reserved	N/C	95	96	N/C	reserved
ground	GND	97	98	GND	ground
SATA5 detect	SATADET5#	99	100	SATADET4#	SATA4 detect
SATA5 power	SATAPW5#	101	102	SATAPW4#	SATA4 power
ground	GND	103	104	GND	ground
stacking error 2	ST2-ERR#	105	106	PCLKPCIE	PCI clock
ground	GND	107	108	GND	ground
reserved	N/C	109	110	N/C	reserved
reserved	N/C	111	112	N/C	reserved
ground	GND	113	114	GND	ground
reserved	N/C	115	116	N/C	reserved
reserved	N/C	117	118	N/C	reserved
ground	GND	119	120	GND	ground
reserved	N/C	121	122	N/C	reserved
reserved	N/C	123	124	N/C	reserved
ground	GND	125	126	GND	ground
reserved	N/C	127	128	N/C	reserved
reserved	N/C	129	130	N/C	reserved
ground	GND	131	132	GND	ground
SATA5 receive +	SATA5RX	133	134	SATA4RX	SATA4 receive +
SATA5 receive -	SATA5RX#	135	136	SATA4RX#	SATA4 receive -
ground	GND	137	138	GND	ground
reserved	N/C	139	140	N/C	reserved
reserved	N/C	141	142	N/C	reserved
ground	GND	143	144	GND	ground
LPC address/data 0	PELAD0	145	146	PEDRQ#	LPC DMA request
LPC address/data 1	PELAD1	147	148	PESIRQ#	LPC serial IRQ
ground	GND	149	150	GND	ground
LPC address/data 2	PELAD2	151	152	PEFRAME#	LPC frame
LPC address/data 3	PELAD3	153	154	RTCBATT	battery 3.3V
ground	GND	155	156	GND	ground
5 volt supply	VCC	C1			
5 volt supply	VCC	C2			
12 volt supply	12V	C3			

3.7 PCI-Express Mini Card

As a soldering option, the ADLD25PC can be equipped with PCI-Express Mini Card connector to interface with approved peripherals, such as Wi-FI and storage cards.

NOTE

The PCI-Express Mini Card option is not recommended for extended temperature applications and should be limited to environments of 0° C to +70° C or less, depending upon the installed PCI-Express Mini Card's environmental specification.

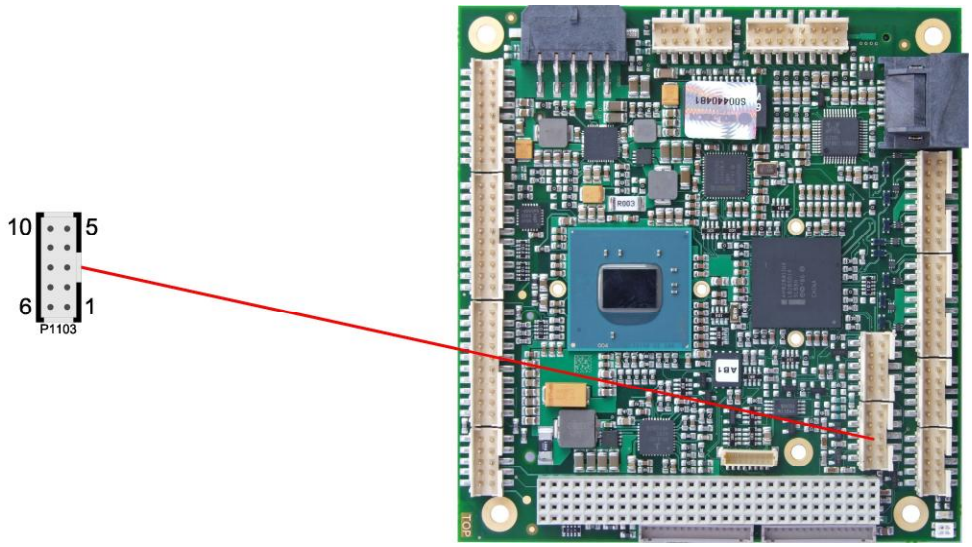


Description	Name	Pin		Name	Description
PCIe ake	PEWAKE#	1	2	S3.3V	3.3 volt standby supply
reserved	N/C	3	4	GND	ground
reserved	N/C	5	6	1.5V	1.5 volt supply
clock enable	PEMCLKen#	7	8	N/C	reserved
ground	GND	9	10	N/C	reserved
clock -	PECLKMC#	11	12	N/C	reserved
clock +	PECLKMC	13	14	N/C	reserved
ground	GND	15	16	N/C	reserved
reserved	N/C	17	18	GND	ground
reserved	N/C	19	20	WDISABLE#	wireless disable
ground	GND	21	22	PERST#	PCIe reset
PCIe receive -	PERMC#	23	24	S3.3V	3.3 volt standby supply
PCIe receive +	PERMC	25	26	GND	ground
ground	GND	27	28	1.5V	1.5 volt supply
ground	GND	29	30	SMB-CLK	SM-bus clock
PCIe transmit -	PETMC#	31	32	SMB-DAT	SM-bus data
PCIe transmit +	PETMC	33	34	GND	ground
ground	GND	35	36	USBMC#	USB -
ground	GND	37	38	USBMC	USB +
3.3 volt standby supply	S3.3V	39	40	GND	ground
3.3 volt standby supply	S3.3V	41	42	N/C	reserved
ground	GND	43	44	N/C	reserved
reserved	N/C	45	46	N/C	reserved

Description	Name	Pin		Name	Description
reserved	N/C	47	48	1.5V	1.5 volt supply
reserved	N/C	49	50	GND	ground
reserved	N/C	51	52	S3.3V	3.3 volt standby supply

3.8 VGA

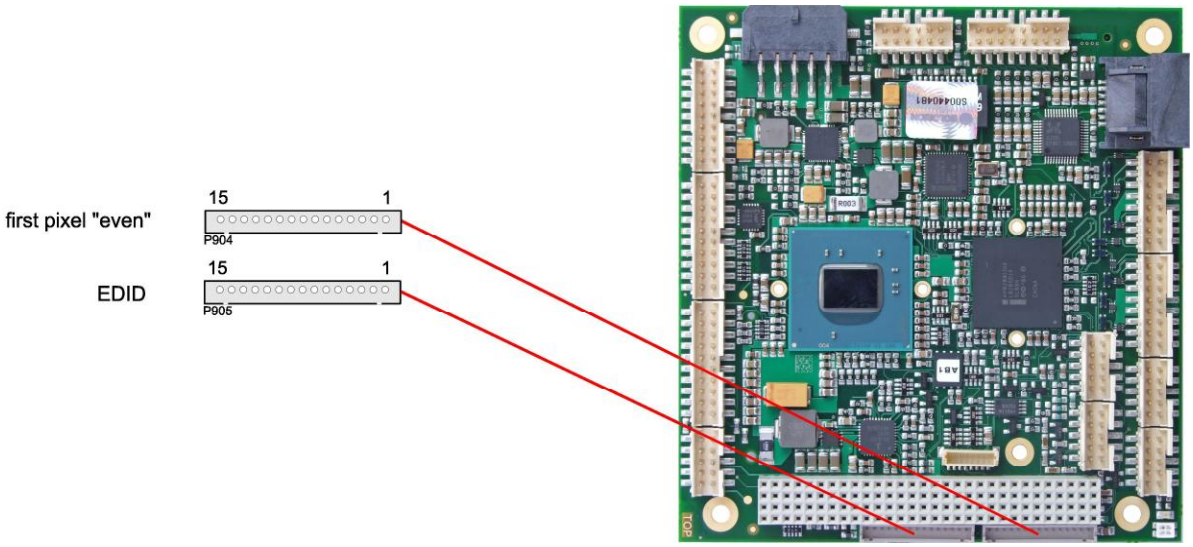
The CRT-VGA signals are provided by a 2x5pin connector (FCI 98424-G52-10LF, mating connector e.g. FCI 90311-010LF).
This interface allows the connection of a standard VGA-monitor. I2C communication is supported.



Description	Name	Pin		Name	Description
analog red	RED	1	6	GND	ground
analog green	GREEN	2	7	DDDA	DD data
analog blue	BLUE	3	8	DDCK	DD clock
vertikal sync	VSYNC	4	9	GND	ground
horizontal sync	HSYNC	5	10	GND	ground

3.9 LCD

The LCD is connected via two 15 pin connectors (Hirose DF13-15P-1.25DSA, mating connector: DF13-15S-xxx). The power supply for the display is also provided through these connectors. The ADLD25PC board only supports displays with LVDS interface. For displays with digital interface an extra receiver board is available. There is no support for DSTN displays.
With the LVDS interface it is possible to trigger LVDS displays with a maximum of 18 Bit colour depth and one or two pixels per clock. For single pixel displays only one connector is necessary. However, if you want to read the display's EDID data the second connector must be connected.
The display type can be chosen over the BIOS setup. Please contact your sales representative regarding an appropriate cable to connect your display.



The following table shows the pin description for the first bit ("even" pixel).

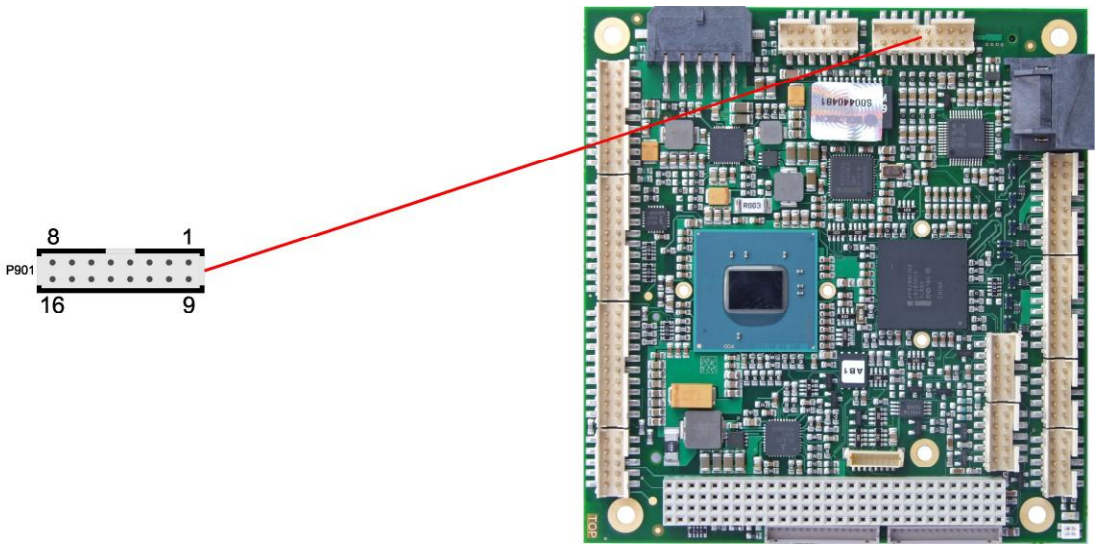
Pin	Name	Description
1	GND	ground
2	GND	ground
3	TXO00#	LVDS even data 0 -
4	TXO00	LVDS even data 0 +
5	TXO01#	LVDS even data 1 -
6	TXO01	LVDS even data 1 +
7	TXO02#	LVDS even data 2 -
8	TXO02	LVDS even data 2 +
9	TXO0C#	LVDS even clock -
10	TXO0C	LVDS even clock +
11	N/C	reserved
12	N/C	reserved
13	BL_VCC	switched 5 volt for backlight
14	FP_3.3V	switched 3.3 volt for display
15	FP_3.3V	switched 3.3 volt for display

The following table shows the pin description for the second connector used for evaluating the display's EDID data.

Pin	Name	Description
1	GND	ground
2	GND	ground
3	N/C	reserved
4	N/C	reserved
5	N/C	reserved
6	N/C	reserved
7	N/C	reserved
8	N/C	reserved
9	N/C	reserved
10	N/C	reserved
11	N/C	reserved
12	N/C	reserved
13	DDC_CLK	EDID clock for LCD
14	DDC_DAT	EDID data for LCD
15	VCC	5 volt supply

3.10 Audio

The ADLD25PC's audio functions are provided via a 2x8pin connector (FCI 98424-G52-16LF, mating connector e.g. FCI 90311-016LF). This interface provides eight output channels for full 7.1 sound output. Two microphone inputs and two AUX inputs are also available.
The signals "SPDIFI" and "SPDIFO" provide digital input and output. If a transformation to a coaxial or optical connector is necessary this must be performed externally.



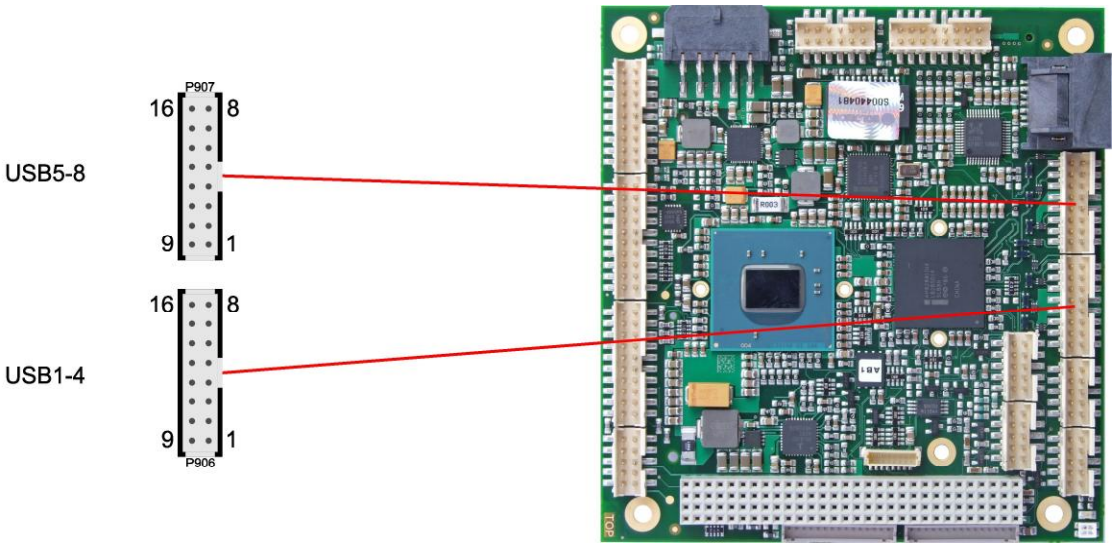
Description	Name	Pin		Name	Description
digital output SPDIF	SPDIFO	1	9	3.3V	3.3 volt supply
digital input SPDIF	SPDIFI	2	10	S_AGND	analog ground sound
sound output right	LOUT_R	3	11	LOUT_L	sound output left
AUX input right	AUXA_R	4	12	AUXA_L	AUX input left
microphone input 1	MIC1	5	13	MIC2	microphone input 2
surround out right	SOUT_R	6	14	SOUT_L	surround out left
center output	CENOUT	7	15	LFEOUT	LFE output
side surround out right	SSOUT_R	8	16	SSOUT_L	side surround out left

3.11 USB

USB channels 1 to 8 are provided via two 2x8pin connectors (FCI 98424-G52-16LF, mating connector e.g. FCI 90311-016LF).
All USB-channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with a USB keyboard without enabling USB keyboard support. Running a USB supporting OS (such as Microsoft® Windows®) with these features enabled may lead to significant performance or functionality limitations.
Every USB interface provides up to 500 mA current and is protected by an electronically resettable fuse.

NOTE

There are two more USB channels available on the PCI104-Express connector (p. 20) and another one on the Mini Card connector (if populated, p. 22).



Pinout USB 1-4:

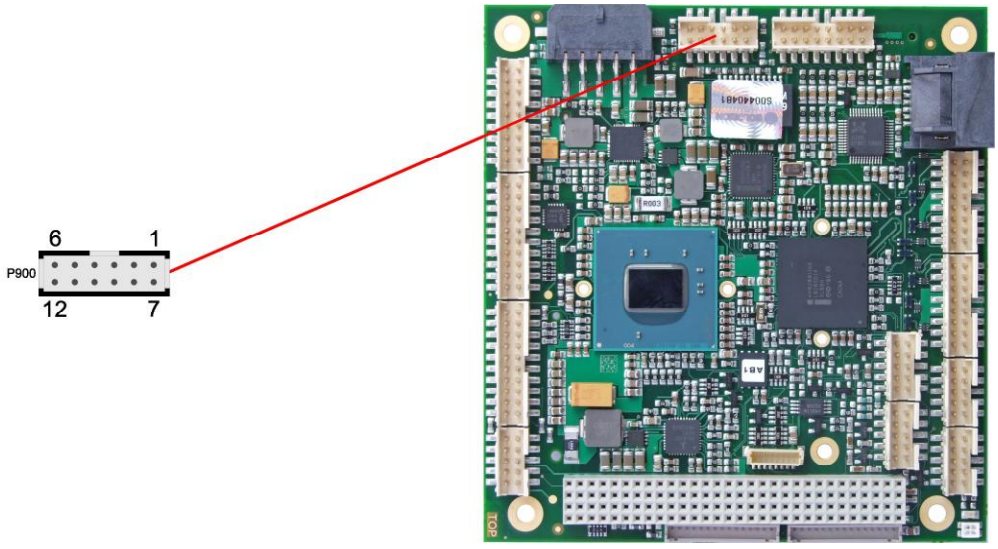
Description	Name	Pin		Name	Description
5 volt for USB1	USB1 VCC	1	9	USB2VCC	5 volt for USB2
minus channel USB1	USB1#	2	10	USB2#	minus channel USB2
plus channel USB1	USB1	3	11	USB2	plus channel USB2
ground	GND	4	12	GND	ground
ground	GND	5	13	GND	ground
plus channel USB3	USB3	6	14	USB4	plus channel USB4
minus channel USB3	USB3#	7	15	USB4#	minus channel USB4
5 volt for USB3	USB3VCC	8	16	USB4VCC	5 volt for USB4

Pinout USB 5-8:

Description	Name	Pin		Name	Description
5 volt for USB5	USB5 VCC	1	9	USB6VCC	5 volt for USB6
minus channel USB5	USB5#	2	10	USB6#	minus channel USB6
plus channel USB5	USB5	3	11	USB6	plus channel USB6
ground	GND	4	12	GND	ground
ground	GND	5	13	GND	ground
plus channel USB7	USB7	6	14	USB8	plus channel USB8
minus channel USB7	USB7#	7	15	USB8#	minus channel USB8
5 volt for USB7	USB7VCC	8	16	USB8VCC	5 volt for USB8

3.12 LAN

The LAN interface is provided via a 2x6pin connector (FCI 98424-G52-12LF, mating connector e.g. FCI 90311-012LF). The interface supports 10BaseT, 100BaseT, and 1000BaseT compatible network components with automatic bandwidth selection. Additional outputs are provided for status LEDs. Auto-negotiate and auto-cross functionality is available, PXE and RPL are available on request.



Pinout LAN interface:

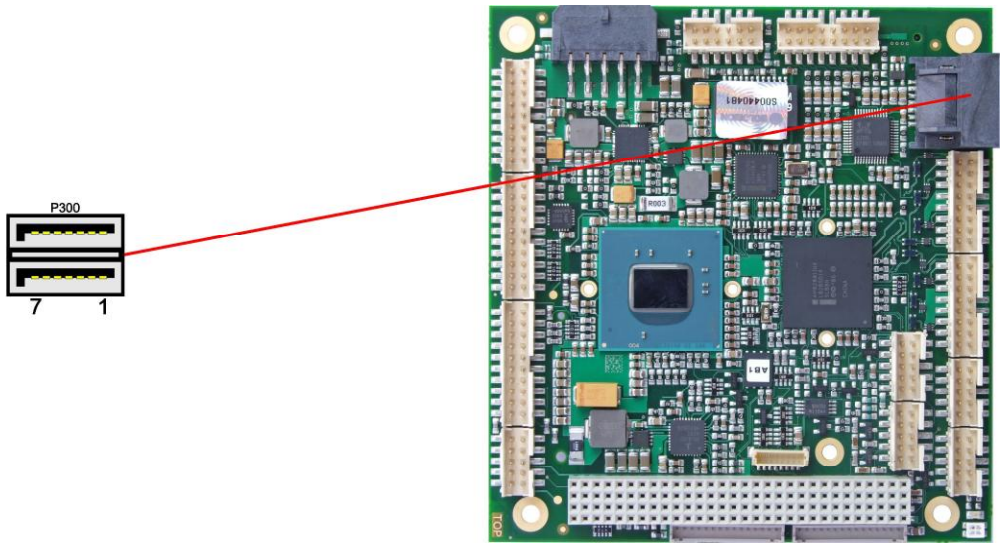
Description	Name	Pin		Name	Description
LAN activity	LINKACT	1	7	SPEED1000	LAN speed 1000Mbit
LAN channel 1 plus	LAN1	2	8	LAN0	LAN channel 0 plus
LAN channel 1 minus	LAN1#	3	9	LAN0#	LAN channel 0 minus
LAN channel 3 plus	LAN3	4	10	LAN2	LAN channel 2 plus
LAN channel 3 minus	LAN3#	5	11	LAN2#	LAN channel 2 minus
LAN speed 100Mbit	SPEED100	6	12	3.3V	3.3 volt supply

3.13 SATA Interfaces

The ADLD25PC provides two SATA interfaces allowing transfer rates of up to 3 Gbit per second. These interfaces are made available via two 7 pin connectors.
The required settings are made in the BIOS setup.

NOTE

There are two more SATA channels available on the PCI104-Express connector (p. 20), extending the available RAID options to 0/1/5/10.

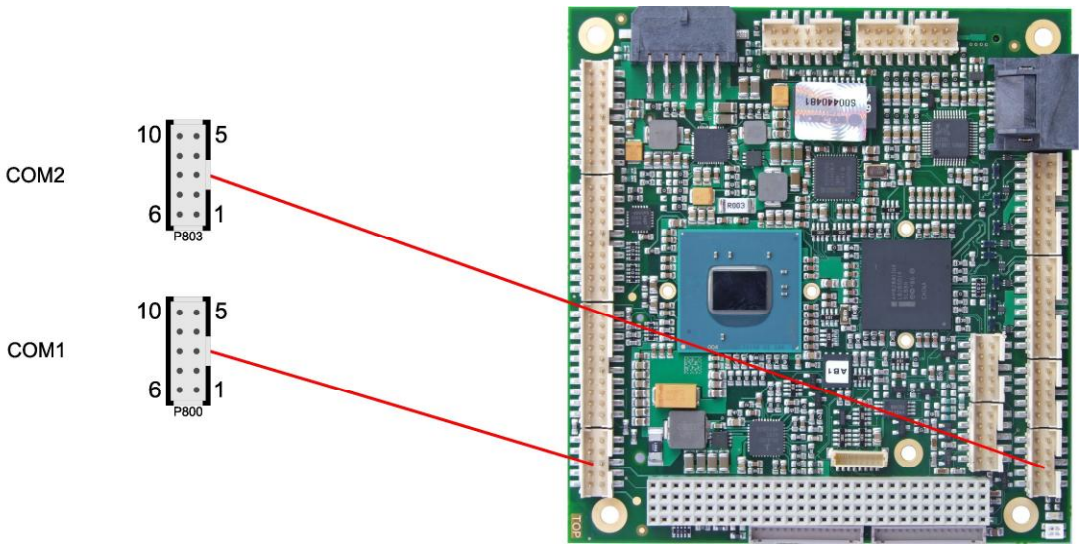


Pinout SATA:

Pin	Name	Description
1	GND	ground
2	SATATX	SATA transmit +
3	SATATX#	SATA transmit -
4	GND	ground
5	SATARX	SATA receive +
6	SATARX#	SATA receive -
7	GND	ground

3.14 COM1 and COM2

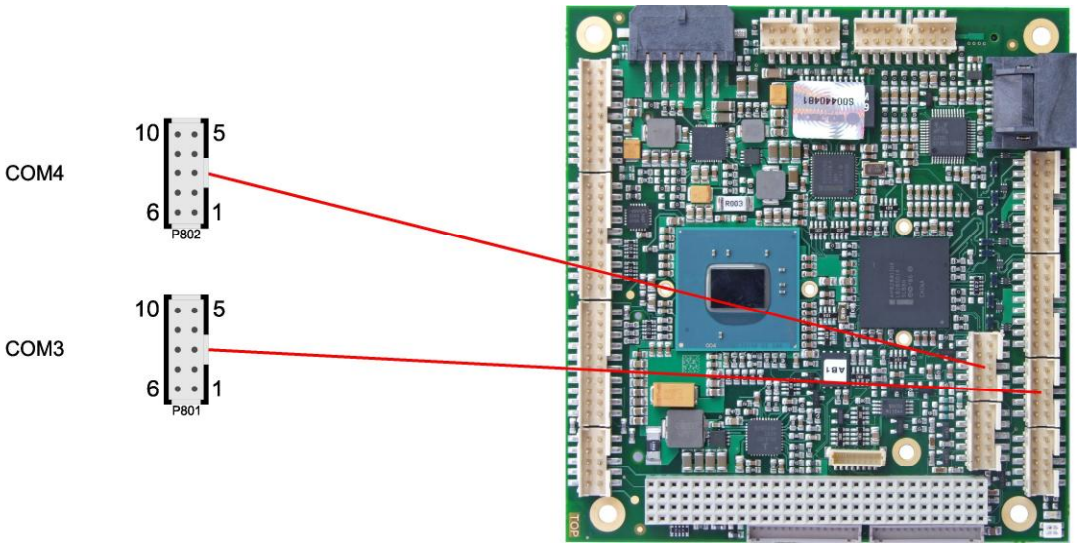
The serial interfaces COM1 and COM2 are provided via a 2x5pin connector (FCI 98424-G52-10LF, mating connector e.g. FCI 90311-010LF).



Description	Name	Pin		Name	Description
data carrier detect	DCD	1	6	DSR	data set ready
receive data	RXD	2	7	RTS	request to send
transmit data	TXD	3	8	CTS	clear to send
data terminal ready	DTR	4	9	RI	ring indicator
ground	GND	5	10	VCC	5 volt supply

3.15 COM3 and COM4

The serial interfaces COM3 and COM4 are provided via a 2x5pin connector (FCI 98424-G52-10LF, mating connector e.g. FCI 90311-010LF). For these two interfaces, both RS232 and RS485 protocols are available. This can be configured in BIOS setup.



Description	Name	Pin		Name	Description
data carrier detect	DCD	1	6	DSR	data set ready
receive data	RXD	2	7	RTS	request to send
transmit data	TXD	3	8	CTS	clear to send
data terminal ready	DTR	4	9	RI	ring indicator
ground	GND	5	10	VCC	5 volt supply

Pinout in RS422/485 mode:

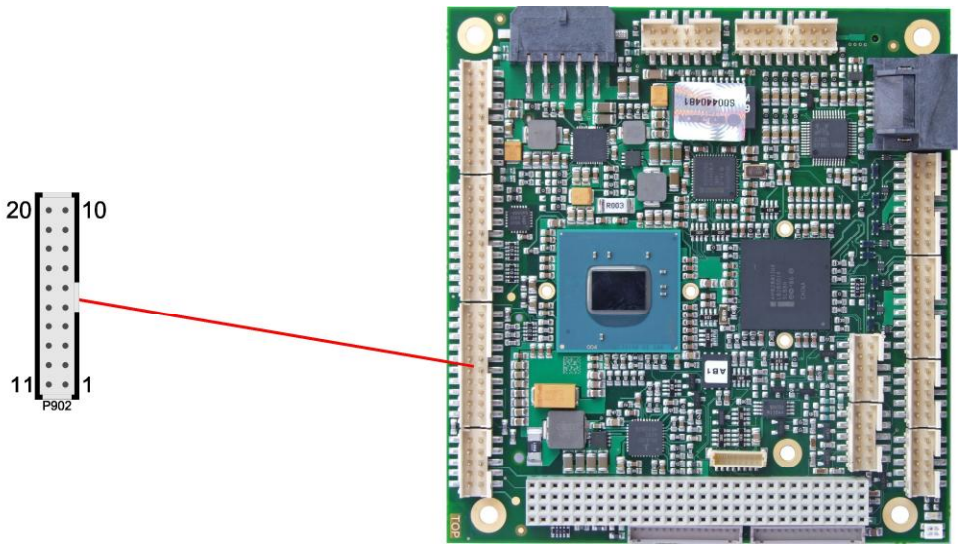
Description	Name	Pin		Name	Description
transmit data +	TX	1	6	TX#	transmit data -
receive data +	RX	2	7	RX#	receive data -
reserved	N/C	3	8	N/C	reserved
reserved	N/C	4	9	N/C	reserved
ground	GND	5	10	VCC	5 volt supply

NOTE

Proper use of RS485 requires that the signal RTS (Request To Send) be toggled on an off in order to turn on and off the transmit function. It is the responsibility of the software application to assert control over the RTS line.

3.16 Parallel Interface LPT

The parallel interface is a 2x10pin connector (FCI 98424-G52-20LF, mating connector e.g. FCI 90311-020LF). The port address and the interrupt are set via the BIOS setup.

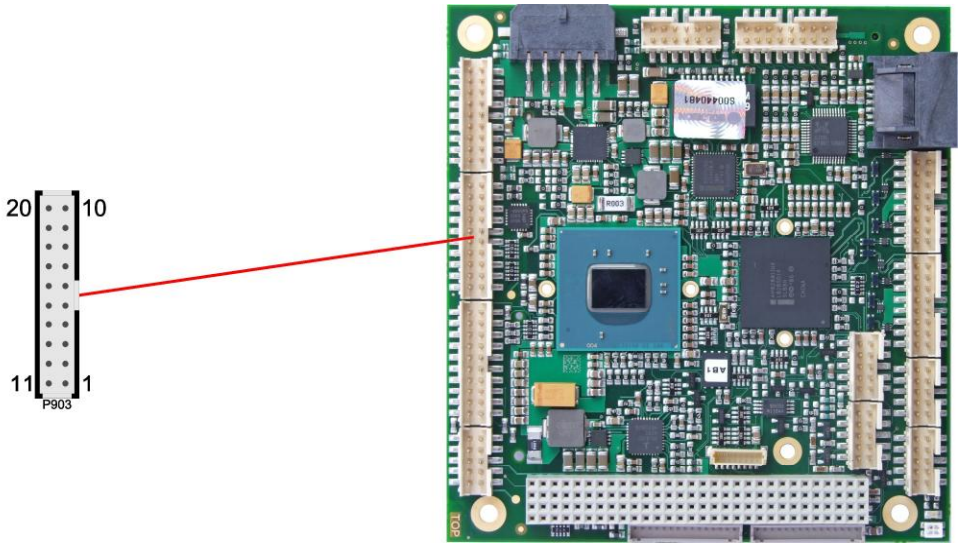


Pinout LPT:

Description	Name	Pin		Name	Description
strobe	STB#	1	11	AFD#	automatic line feed
LPT data 0	PD0	2	12	ERR#	error
LPT data 1	PD1	3	13	INIT#	init
LPT data 2	PD2	4	14	SLIN#	select input
LPT data 3	PD3	5	15	SLCT	select printer
LPT data 4	PD4	6	16	PE	paper end
LPT data 5	PD5	7	17	BUSY	busy
LPT data 6	PD6	8	18	ACK#	acknowledge
LPT data 7	PD7	9	19	GND	ground
5 volt supply	VCC	10	20	GND	ground

3.17 GPIO

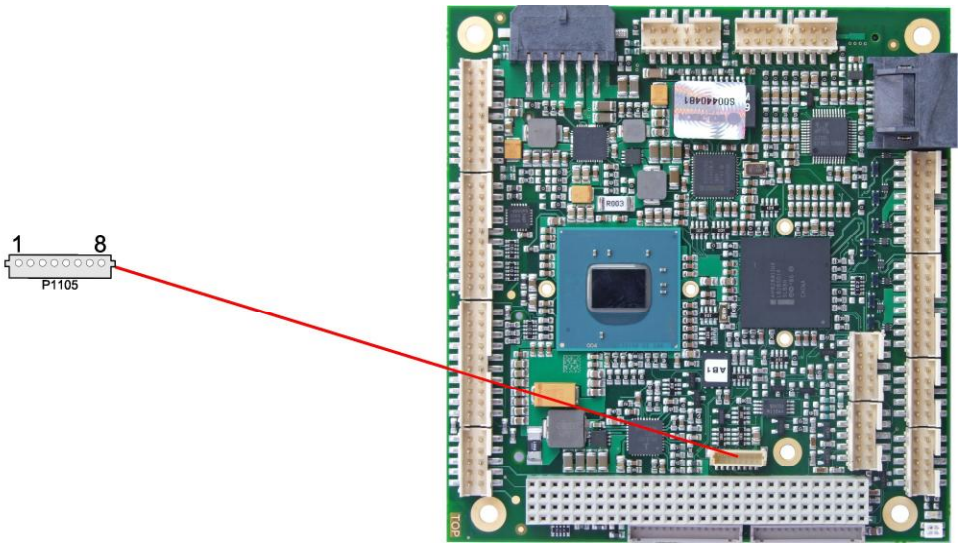
The General Purpose Input/Output interface is made available through a 2x10 pin connector (FCI 98424-G52-20LF, mating connector e.g. FCI 90311-020LF). To make use of this interface the SIO unit must be programmed accordingly. Please refer to your sales representative for information on available software support.



Description	Name	Pin		Name	Description
ground	GND	1	11	3.3V	3.3 volt supply
GP input/output 00	GPIO00	2	12	GPIO10	GP input/output 10
GP input/output 01	GPIO01	3	13	GPIO11	GP input/output 11
GP input/output 02	GPIO02	4	14	GPIO12	GP input/output 12
GP input/output 03	GPIO03	5	15	GPIO13	GP input/output 13
GP input/output 04	GPIO04	6	16	GPIO14	GP input/output 14
GP input/output 05	GPIO05	7	17	GPIO15	GP input/output 15
GP input/output 06	GPIO06	8	18	GPIO16	GP input/output 16
GP input/output 07	GPIO07	9	19	GPIO17	GP input/output 17
3.3 volt supply	3.3V	10	20	GND	ground

3.18 Monitoring Functions

Additional monitoring functions, such as the status of the fan or of other devices connected over SM-Bus (e. g. temperature sensor), are accessible via an 8 pin connector (JST BM08B-SRSS-TB, mating connector: SHR-08V-S(-B)).

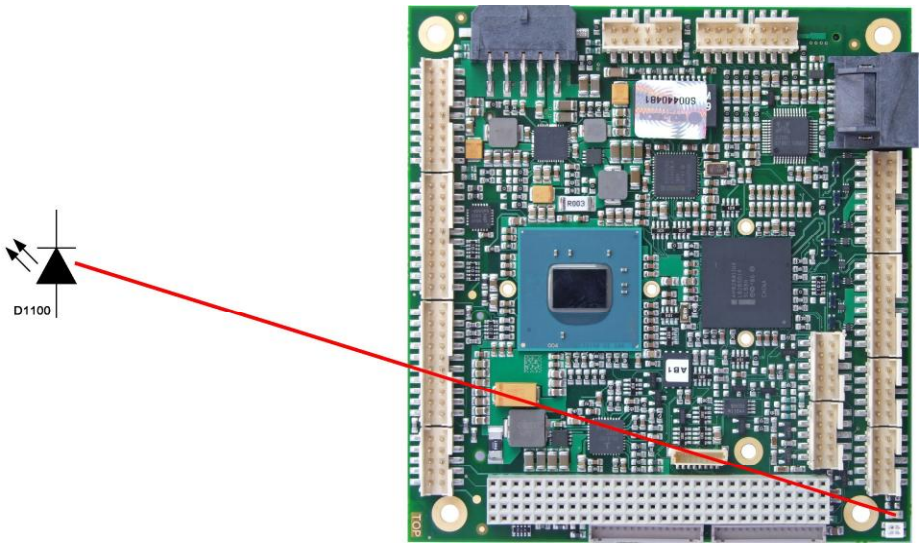


Pin	Name	Description
1	3.3V	3.3 volt supply
2	CS-SMB-CLK	SMBus clock
3	CS-SMB-DAT	SMBus data
4	GND	ground
5	FANON1	5 volt supply (switched)
6	FANCTRL1	fan 1 monitoring signal
7	VCC	5 volt supply
8	FANCTRL3	fan 3 monitoring signal

4 Status LEDs

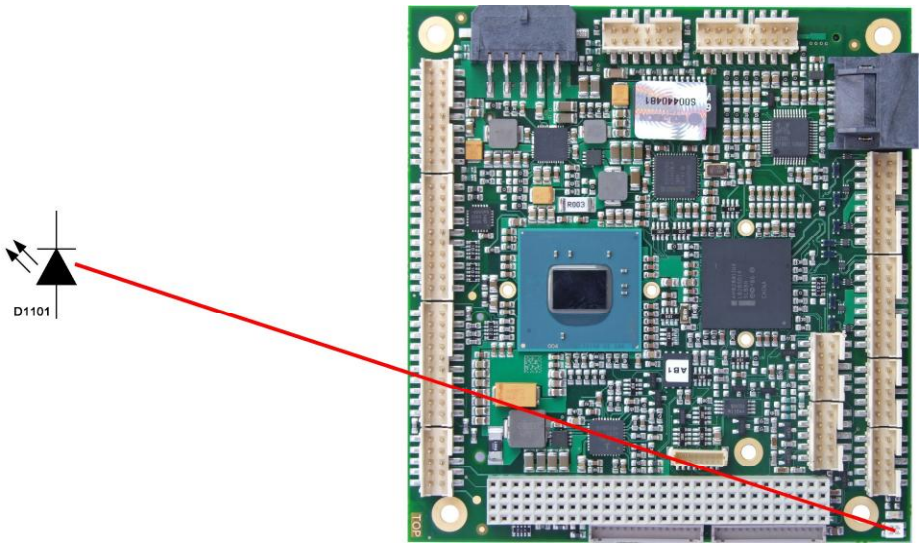
4.1 HD LED

Harddisk activity is signalled by a dedicated LED.



4.2 RGB LED

The ADLD25PC has an RGB LED, which can signal status messages by using different colors and flash intervals.



Status Codes RGB LED:

Color	Interval	Meaning
none	solid	Invalid system state
White	solid	The microcontroller has just been flashed and is being prepared for normal operation after reboot
Cyan	solid	Reserved
Magenta	solid	Reserved
Blue	solid	Reserved
Yellow	solid	Reserved
Green	solid	Board operates normal
Red	solid	Board is in Reset
Green/Yellow	flashing	Bootloader operates normal
Red	flashing	Firmware is being started (start sequence still running)
Red/Yellow	flashing	Bootloader is being started (start sequence still running)
Red/Magenta	flashing	Checksum error during I2C transmission in bootloader
Red/Blue	flashing	Update completed, waiting for manual Reset
Yellow	flashing (10s)	S5 state
Yellow	flashing (6s)	S4 state
Yellow	flashing (3s)	Reserved
Yellow	flashing (0.5s)	Reserved

NOTE

If the board appears to be in Reset (Red LED lit) then this could also indicate a PCI104-Express "stacking error". Such an error could occur when the stack contains a peripheral card which has the wrong type of connector (PCI104-Express Type 1 instead of Type 2 or vice versa).

5 BIOS Settings

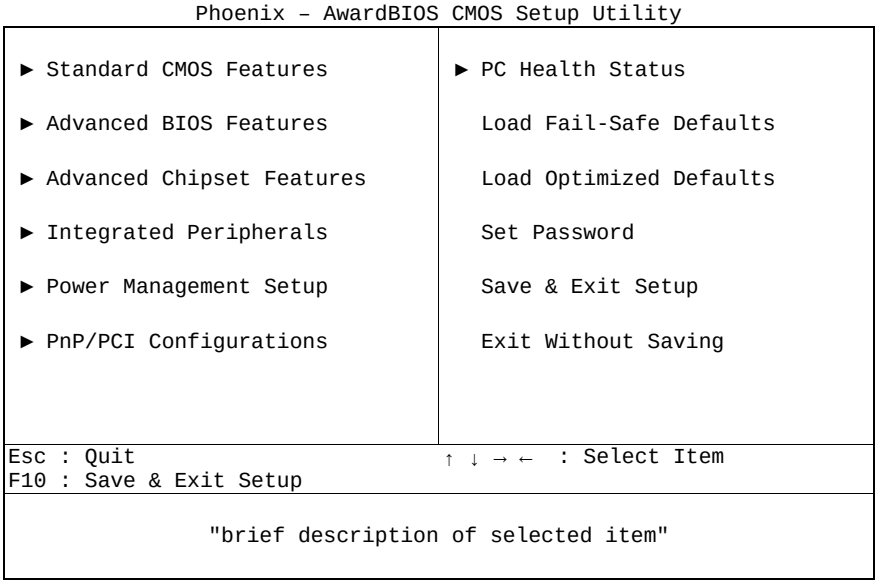
5.1 Remarks for Setup Use

In a setup page, standard values for its setup entries can be loaded. Fail-safe defaults are loaded with F6 and optimized defaults are loaded with F7. These standard values are independent of the fact that a board has successfully booted with a setup setting before.
This is different if these defaults are called from the Top Menu. Once a setup setting was saved, which subsequently leads to a successful boot process, those values are loaded as default for all setup items afterwards.
See also the chapters “Load Fail-Safe Defaults" (5.10) and “Load Optimized Defaults” (5.11).

NOTE

BIOS features and setup options are subject to change without notice. The settings displayed in the screenshots on the following pages are meant to be examples only. They do not represent the recommended settings or the default settings. Determination of the appropriate settings is dependent upon the particular application scenario in which the board is used.

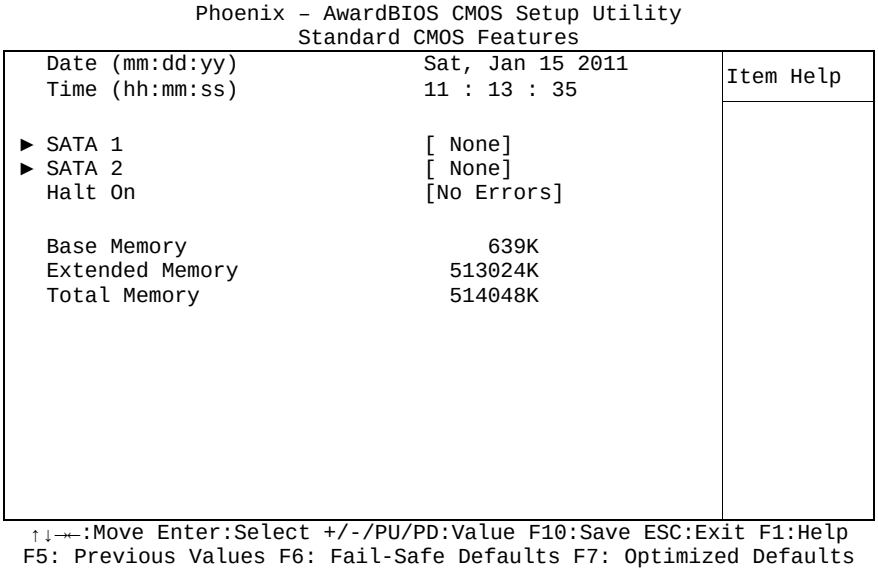
5.2 Top Level Menu



The sign „►“ in front of an item means that there is a sub menu.
The „x“ sign in front of an item means, that the item is disabled but can be enabled by changing or selecting some other item (usually somewhere above the disabled item on the same screen).

Use the arrow buttons to navigate from one item to another. For selecting an item press Enter which will open either a sub menu or a dialog screen.

5.3 Standard CMOS Features



- **Date (mm:dd:yy)**
  Options: mm: month
  dd: day
  yy: year

- **Time (hh:mm:ss)**
  Options: hh: hours
  mm: minutes
  ss: seconds

- **SATA 1**
  Sub menu: see "SATA channels" (p. 41)

- **SATA 2**
  Sub menu: see "SATA channels" (p. 41)

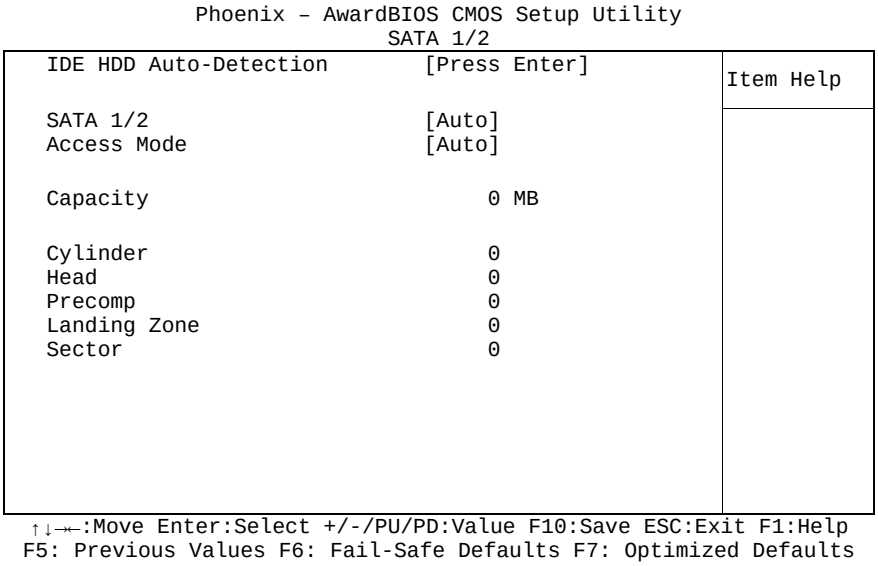
- **Halt On**
  Options: All Errors / No Errors / All, But Keyboard

- **Base Memory**
  Options: none

- **Extended Memory**
  Options: none

- **Total Memory**
  Options: none

5.3.1 SATA channels



- **IDE HDD Auto-Detection**
  Options: none

- **SATA 1/2**
  Options: None / Auto / Manual

- **Access Mode**
  Options: CHS / LBA / Large / Auto

5.4 Advanced BIOS Features

```
                Phoenix – AwardBIOS CMOS Setup Utility
                      Advanced BIOS Features
┌──────────────────────────────────────────────────────┬──────────────┐
│ ► CPU Feature                  [Press Enter]         │ Item Help    │
│ ► Hard Disk Boot Priority      [Press Enter]         │              │
│   CPU L3 Cache                 [Enabled]             │              │
│   Hyper-Threading Technology   [Enabled]             │              │
│   Quick Power On Self Test     [Enabled]             │              │
│   First Boot Device            [USB-FDD]             │              │
│   Second Boot Device           [USB-CDROM]           │              │
│   Third Boot Device            [Hard Disk]           │              │
│   Boot Other Device            [Enabled]             │              │
│   Boot Up NumLock Status       [On]                  │              │
│   Gate A20 Option              [Fast]                │              │
│   Typematic Rate Setting       [Disabled]            │              │
│ x Typematic Rate (Chars/Sec)    6                    │              │
│ x Typematic Delay (Msec)        250                  │              │
│   Security Option              [Setup]               │              │
│ x APIC Mode                     Enabled              │              │
│   MPS Version Control For OS   [1.4]                 │              │
│   OS Select For DRAM > 64MB    [Non-OS2]             │              │
│   Report No FDD For WIN 95     [No]                  │              │
│   Full Screen LOGO Show        [Disabled]            │              │
└──────────────────────────────────────────────────────┴──────────────┘
  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **CPU Feature**
  Sub menu: see "CPU Feature" (p. 44)

- **Hard Disk Boot Priority**
  Sub menu: see "Hard Disk Boot Priority" (p. 45)

- **CPU L3 Cache**
  Options: Enabled / Disabled

- **Hyper-Threading Technology**
  Options: Enabled / Disabled

- **Quick Power On Self Test**
  Options: Enabled / Disabled

- **First Boot Device**
  Options: LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / Legacy LAN / Onboard LAN 00C8 / Disabled

- **Second Boot Device**
  Options: LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / Legacy LAN / Onboard LAN 00C8 / Disabled

- **Third Boot Device**
  Options: LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / Legacy LAN / Onboard LAN 00C8 / Disabled

- **Boot Other Device**
  Options: Enabled / Disabled

- **Boot Up NumLock Status**
  Options: Off / On

- **Gate A20 Option**
  Options: Normal / Fast

- **Typematic Rate Setting**
  Options: Enabled / Disabled

- **Typematic Rate (Chars/Sec)**
  Options: 6 / 8 / 10 / 12 / 15 / 20 / 24 / 30

- **Typematic Delay (Msec)**
  Options: 250 / 500 / 750 / 1000

- **Security Option**
  Options: Setup / System

- **APIC Mode**
  Options: none

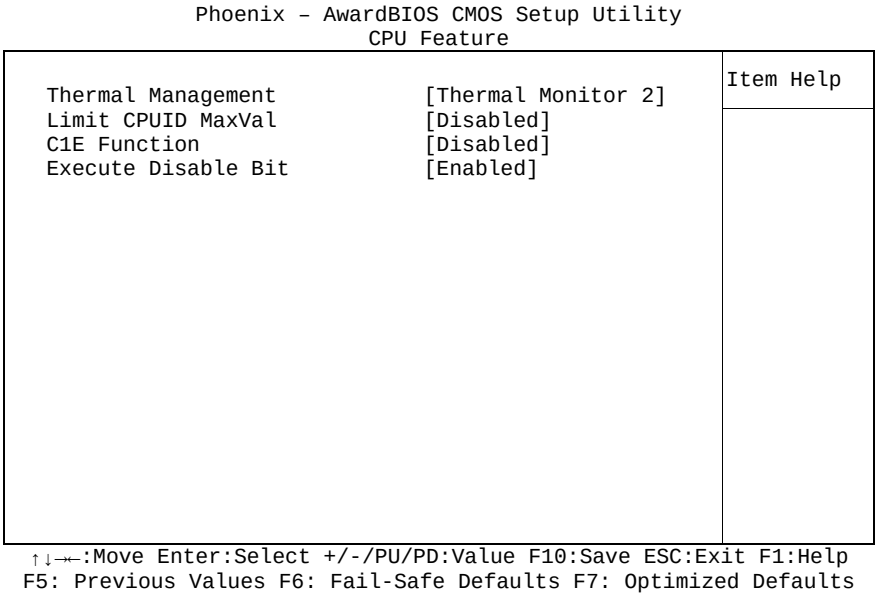
- **MPS Version Control For OS**
  Options: 1.1 / 1.4

- **OS Select For DRAM > 64MB**
  Options: Non-OS2 / OS2

- **Report No FDD For WIN 95**
  Options: No / Yes

- **Full Screen LOGO Show**
  Options: Enabled / Disabled

5.4.1 CPU Feature



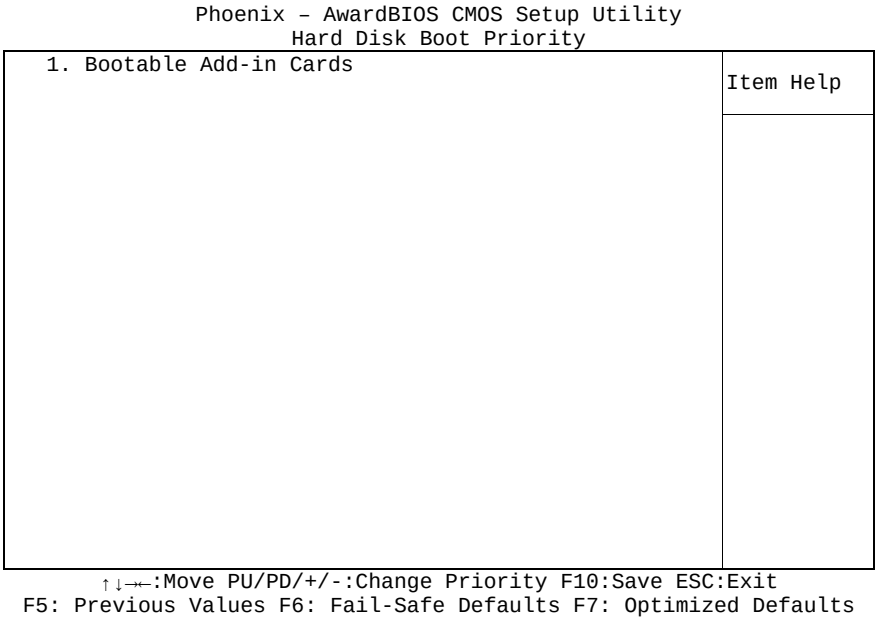
- **Thermal Management**
  Options: Thermal Monitor 1 / Thermal Monitor 2 / Disabled / TM1 + TM2 enabled

- **Limit CPUID MaxVal**
  Options: Enabled / Disabled

- **C1E Function**
  Options: Auto / Disabled

- **Execute Disable Bit**
  Options: Enabled / Disabled

5.4.2 Hard Disk Boot Priority



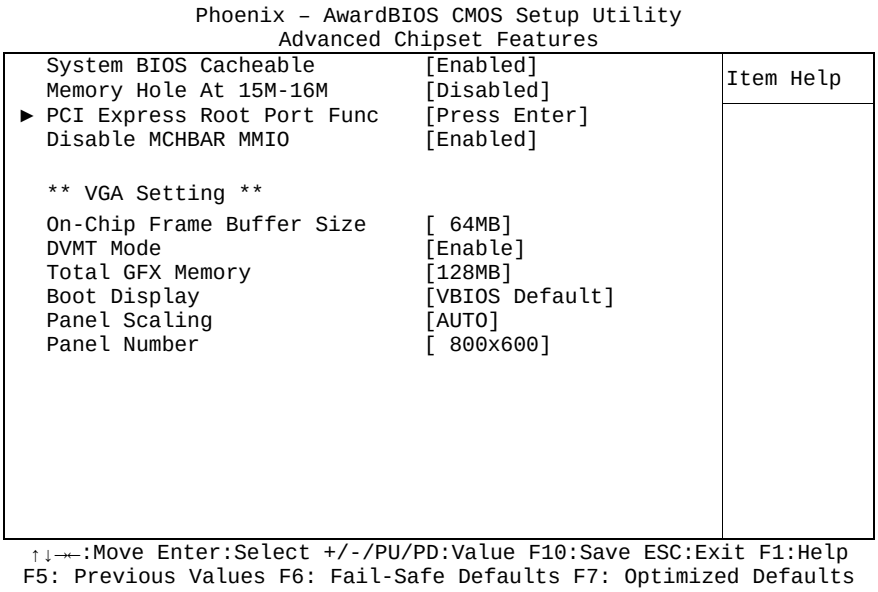
ü [list of available devices]

Options: this dialog allows you to set the order in which the available bootable devices shall be accessed for an attempt to boot.

ü Attention!

in this sub menu the buttons <Page Up>, <Page Down>, <+> and <-> have a different function than in the rest of the setup: They serve to move the items of the list up or down.

5.5 Advanced Chipset Features



- **System BIOS Cacheable**
  Options: Enabled / Disabled

- **Memory Hole At 15M-16M**
  Options: Enabled / Disabled

- **PCI Express Root Port Func**
  Sub menu: see "PCI Express Root Port Function" (p. 47)

- **Disable MCHBAR MMIO**
  Options: Enabled / Disabled

- **On-Chip Frame Buffer Size**
  Options: 1MB / 8MB

- **DVMT Mode**
  Options: Disable / Enable

- **Total GFX Memory**
  Options: 128MB / 256MB / MAX.

- **Boot Display**
  Options: Auto / CRT / LFP

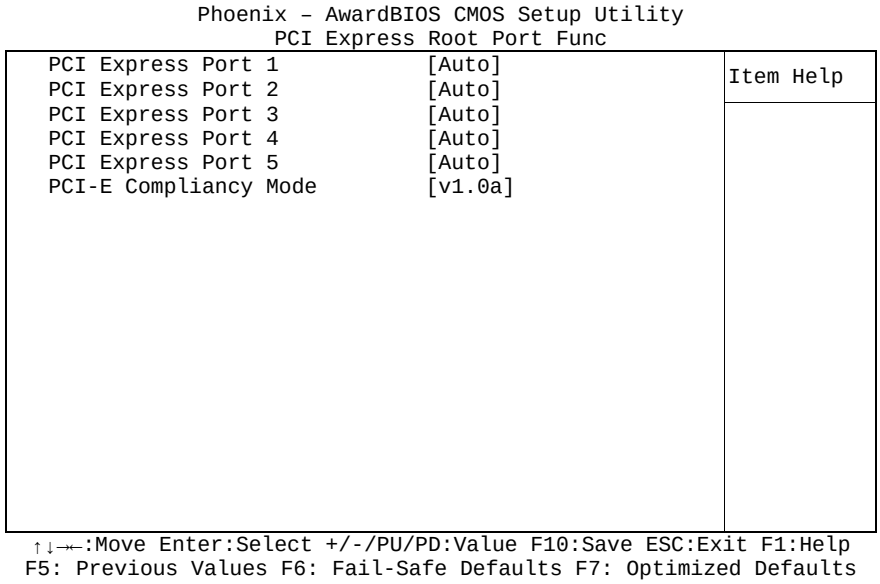
- **Panel Scaling**
  Options: Auto / On / Off

- **Panel Number**
  Options: 640x480 / 800x600 / 1024x768 / 1280x768 / 1024x768 / 1280x800 / 1280x600

NOTE

For "Panel Number", some values might occur multiple times in the list. This means that the video signal is available in slightly different configurations, offering the possibility to choose the one which works best with the target display.

5.5.1 PCI Express Root Port Function



- **PCI Express Port 1**
  Options: Auto / Enabled / Disabled

- **PCI Express Port 2**
  Options: Auto / Enabled / Disabled

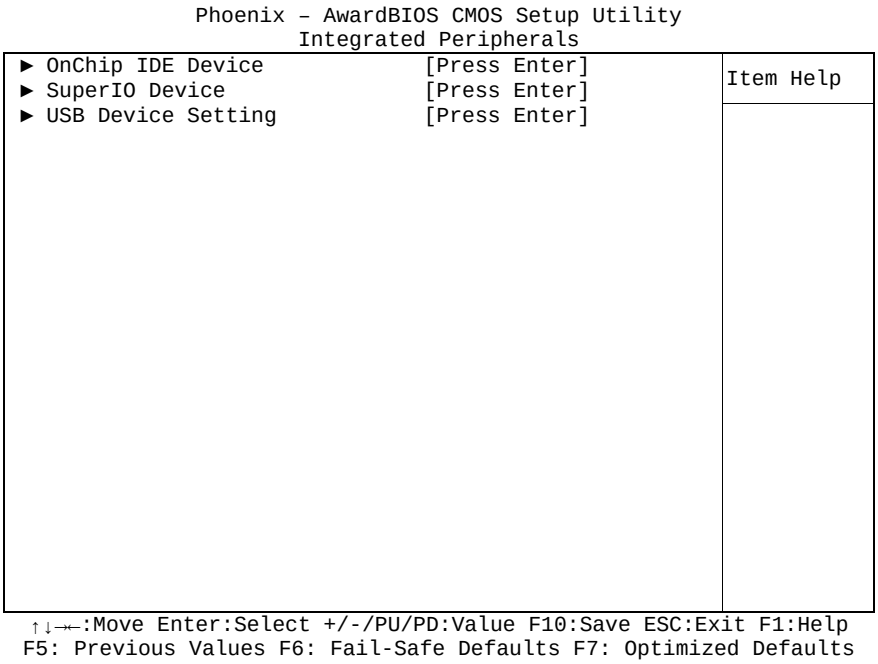
- **PCI Express Port 3**
  Options: Auto / Enabled / Disabled

- **PCI Express Port 4**
  Options: Auto / Enabled / Disabled

- **PCI Express Port 5**
  Options: Auto / Enabled / Disabled

- **PCI-E Compliancy Mode**
  Options: v1.0a / v1.0

5.6 Integrated Peripherals

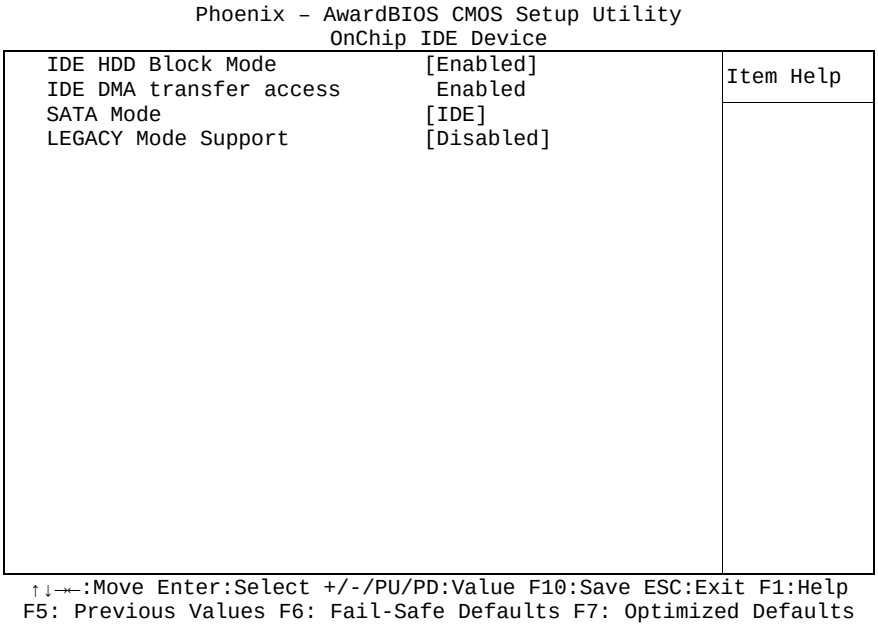


- **OnChip IDE Device**
  Sub menu: see "OnChip IDE Devices" (p. 49)

- **SuperIO Device**
  Sub menu: see "SuperIO Devices" (p. 50)

- **USB Device Setting**
  Sub menu: see "USB Device Setting" (p. 51)

5.6.1 OnChip IDE Devices



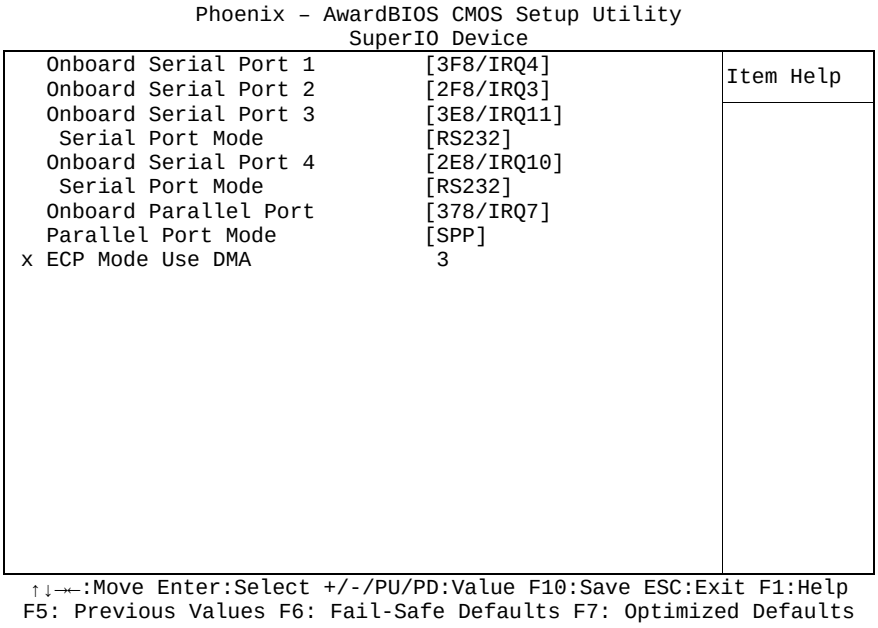
- **IDE HDD Block Mode**
  Options: Enabled / Disabled

- **IDE DMA transfer access**
  Options: none

- **SATA Mode**
  Options: IDE / RAID / AHCI

- **LEGACY Mode Support**
  Options: Enabled / Disabled

5.6.2 SuperIO Devices



- **Onboard Serial Port 1**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3

- **Onboard Serial Port 2**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3

- **Onboard Serial Port 3**
  Options: Disabled / 3F8/IRQ11 / 2F8/IRQ11 / 3E8/IRQ11 / 2E8/IRQ11

- **Serial Port Mode**
  Options: RS232 / RS485

- **Onboard Serial Port 4**
  Options: Disabled / 3F8/IRQ10 / 2F8/IRQ10 / 3E8/IRQ10 / 2E8/IRQ10

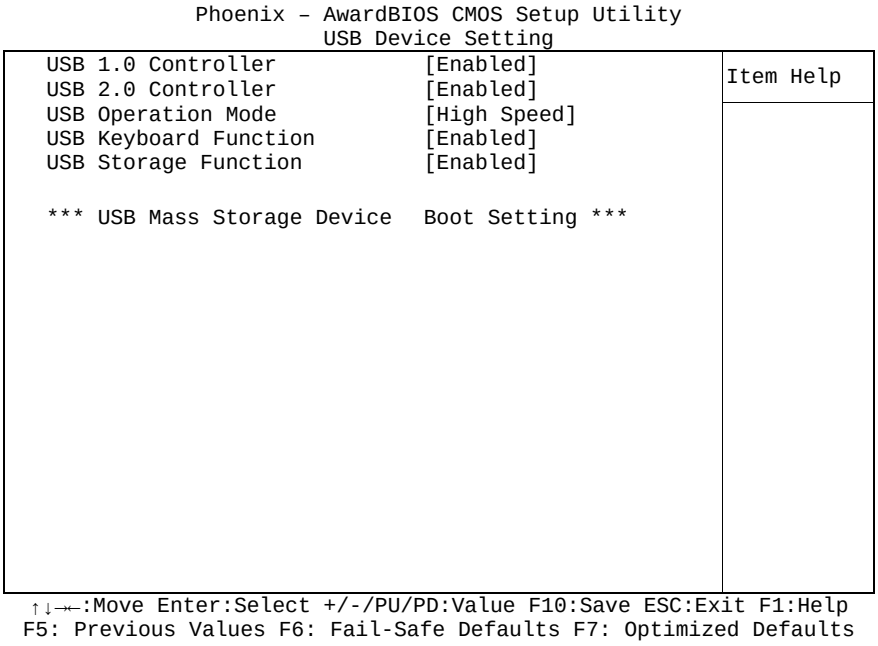
- **Serial Port Mode**
  Options: RS232 / RS485

- **Onboard Parallel Port**
  Options: Disabled / 378/IRQ7 / 278/IRQ5 / 3BC/IRQ7

- **Parallel Port Mode**
  Options: SPP / EPP1.9 + SPP / ECP / EPP1.9 + ECP / PRINTER / EPP1.7 + SPP / EPP1.7 + ECP

- **ECP Mode Use DMA**
  Options: 1 / 3

5.6.3 USB Device Setting



- **USB 1.0 Controller**
  Options: Enabled / Disabled

- **USB 2.0 Controller**
  Options: Enabled / Disabled

- **USB Operation Mode**
  Options: Full/Low Speed / High Speed

- **USB Keyboard Function**
  Options: Enabled / Disabled

- **USB Storage Function**
  Options: Enabled / Disabled

5.7 Power Management Setup

```
                Phoenix – AwardBIOS CMOS Setup Utility
                      Power Management Setup
  Power-Supply Type             [AT]                    | Item Help
  ACPI Function                 [Enabled]               |
  ACPI Suspend Type             [S1(POS)]               |
  Run VGABIOS if S3 Resume       Auto                   |
  Power Management              [User Define]           |
  Video Off Method              [DPMS]                  |
  Video Off in Suspend          [Yes]                   |
  Suspend Type                  [Stop Grant]            |
  Modem Use IRQ                 [3]                     |
  Suspend Mode                  [Disabled]              |
  HDD Power Down                [Disabled]              |
  Soft-Off by PWR-BTTN          [Instant-Off]           |
  PWRON After PWR-Fail          [On]                    |
  Wake-Up by PCI card           [Disabled]              |
  Power On by Ring              [Disabled]              |
x USB KB Wake-Up From S3        Disabled                |
  Resume by Alarm               [Disabled]              |
x  Date(of Month) Alarm          0                      |
x  Time(hh:mm:ss)                0 : 0 : 0              |
                                                        |
  ** Reload Global Timer        Events **               |
  Primary IDE 0                 [Disabled]              |
  Primary IDE 1                 [Disabled]              |
  Secondary IDE 0               [Disabled]              |
  Secondary IDE 1               [Disabled]              |
  FDD,COM,LPT Port              [Disabled]              |
  PCI PIRQ[A-D]#                [Disabled]              |
  HPET Support                  [Enabled]               |
  HPET Mode                     [32-bit mode]           |
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- **Power Supply Type**
  Options: AT / ATX

- **ACPI function**
  Options: Enabled / Disabled

- **ACPI Suspend Type**
  Options: S1(POS) / S3(STR) / S1&S3

- **Run VGABIOS if S3 Resume**
  Options: Auto / Yes / No

- **Power Management**
  Options: User Define / Min Saving / Max Saving

- **Video Off Method**
  Options: Blank Screen / V/H SYNC+Blank / DPMS

- **Video Off In Suspend**
  Options: No / Yes

- **Suspend Type**
  Options: Stop Grant / PwrOn Suspend

- **MODEM Use IRQ**
  Options: NA / 3 / 4 / 5 / 7 / 9 / 10 / 11

- **Suspend Mode**
  Options: Disabled / 1 Min / 2 Min / 4 Min / 8 Min / 12 Min / 20 Min / 30 Min / 40 Min / 1 Hour

- **HDD Power Down**
  Options: Disabled / 1 Min ... 15 Min

- **Soft-Off by PWR-BTTN**
  Options: Instant-Off / Delay 4 Sec

- **PWRON After PWR-Fail**
  Options: Former Sts / On / Off

- **Wake Up by PCI Card**
  Options: Enabled / Disabled

- **Power-On by Ring**
  Options: Enabled / Disabled

- **USB KB Wake Up From S3**
  Options: Enabled / Disabled

- **Resume by Alarm**
  Options: Enabled / Disabled

- **Date(of Month) Alarm**
  Options: 1 / ... / 31

- **Time (hh:mm:ss) Alarm**
  Options: insert [hh], [mm] and [ss]

- **Primary IDE 0**
  Options: Enabled / Disabled

- **Primary IDE 1**
  Options: Enabled / Disabled

- **Secondary IDE 0**
  Options: Enabled / Disabled

- **Secondary IDE 1**
  Options: Enabled / Disabled

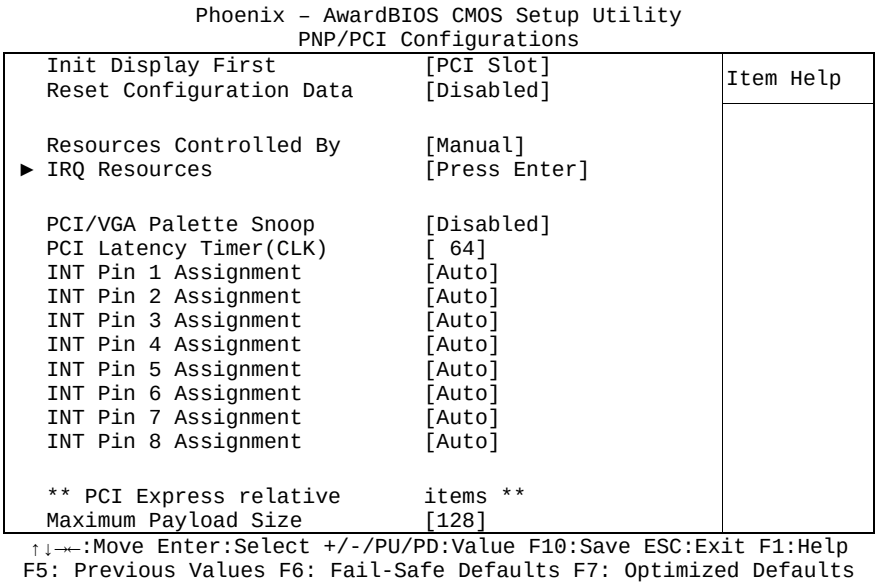
- **FDD,COM,LPT Port**
  Options: Enabled / Disabled

- **PCI PIRQ[A-D]#**
  Options: Enabled / Disabled

- **HPET Support**
  Options: Enabled / Disabled

- **HPET Mode**
  Options: 32-bit mode / 64-bit mode

5.8 PnP/PCI Configuration



- **Init Display First**
  Options: PCI Slot / Onboard / PCIEx

- **Reset Configuration Data**
  Options: Enabled / Disabled

- **Resources Controlled By**
  Options: Auto(ESCD) / Manual

- **IRQ Resources**
  Sub menu: see "IRQ Resources" (p. 56)

- **PCI/VGA Palette Snoop**
  Options: Enabled / Disabled

- **PCI Latency Timer(CLK)**
  Options: 0...255

- **INT Pin 1 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 2 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 3 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 4 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 5 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

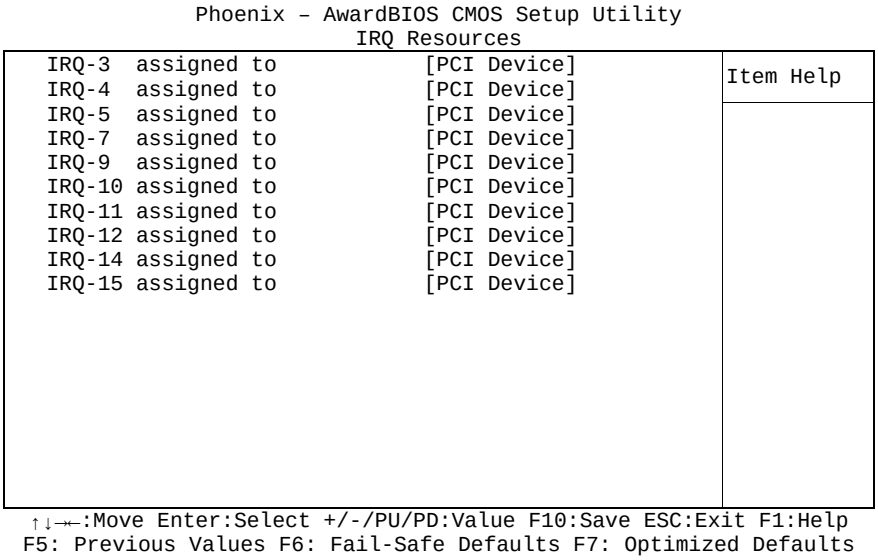
- **INT Pin 6 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 7 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **INT Pin 8 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- **Maximum Payload Size**
  Options: none

5.8.1 IRQ Resources



- **IRQ-3 assigned to**
  Options: PCI Device / Reserved

- **IRQ-4 assigned to**
  Options: PCI Device / Reserved

- **IRQ-5 assigned to**
  Options: PCI Device / Reserved

- **IRQ-7 assigned to**
  Options: PCI Device / Reserved

- **IRQ-9 assigned to**
  Options: PCI Device / Reserved

- **IRQ-10 assigned to**
  Options: PCI Device / Reserved

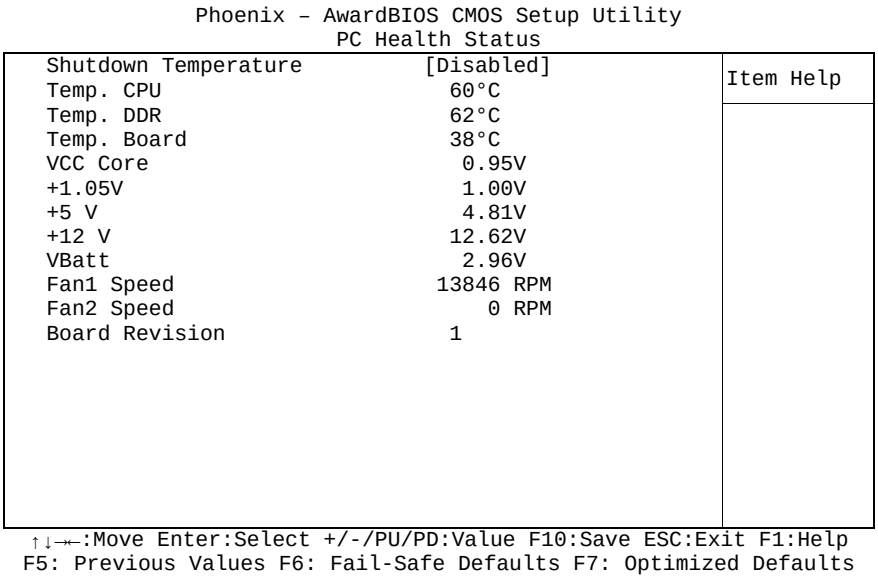
- **IRQ-11 assigned to**
  Options: PCI Device / Reserved

- **IRQ-12 assigned to**
  Options: PCI Device / Reserved

- **IRQ-14 assigned to**
  Options: PCI Device / Reserved

- **IRQ-15 assigned to**
  Options: PCI Device / Reserved

5.9 PC Health Status



- **Shutdown Temperature**
  Options: 60°C/140°F / 65°C/149°F / 70°C/158°C / Disabled

- **Temp. CPU**
  Options: none

- **Temp. DDR**
  Options: none

- **Temp. Board**
  Options: none

- **VCC Core**
  Options: none

- **+1.05 V**
  Options: none

- **+5 V**
  Options: none

- **+12 V**
  Options: none

- **Fan1 Speed**
  Options: none

- **Fan2 Speed**
  Options: none

- **Board Revision**
  Options: none

5.10 Load Fail-Safe Defaults

If this option is chosen, the last working setup is loaded from flash. Working means that the setup setting has already led to a successful boot process.
At the first setting of the BIOS setup, safe values are loaded which lets the board boot. This status is reached again, if the board is reprogrammed with the corresponding flash-program and the required parameters.

5.11 Load Optimized Defaults

This option applies like described under “Remarks for Setup Use” (5.1).
At first start of the BIOS, optimized values are loaded from the setup, which are supposed to make the board boot. This status is achieved again, if the board is reprogrammed using the flash program with the required parameters.

5.12 Set Password

Here you can enter a password to protect the BIOS settings against unauthorized changes. Use this option with care! Forgotten or lost passwords are a frequent problem.

5.13 Save & Exit Setup

Settings are saved and the board is restarted.

5.14 Exit Without Saving

This option leaves the setup without saving any changes.

6 BIOS update

If a BIOS update becomes necessary, the program “AWDFLASH.EXE” from Phoenix Technologies is used for this. It is important, that the program is started from a DOS environment without a virtual memory manager such as for example “EMM386.EXE”. In case such a memory manager is loaded, the program will stop with an error message.
The system must not be interrupted during the flash process, otherwise the update is stopped and the BIOS is destroyed afterwards.
The program should be started as follows:

```
awdflash [biosfilename] /sn /cc /cp
```

/sn	Do not save the current BIOS
/cc	Clear the CMOS
/cp	Clear the PnP information

The erasure of CMOS and PnP is strongly recommended. This ensures, that the new BIOS works correctly and that all chipset registers, which were saved in the setup, are reinitialized through the BIOS. DMI should only be erased (option /cd) if the BIOS supplier advises to do so.
A complete description of all valid parameters is shown with the parameter “/?”.
In order to make the updating process run automatically, the parameter “/py” must be added. This parameter bypasses all security checks during programming.

CAUTION

Updating the BIOS in an improper way can render the board unusable. Therefore, you should only update the BIOS if you really need the changes/corrections which come with the new BIOS version.

CAUTION

Before you proceed to update the BIOS you need to make absolutely sure that you have the right BIOS file which was issued for the exact board and exact board revision that you wish to update. If you try to update the BIOS using the wrong file the board will not start up again.

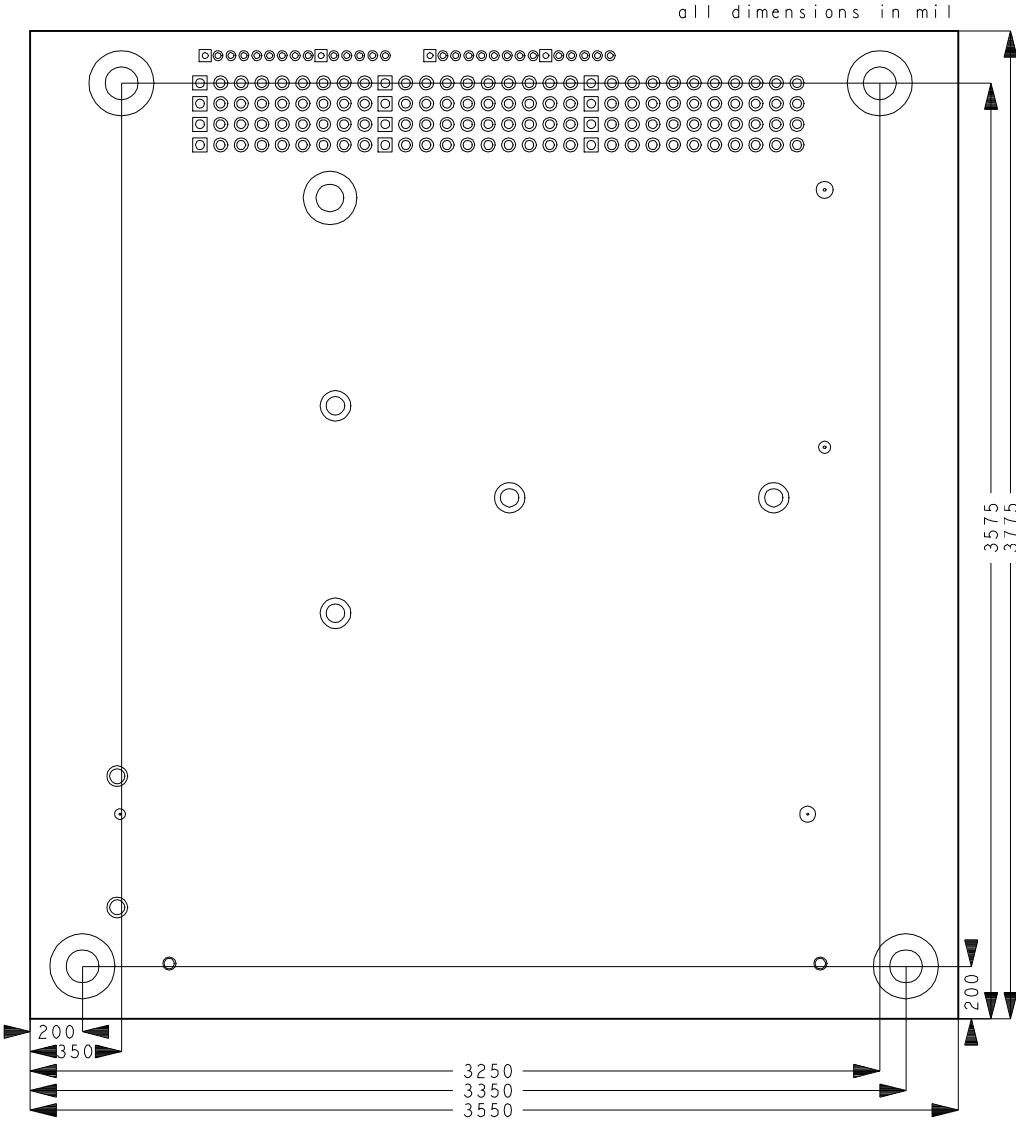
7 Mechanical Drawing

7.1 PCB: Mounting Holes

A true dimensioned drawing can be found in the PC/104 specification.

NOTE

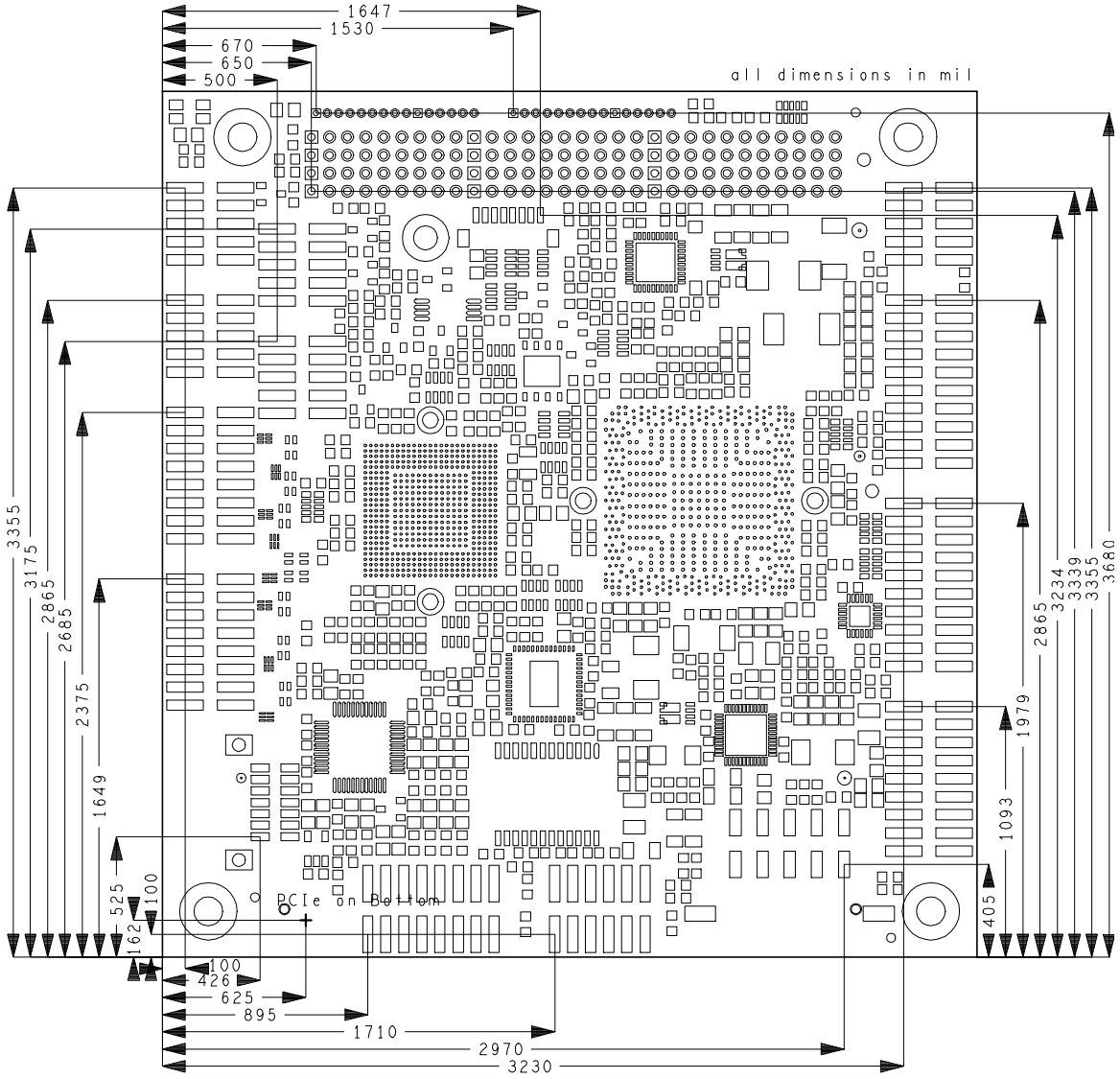
All dimensions are in mil (1 mil = 0,0254 mm)



7.2 PCB: Pin 1 Dimensions

NOTE

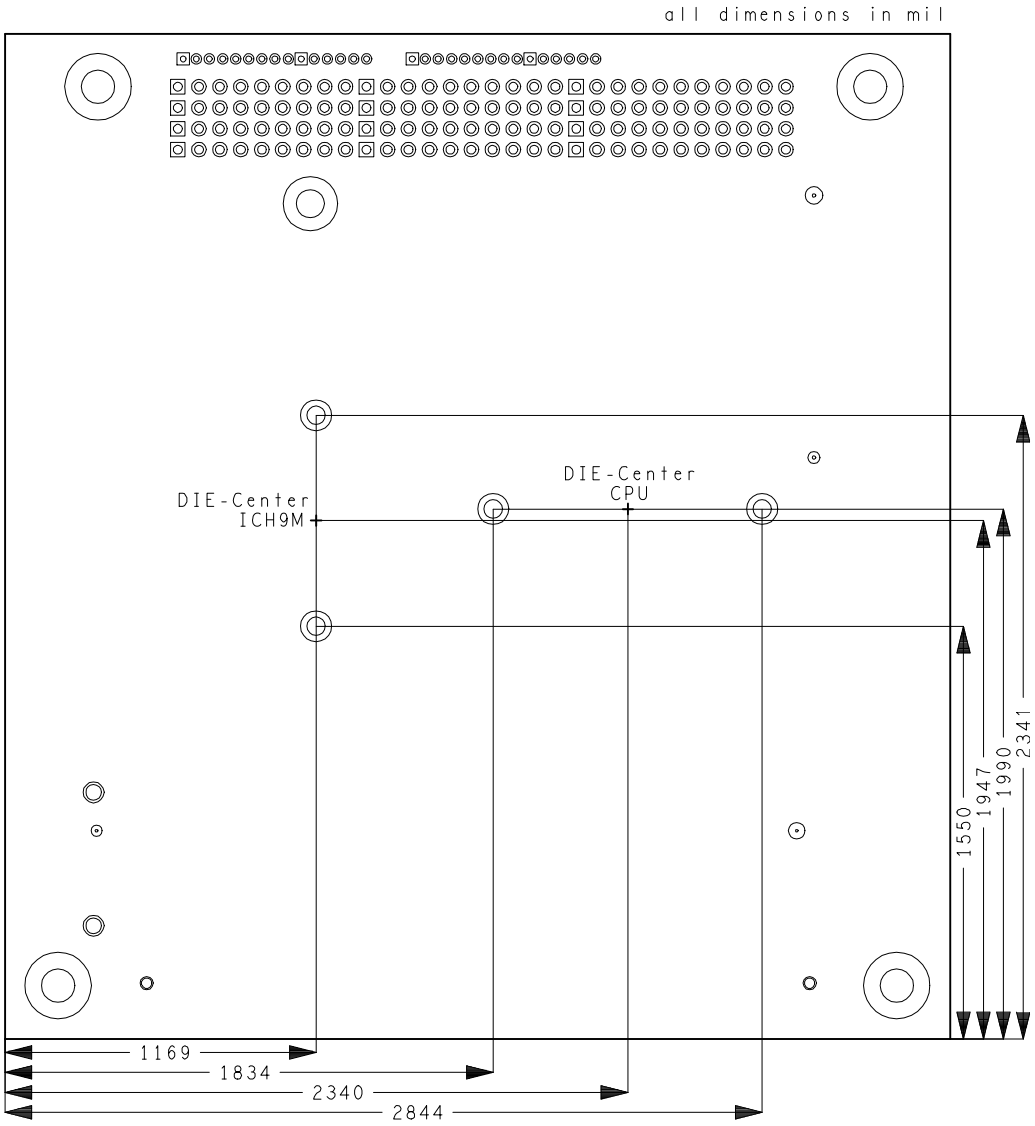
All dimensions are in mil (1 mil = 0,0254 mm)



7.3 PCB: Heat Sink

NOTE

All dimensions are in mil (1 mil = 0,0254 mm)

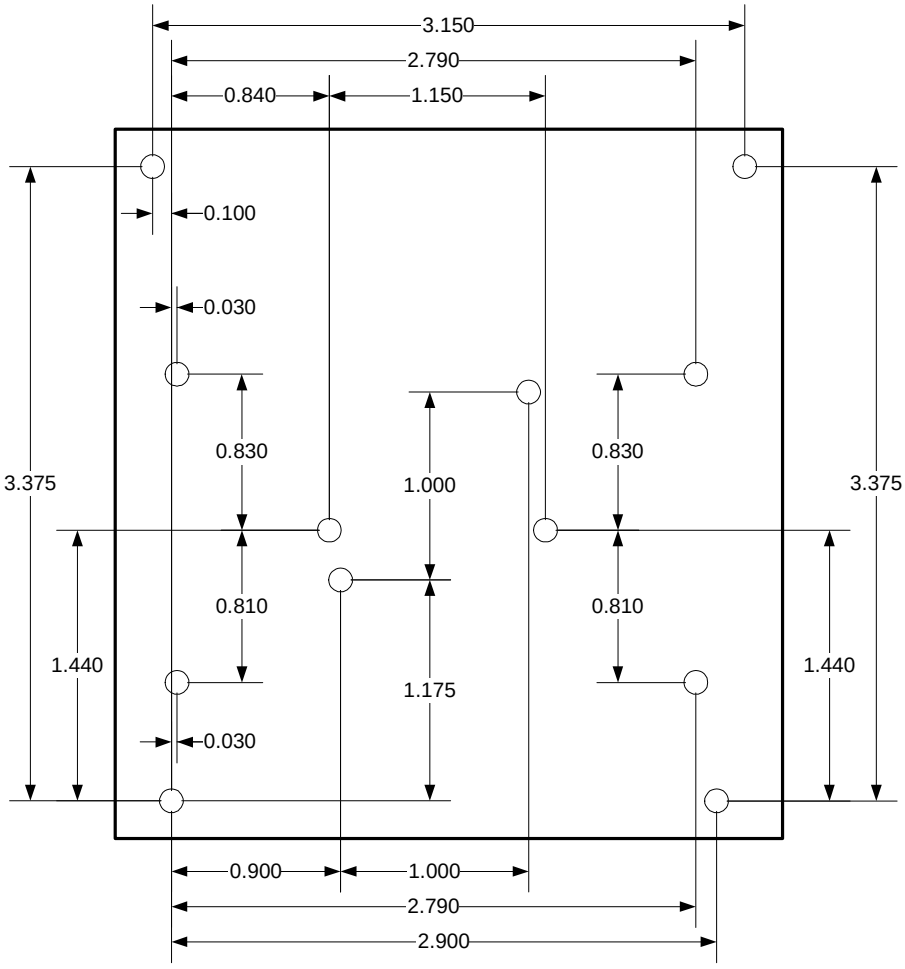


7.4 Heat Spreader: Chassis Mount

The figure below includes all hole spacing for each heat spreader available and can be used to aid in mating the heat spreader to a bulkhead or chassis.

NOTE

Dimensions are in inch (1 in = 2.54cm; 1 mil = 0.0254 mm)



8 Technical Data

8.1 Electrical Data

Power Supply:

Board:	5 Volt and 12 Volt (+/- 5%)
RTC:	>= 3 Volt

Electric Power Consumption:

Board:	3.16A Peak, 2.25A Idle (D525)
RTC:	<= 10µA

8.2 Environmental Conditions

Temperature Range:

Operating:	-25°C to +70°C (using approved thermal solution)
	-40°C up to +85°C (when pre-screened for use with an approved thermal solution)
Storage:	-40°C up to +85°C
Shipping:	-40°C up to +85°C, for packaged boards

Temperature Changes:

Operating:	0.5°C per minute, 7.5°C per 30 minutes
Storage:	1.0°C per minute
Shipping:	1.0°C per minute, for packaged boards

Relative Humidity:

Operating:	5% up to 85% (non condensing)
Storage:	5% up to 95% (non condensing)
Shipping:	5% up to 100% (non condensing), for packaged boards

Shock:

Operating:	150m/s^2, 6ms
Storage:	400m/s^2, 6ms
Shipping:	400m/s^2, 6ms, for packaged boards

Vibration:

Operating:	10 up to 58Hz, 0.075mm amplitude
	58 up to 500Hz, 10m/s^2
Storage:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2
Shipping:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2, for packaged boards

CAUTION

Shock and vibration figures pertain to the motherboard alone and do not include additional components such as heat sinks, memory modules, cables etc.

8.3 Thermal Specifications

The board is specified to operate in an environmental temperature range from -25°C to +70°C when using an approved thermal solution, and an extended temperature range of -40°C to +85°C when pre-screened for use with an approved thermal solution.
Maximum die temperature is 100°C. To keep the processor under this threshold an appropriate cooling solution needs to be applied. This solution has to take typical and maximum power consumption into account. The maximum power consumption may be twice as high and should be used as a basis for the cooling concept. Additional controllers may also affect the cooling concept. The power consumption of such components may be comparable to the consumption of the processor.
The board design includes thermal solution mounting points that will provide the best possible thermal interface between die and solution. Since we take thermal solutions seriously we have several advanced, aggressive cooling solutions in our product portfolio. Please contact your sales representative to order or discuss your thermal solution needs.

CAUTION

The end customer has the responsibility to ensure that the die temperature of the processor does not exceed 100°C. Permanent overheating may destroy the board!
In case the temperature exceeds 100°C the environmental temperature must be reduced. Under certain circumstances sufficient air circulation must be provided.

CAUTION

The ADLD25PC includes circuitry that will notify an intelligent power supply to shut down if the processor reaches a critical temperature. This is achieved by deasserting the (low-active) PS_ON# signal found on the SM-Bus connector. When PS_ON# is no longer pulled low, an intelligent power supply would take this as a signal to shut down power. For this to work, PS_ON# must be connected to the power supply's PS_ON input. If PS_ON# is not otherwise connected, the ADLD25PC can be damaged beyond repair if a thermal shutdown event occurs. In rare instances, if power is not shut down, the board will continue to heat up until failure occurs.

I Annex: Post-Codes

Code	Description
01h	The Xgroup-program code is written in the random access memory from address 1000:0 onwards.
03h	Initialise Variable/Routine "Superio_Early_Init".
05h	1. Cancel display 2. Cancel CMOS error flag
07h	1. Cancel 8042 (keyboard controller) Interface Register 2. Initialising and self testing of 8042 (keyboard controller)
08h	1. Test of special keyboard controllers (Winbond 977 super I/O Chip-series). 2. Enabling of the keyboard-interface register
0Ah	1. Disabling of the PS/2 mouse interface (optional). 2. Auto-detection of the connectors for Keyboard and mouse, optional: swap of PS/2 mouse ports and PS/2 interfaces.
0Eh	Test of the F000h-memory segment (Read/Write ability). In case of an error a signal will come out of the loud speakers.
10h	Auto-detection of the flash-rom-type and loading of the suitable Read/Write program into the run time memory segment F000 (it is required for ESCD-data & the DMI-pool-support).
12h	Interface-test of the CMOS RAM-logic (walking 1's"-algorithm). Setting of the power status of the real-time-clock (RTC), afterwards test of register overflow.
14h	Initialising of the chip-set with default values. They can be modified through a software (MODBIN) by the OEM-customer.
16h	Initialise Variable/Routine "Early_Init_Onboard_Generator".
18h	CPU auto-detection (manufacturer, SMI type (Cyrix or Intel), CPU-class (586 or 686).
1Bh	Initialising if the interrupt pointer table. If nothing else is pretended, the hardware interrupts will point on "SPURIOUS_INT_HDLR and the software interrupts will point on SPURIOUS_soft_HDLR.
1Dh	Initialise Variable/Routine EARLY_PM_INIT.
1Fh	Load the keyboard table (Notebooks)
21h	Initialising of the hardware power management (HPM) (Notebooks)
23h	1. Test the validity of the RTC-values (Example: "5Ah" is an invalid value for an RTC-minute). 2. Load the CMOS-values into the BIOS Stack. Default-values are loaded if CMOS-checksum errors occur. 3. Preparing of the BIOS 'resource map' for the PCI & plug and play configuration. If ESCD is valid, take into consideration the ESCD's legacy information. 4. Initialise the onboard clock generator. Clock circuit at non-used PCI- and DIMM slots. 5. First initialising of PCI-devices: assign PCI-bus numbers - alot memory- & I/O resources - search for functional VGA-controllers and VGA-BIOS and copy the latter into memory segment C000:0 (Video ROM Shadow).
27h	Initialise cache memory for INT 09
29h	1. Program the CPU (internal MTRR at P6 and PII) for the first memory address range (0-640K). 2. Initialising of the APIC at CPUs of the Pentium-class. 3. Program the chip-set according to the settings of the CMOS-set-up (Example: Onboard IDE-controller). 4. Measuring of the CPU clock speed. 5. Initialise the video BIOS.
2Dh	1. Initialise the "Multi-Language"-function of the BIOS 2. Soft copy, e.g. Award-Logo, CPU-type and CPU clock speed…
33h	Keyboard-reset (except super I/O chips of the Winbond 977 series)
3Ch	Test the 8254 (timer device)
3Eh	Test the interrupt Mask bits of IRQ-channel 1 of the interrupt controller 8259.
40h	Test the interrupt Mask bits of IRQ-channel 2 of the interrupt controller 8259
43h	Testing the function of the interrupt controller (8259).
47h	Initialise EISA slot (if existent).

Code	Description
49h	1. Determination of the entire memory size by revising the last 32-Bit double word of each 64k memory segment. 2. Program “write allocation” at AMD K5-CPUs.
4Eh	1. Program MTRR at M1 CPUs 2. Initialise level 2-cache at CPUs of the class P6 and set the “cacheable range” of the random access memory. 3. Initialise APIC at CPUs of the class P6. 4. Only for multiprocessor systems (MP platform): Setting of the “cacheable range” on the respective smallest value (for the case of non-identical values).
50h	Initialise USB interface
52h	Testing of the entire random access memory and deleting of the extended memory (put on “0”)
55h	Only for multi processor systems (MP platform): Indicate the number of CPUs.
57h	1. Indicate the plug and play logo 2. First ISA plug and play initialising – CSN-assignment for each identified ISA plug and play device.
59h	Initialise TrendMicro anti virus program code.
5Bh	(Optional:) Indication of the possibility to start AWDFLASH.EXE (Flash ROM programming) from the hard disk.
5Dh	1. Initialise Variable/Routine Init_Onboard_Super_IO. 2. Initialise Variable/Routine Init_Onbaord_AUDIO.
60h	Release for starting the CMOS set-up (this means that before this step of POST, users are not able to access the BIOS set-up).
65h	Initialising of the PS/2 mouse.
67h	Information concerning the size of random access memory for function call (INT 15h with AX-Reg. = E820h).
69h	Enable level 2 cache
6Bh	Programming of the chip set register according to the BIOS set-up and auto-detection table.
6Dh	1. Assignment of resources for all ISA plug and play devices. 2. Assignment of the port address for onboard COM-ports (only if an automatic junction has been defined in the setup).
6Fh	1. Initialising of the floppy controller 2. Programming of all relevant registers and variables (floppy and floppy controller).
73h	Optional feature: Call of AWDFLASH.EXE if: - the AWDFLASH program was found on a disk in the floppy drive. - the shortcut ALT+F2 was pressed.
75h	Detection and installation of the IDE drives: HDD, LS120, ZIP, CDROM…
77h	Detection of parallel and serial ports.
7Ah	Co-processor is detected and enabled.
7Fh	1. Switch over to the text mode, the logo output is supported. - Indication of possibly emerged errors. Waiting for keyboard entry. - No errors emerged, respective F1 key was pressed (continue): Deleting of the EPA- or own logo.
82h	1. Call the pointer to the “chip set power management”. 2. Load the text font of the EPA-logo (not if a complete picture is displayed) 3. If a password is set, it is asked here.
83h	Saving of the data in the stack, back to CMOS.
84h	Initialising of ISA plug and play boot drives (also Boot-ROMs)
85h	1. Final initialising of the USB-host. 2. At network PCs (Boot-ROM): Construction of a SYSID structure table 3. Backspace the scope presentation into the text mode 4. Initialise the ACPI table (top of memory). 5. Initialise and link ROMs on ISA cards 6. Assignment of PCI-IRQs 7. Initialising of the advanced power management (APM) 8. Set back the IRQ-register.

Code	Description
93h	Reading in of the hard disk boot sector for the inspection through the internal anti virus program (trend anti virus code)
94h	1. Enabling of level 2 cache 2. Setting of the clock speed during the boot process 3. Final initialising of the chip set. 4. Final initialising of the power management. 5. Erase the onscreen and display the overview table (rectangular box). 6. Program “write allocation” at K6 CPUs (AMD) 7. Program “write combining” at P6 CPUs (INTEL)
95h	1. Program the changeover of summer-and winter-time 2. Update settings of keyboard-LED and keyboard repeat rates
96h	1. Multi processor system: generate MP-table 2. Generate and update ESCD-table 3. Correct century settings in the CMOS (20xx or 19xx) 4. Synchronise the DOS-system timer with CMOS-time 5. Generate an MSIRQ-Routing table..
C0h	Chip set initialising: - Cut off shadow RAM - Cut off L2 cache (apron 7 or older) - Initialise chip set register
C1h	Memory detection: Auto detection of DRAM size, type and error correction (ECC or none) Auto detection of L2 cache size (apron 7 or older)
C3h	Unpacking of the packed BIOS program codes into the random access memory.
C5h	Copying of the BIOS program code into the shadow RAM (segments E000 & F000) via chipset hook.
CFh	Testing of the CMOS read/write functionality
FFh	Boot trial over boot-loader-routine (software-interrupt INT 19h)

II Annex: Resources

A IO Range

The used resources depend on setup settings.
The given values are ranges, which are fixed by AT compatibility. Other IO ranges are used, which are dynamically adjusted by Plug & Play BIOS while booting.

Address	Function
0-FF	Reserved IO area of the board
170-17F	
1F0-1F7	IDE1
278-27F	
2E8-2EF	COM4
2F8-2FF	COM2
370-377	
378-37F	LPT1
3BC-3BF	
3E8-3EF	COM3
3F0-3F7	
3F8-3FF	COM1

B Memory Range

The used resources depend on setup settings.
If the entire range is clogged through option ROMs, these functions do not work anymore.

Address	Function
A0000-BFFFF	VGA RAM
C0000-CFFFF	VGA BIOS
D0000-DFFFF	AHCI BIOS / RAID / PXE (if available)
E0000-EFFFF	System BIOS while booting
F0000-FFFFF	System BIOS

C Interrupt

The used resources depend on setup settings.
The listed interrupts and their use are given through AT compatibility.
If interrupts must exclusively be available on the ISA side, they have to be reserved through the BIOS setup. The exclusivity is not given and not possible on the PCI side.

Address	Function
IRQ0	Timer
IRQ1	PS/2 Keyboard
IRQ2 (9)	COM3
IRQ3	COM1
IRQ4	COM2
IRQ5	COM4
IRQ6	
IRQ7	LPT1
IRQ8	RTC
IRQ9	
IRQ10	
IRQ11	

Address	Function
IRQ12	PS/2 Mouse
IRQ13	FPU
IRQ14	IDE Primary
IRQ15	

D PCI Devices

All listed PCI devices exist on the board. Some PCI devices or functions of devices may be disabled in the BIOS setup. Once a device is disabled other devices may get PCI bus numbers different from the ones listed in the table.

AD	INTA	REQ	Bus	Dev.	Fct.	Controller / Slot
	-	-	0	0	0	Host Bridge IDA000h
	A	-	0	2	0	VGA Graphics IDA001h
	-	-	0	2	1	Non-VGA Graphics IDA002h
	A	-	0	25	0	LAN ICH9 ID10F5h
	A	-	0	26	0	USB UHCI Controller #4 ID2937h
	B	-	0	26	1	USB UHCI Controller #5 ID2938h
	D	-	0	26	2	USB UHCI Controller #6 ID2939h
	C	-	0	26	7	USB 2.0 EHCI Controller #2 ID293Ch
	A	-	0	27	0	HDA Controller ID293Eh
	A	-	0	28	0	PCI Express Port 1 ID2940h
	A	-	0	28	3	PCI Express Port 4 ID2946h
	A	-	0	28	4	PCI Express Port 5 ID2948h
	A	-	0	29	0	USB UHCI Controller #1 ID2934h
	B	-	0	29	1	USB UHCI Controller #2 ID2935h
	C	-	0	29	2	USB UHCI Controller #3 ID2936h
	A	-	0	29	7	USB 2.0 EHCI Controller #1 ID293Ah
	-	-	0	30	0	DMI-to-PCI Bridge ID2448h
	-	-	0	31	0	LPC Interface ID2917h
	B	-	0	31	2	SATA Interface #1 ID2928h
	B	-	0	31	3	SMBus Interface ID2930h
	B	-	0	31	5	SATA Interface #2 ID292Dh
20	A	0	(2)	4		External Slot 1
21	B	1	(2)	5		External Slot 2
22	C	2	(2)	6		External Slot 3
23	D	3	(2)	7		External Slot 4

E SMB Devices

The following table contains all reserved SM-Bus device addresses in 8-bit notation. Note that external devices must not use any of these addresses even if the component mentioned in the table is not present on the motherboard.

Address	Function
10-11	Standard slave address
40-41	GPIO
60-61	BIOS internal
70-73	POST code output
88-89	BIOS-defined slave address
A0-A1	DIMM 1
A2-A3	DIMM 2
A4-AF	BIOS internal
B0-BF	BIOS internal
D2-D3	Clock